A 128-channel SALT ASIC for the readout of Upstream Tracker in the LHCb Upgrade

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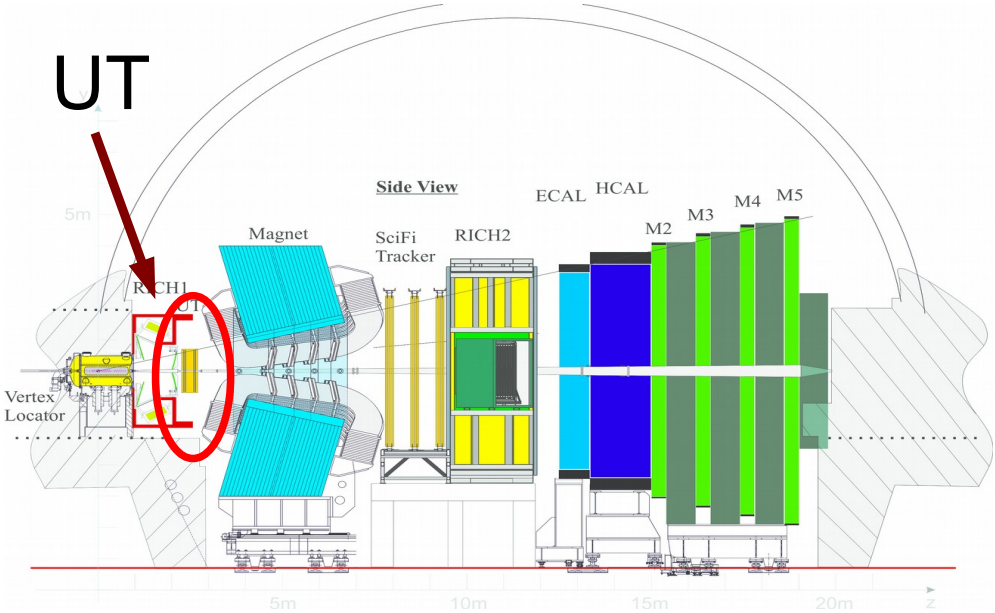
Outline

- Introduction
- SALT design
  - Main blocks (FE, ADC, DSP)
  - SALTv3 versus previous versions
- SALT measurements
  - SALT on hybrid with sensor type A – full tests with transmission of digitized data
- Summary and plans

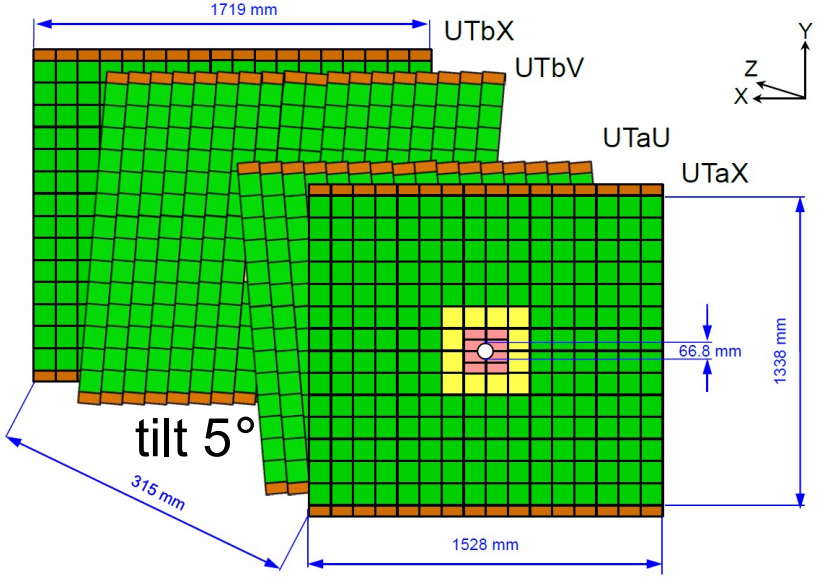
Introduction
Upgrade of LHCb Inner Tracker at LHC

- Upstream Tracker (UT) replaces the Tracker Turicensis (TT)
- 500 000 silicon strip detector channels
- Readout frequency increases to 40 MHz – *currently Level-0 trigger output is limited to 1MHz*
- New readout electronics was needed

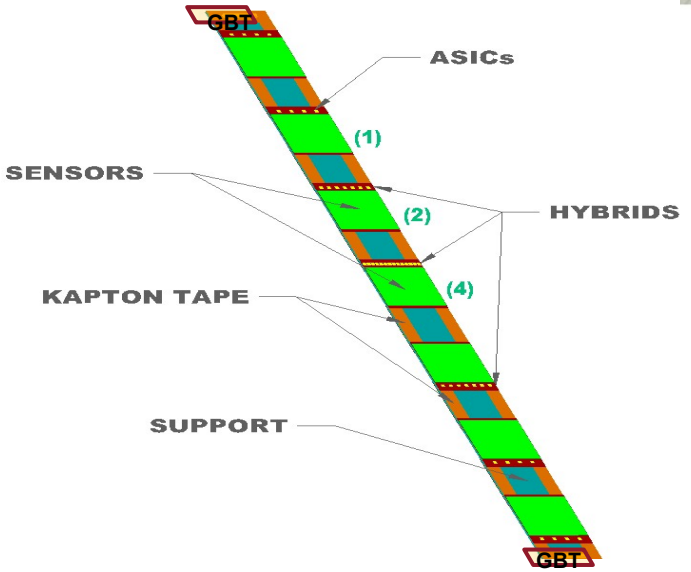


LHCb detector

Introduction
Upstream Tracker (UT)



- 4 silicon strip sensor types
  - p^+-in-n, 10 cm
  - n^+-in-p, 10/5 cm
- ~1000 hybrids with 4 or 8 ASICs



- ~4000 128-channel readout ASICs – SALT
- Data rate depends on position – different number of active e-links in SALT

Introduction
SALT specification

- CMOS 130 nm technology
- 128 channels, Front-end & ADC in each channel
- In/Out pitch 80/140um, No Top/Bottom pads (previous ver.) SALTv3 uses it
- Sensor: capacitance 1.6–12 pF, AC coupled
- Input charge range ~30ke– with both polarities (p^+-in-n and n^+-in-p)
- Noise: ENC ~1000e– @10pF + 50e–/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after $2*T_{peak}$
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit&polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization & Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~30 MRad

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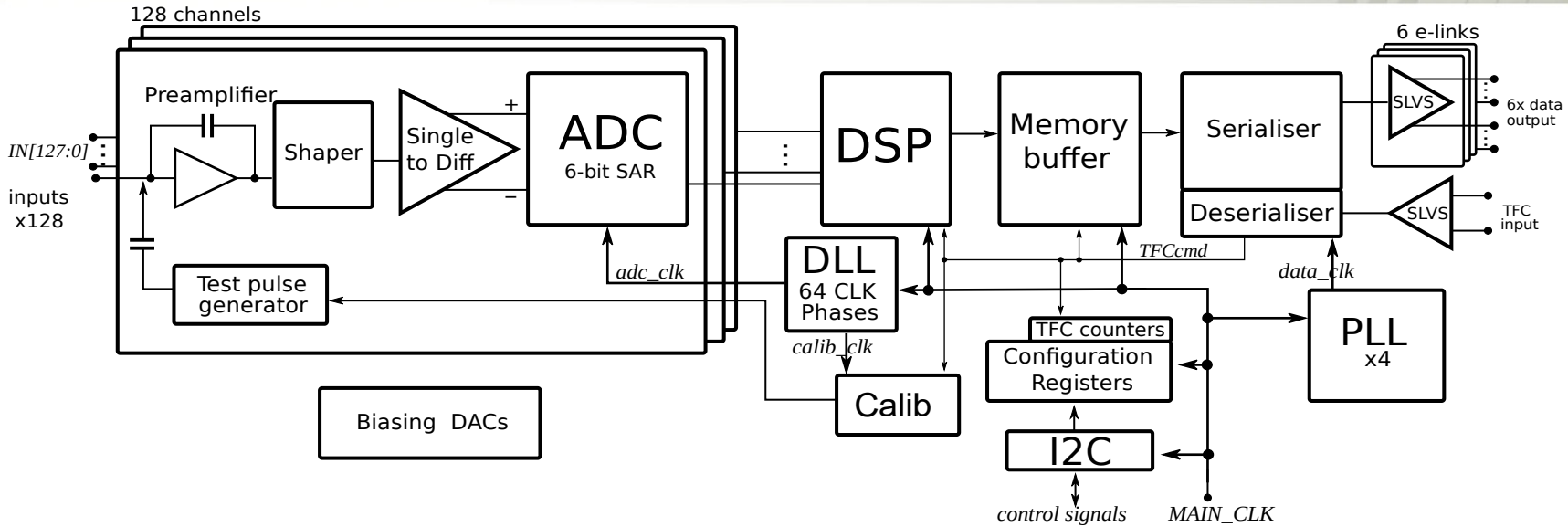
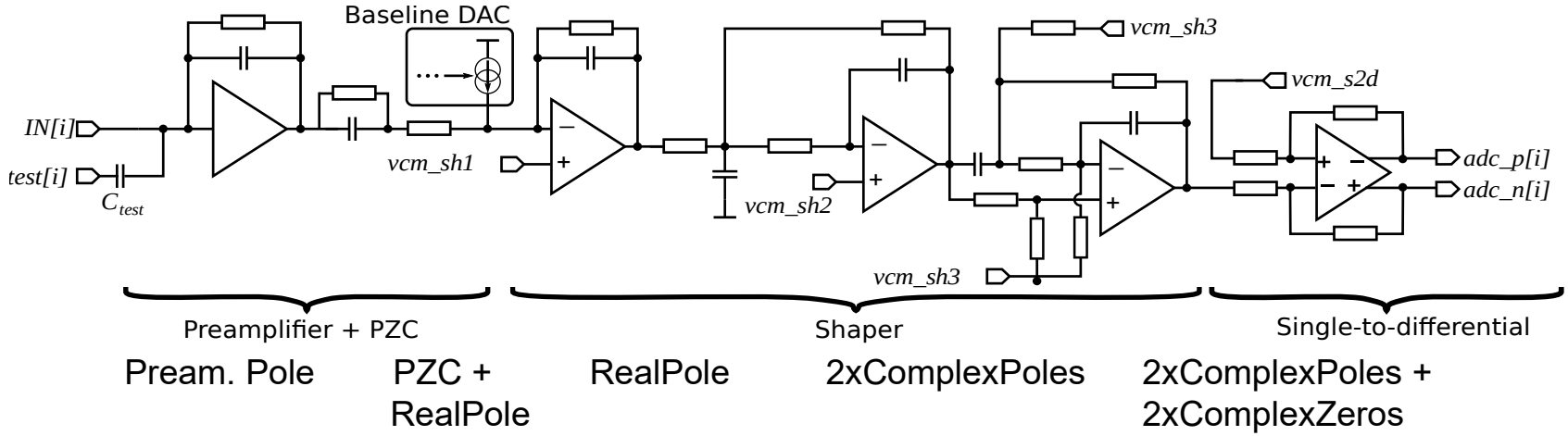
SALT – Silicon ASIC for LHCb Tracking Architecture



- Front-end & ADC in each channel – 128 standard channels plus 2 test channels (nr -1,128 not shown) with analog outputs
- Digital Signal Processing (DSP) of the ADC data
- And many other features/blocks: PLL, DLL, TFC, I2C, serialiser, SLVS I/O, biasing DACs, monitoring ADCs, ... (not all shown)

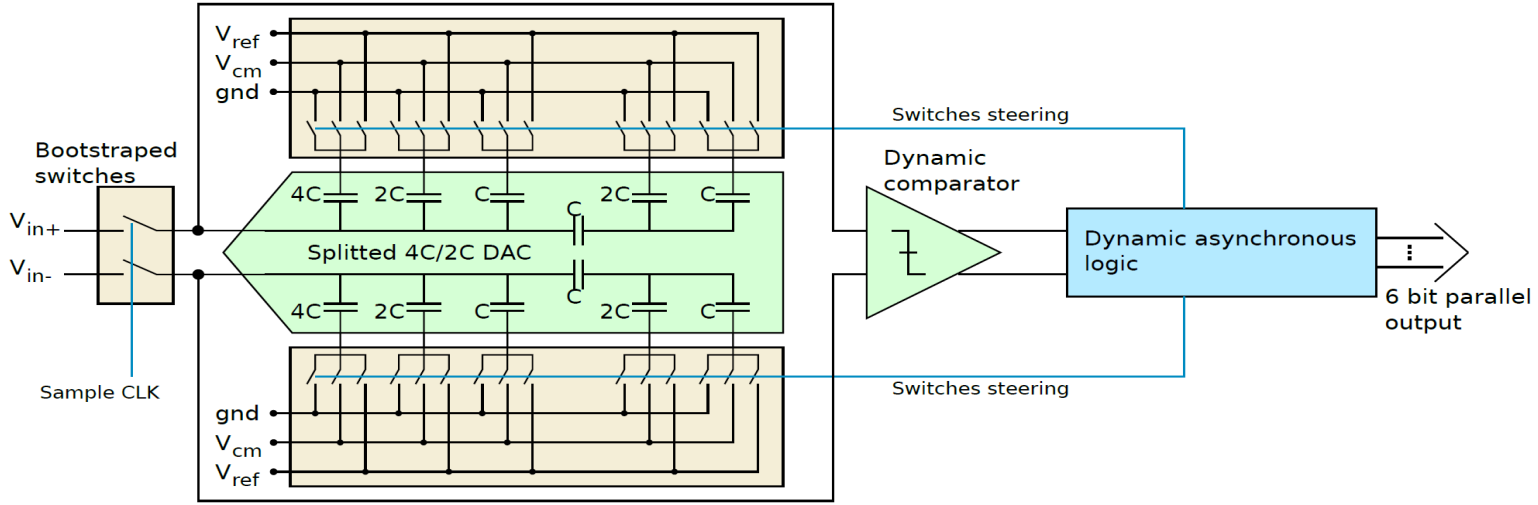
SALT design
Preamplifier&Shaper and Conv. Single-to-Diff.

Simplified circuit diagram



- 3-stage shaper (complex poles and zeros) gives the pulse with short tail
- Common mode (vcm_sh) at half power supply for both pulse polarities
- Single-to-Differential converter to generate differential signal for ADC
- Power consumption: ~1.5 mW

SALT design
6-bit ADC



SALTv3:

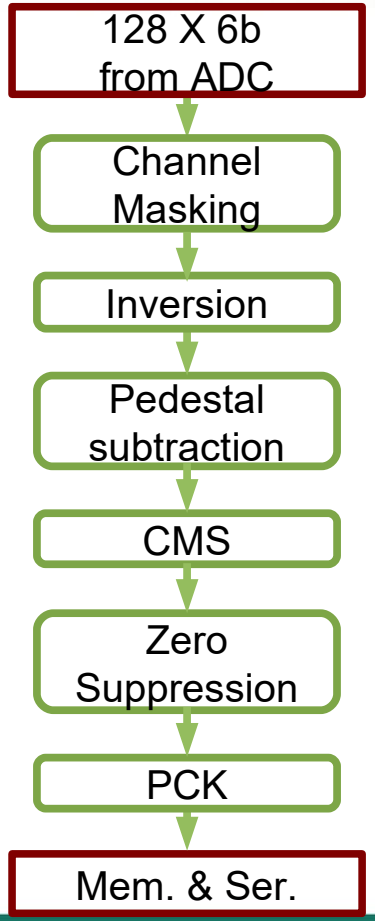
optional dummy current added (constant current after conversion) to keep current consumption more stable

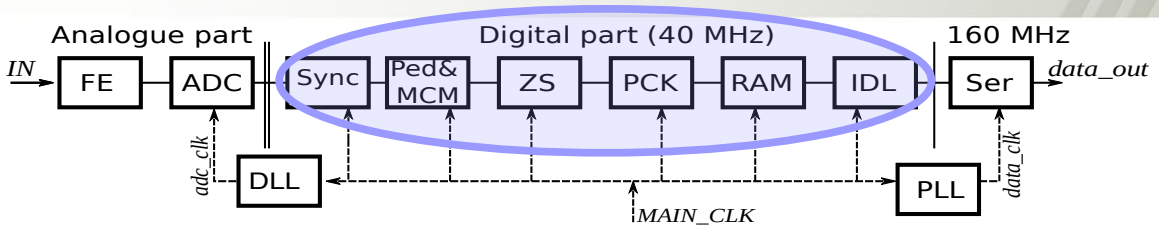
Main features:

- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Merge Capacitor Switching (MCS)
- Capacitive DAC with 3b/2b split

- Dynamic comparator
- Dynamic asynchronous logic
- Bootstrapped input switches
- Power consumption ~350µW+400µW

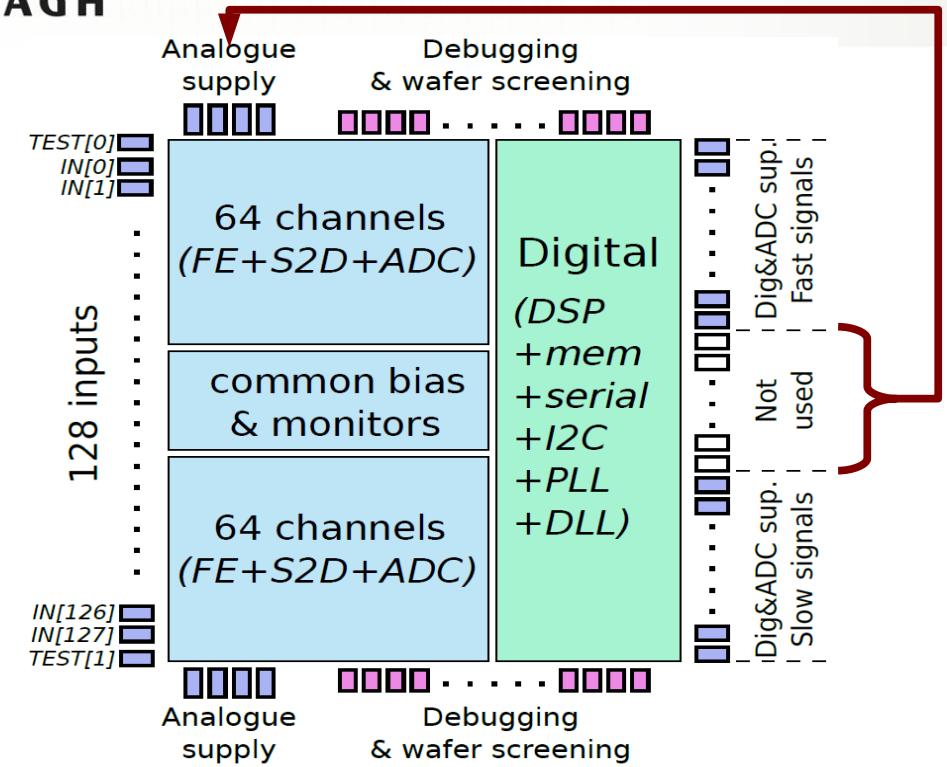
SALT design
DSP operations





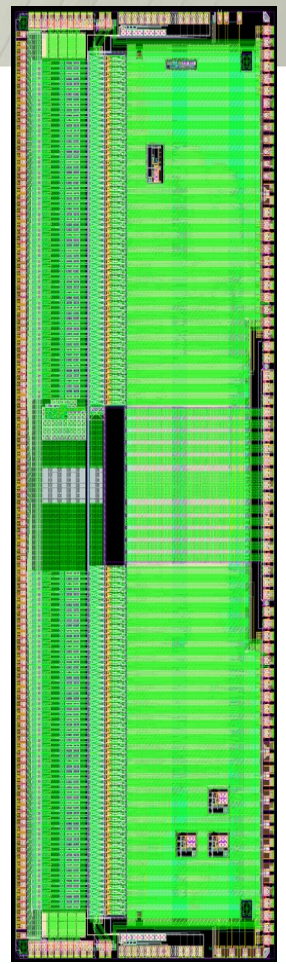
- Input data: 6 bits (5 bits plus sign – 2's complement)
- Noisy or dead channels can be masked
- All channel values can be inverted (1 config bit)
- Pedestal subtraction – subtraction in each channel
- CMS – (Mean) Common Mode Subtraction
  - average of all channels below CM threshold
  - subtraction in each channel
- ZS – Zero suppression
  - only channels above ZS threshold are sent out
- PCK – Packet building

SALT Design
Floorplan and layout – SALTv3 changes



- Left & right sides bonded to the hybrid.
- **Top&bottom pads for analog supply**

- Unsatisfactory SALTv2 performance was attributed mainly to internal inductive couplings in power distribution typically not covered by extraction tools
- Analogue power distribution redesign to minimize inductances
- ADC supplied from digital domain mesh



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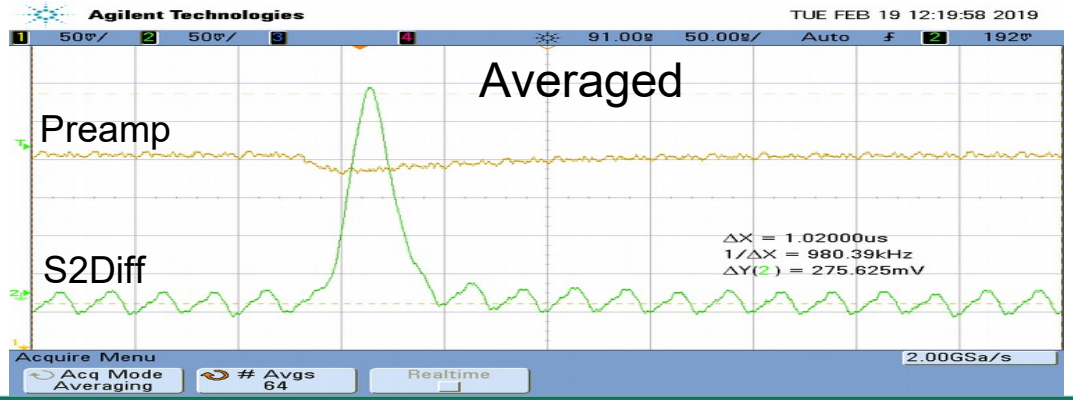
Analogue test channel output (@scope)

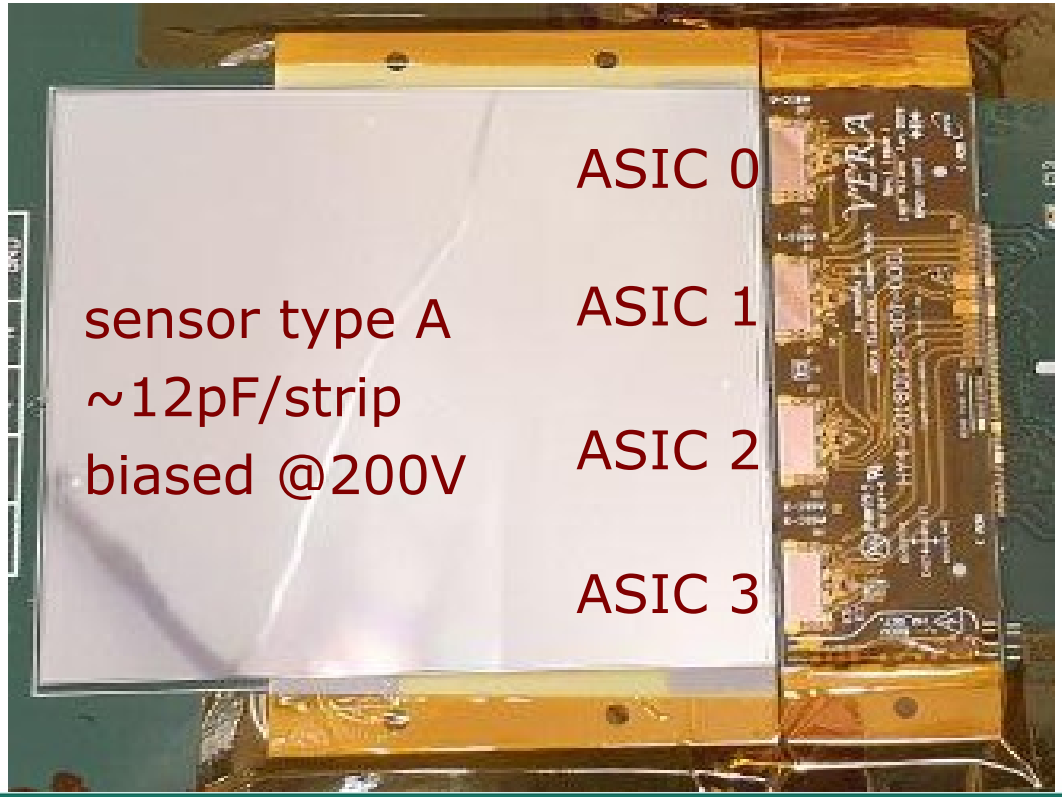


Transient response to MIP (~4fC) with 12pF external input capacitance

- For SALTv3 good pulse response is seen with large input capacitance
- With large input capacitance small 40MHz disturbance is still present (also in simulations)

SALT on hybrid with sensor A (full tests with digitized data)

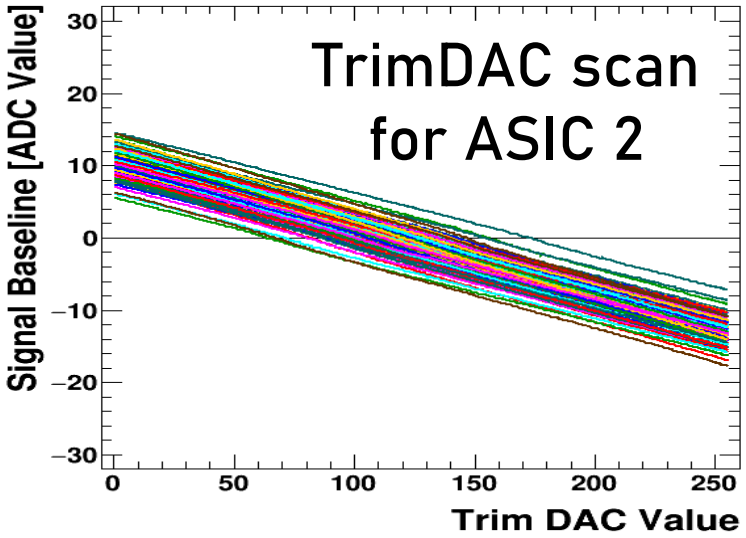
Hybrid with the largest sensor and 4 SALT ASICs



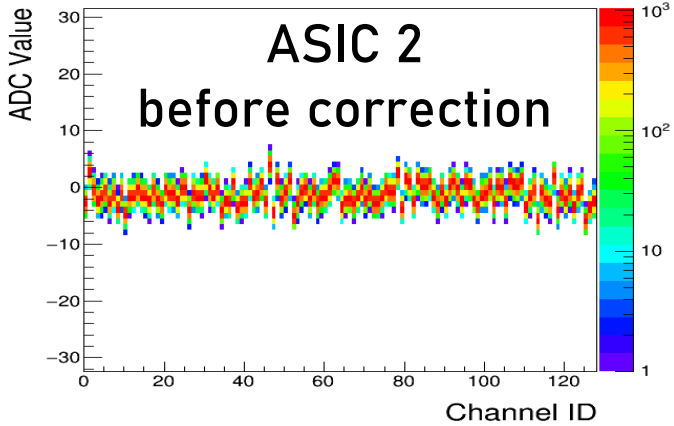
Power consumption @ Vsup=1.2 V:

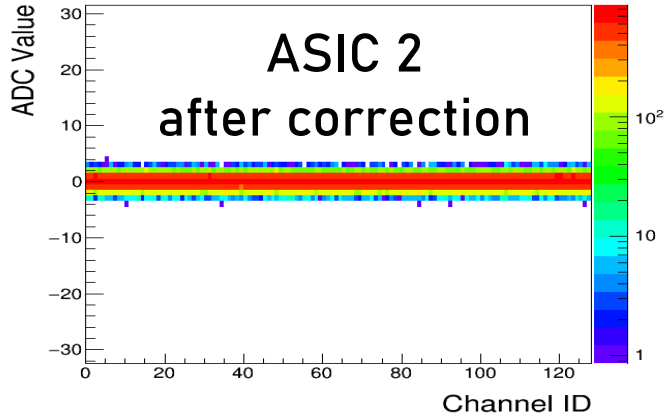
- P = ~580 mW (total)
- ~4.5 mW / channel (within spec.)

Baseline correction



Each channel is corrected by setting its own TrimDAC

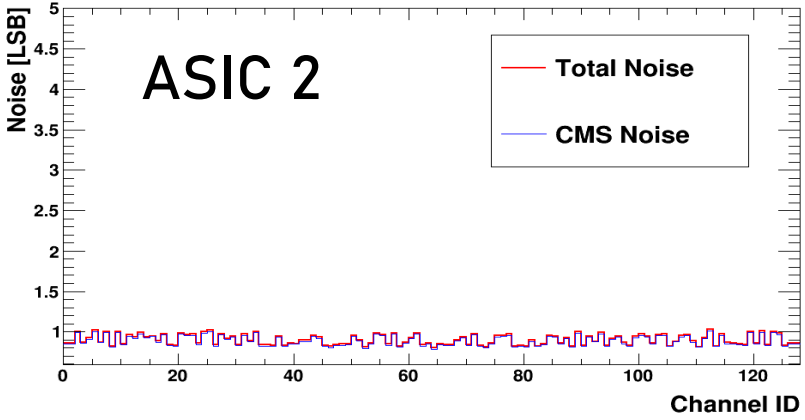




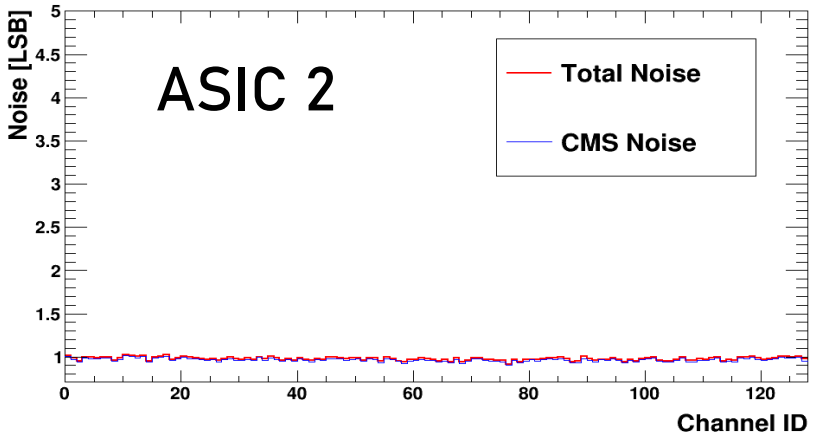
- Baseline correction works well
- These data confirm that full processing chain (analog&digital) is functionally correct

Noise with sensor type A (on hybrid)

Before TrimDAC correction



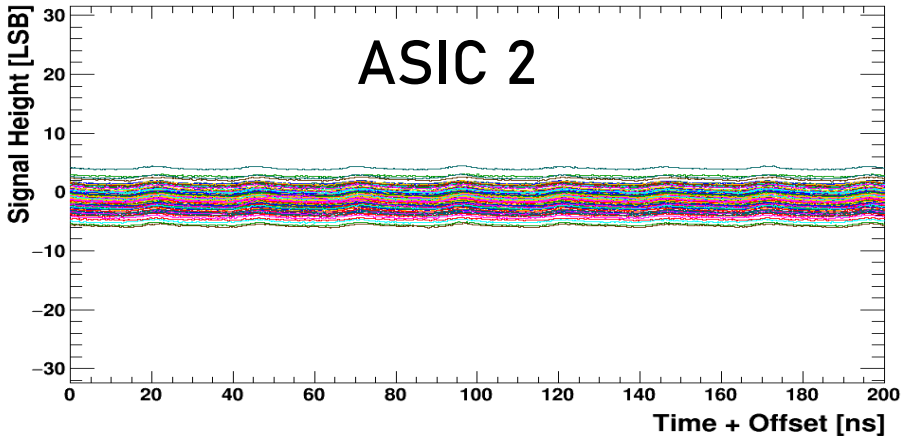
After TrimDAC correction



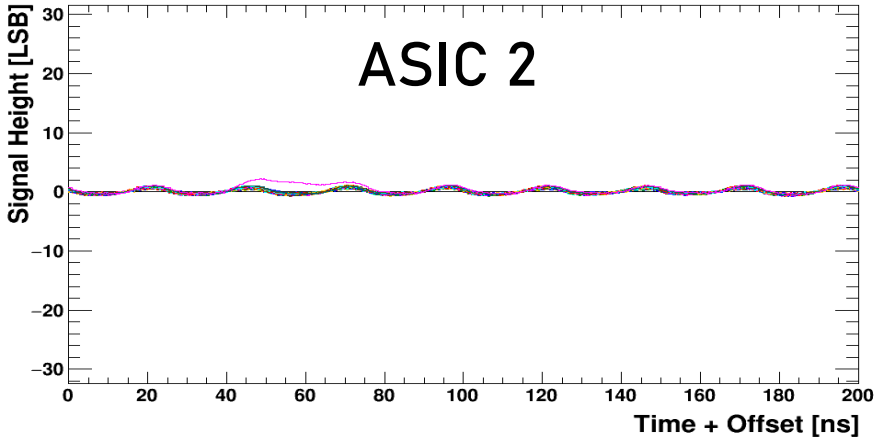
- Measurements show that noise RMS is slightly below 1 LSB
- For MIP (4 fC) one can estimate SNR above 10

Baseline versus time

Before TrimDAC correction



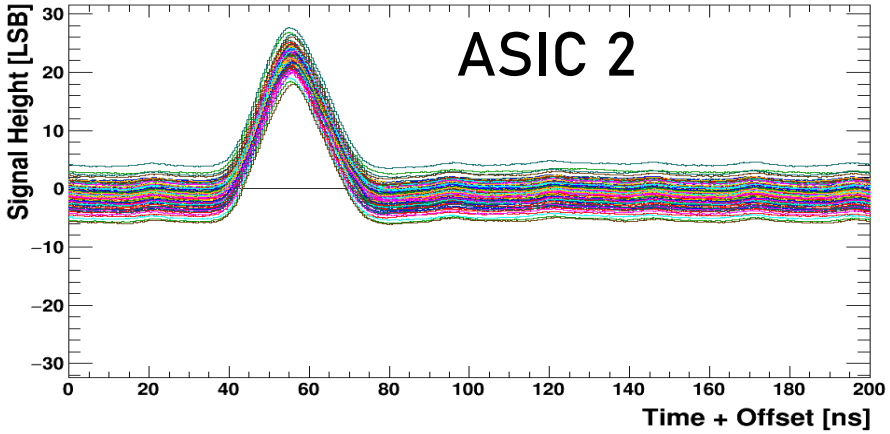
After TrimDAC correction



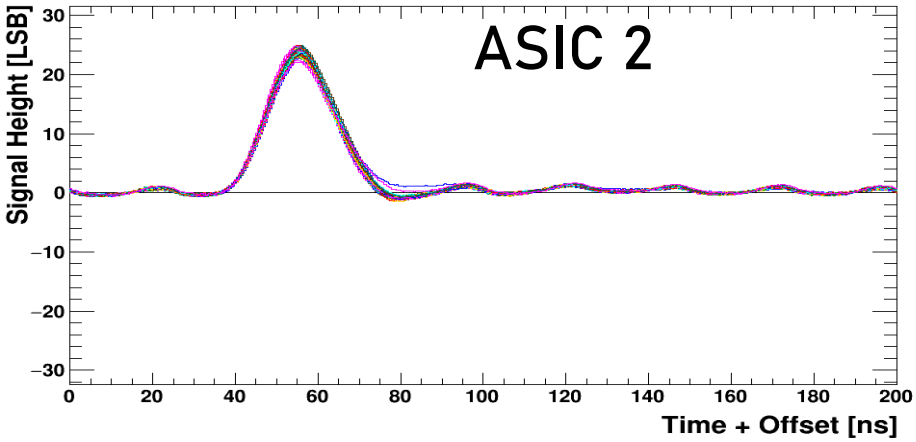
- In standard operation samples are taken every 25ns
- To obtain above plots internal DLL was scanned over all 64 phases ($\Delta t = 25ns/64$) and data was averaged for each phase
- In standard operation small 40MHz component is seen as constant offset but can be subtracted in DSP

SALT on hybrid with sensor A
Pulse shape

Before TrimDAC correction



After TrimDAC correction



- Pulse shape is obtained via DLL scan
- Expected pulse shape is observed

- Disturbances are small and similar to scope measurements of analogue test channels

Summary and plans

- The third SALT prototype, which addressed the issues found in the past, was fabricated and tested.
- The tests confirmed that the measures taken were effective.
- Good results have been obtained for 4-chip hybrid.
- Full stave tests have been already started. SALT production has been recently completed, wafer tests done.

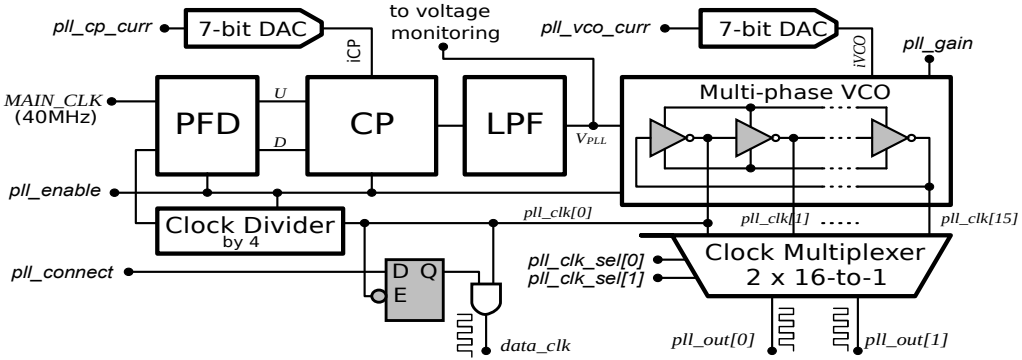
- Back side power delivery scheme will be tested soon – waiting for chips with respinned metal layers.

Thank you for your attention

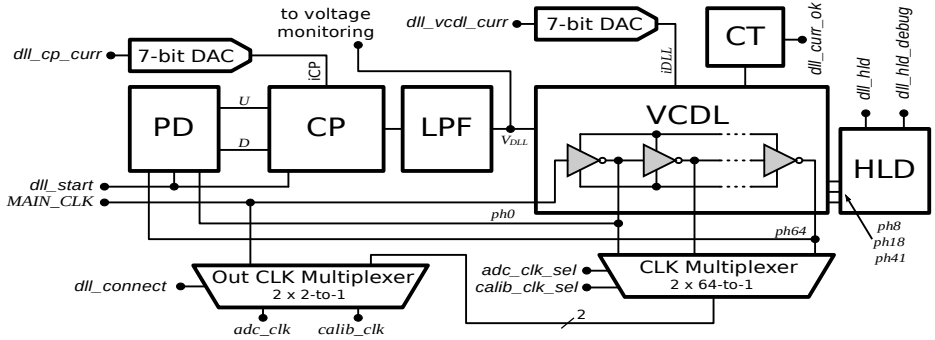
Backup

SALT design
PLL, DLL

PLL



DLL



PLL features:

- High frequency (160 MHz) clock for DDR serializer
- Input frequency 40 MHz
- Power consumption ~0.5 mW @ 160 MHz
- 2 output phases (multiplexing) selected from 16 uniform phases (receiver synchronization)

DLL features:

- ADC sampling phase setting
- Test pulse phase setting
- Input frequency 40 MHz
- Power consumption ~0.7 mW
- 2 output phases (multiplexing) selected from 64 uniform phases

SALT design
Modifications of SALTv3 versus SALTv2

- Single Channel
  - Analogue front-end – highly improved PSRR
  - ADC – dummy current option added to minimize current fluctuations
  - Power supply domains separation optimized for inductive effects
  - Decoupling of analogue supply removed to minimize LC factor
- Power distribution network
  - Analogue front-end supplied from **top&bottom** pads (issue for 8-chip hybrid),
  - ADC supplied from **digital domain mesh** (output side)
  - Layout of analogue power distribution drawn to minimize inductances

Analogue test channel output for large input capacitance (@scope)

Transient response to MIP (~4fC) with 24pF external input capacitance

- Good pulse response is seen even with 24pF input capacitance
- With this capacitance small 40MHz disturbance are also present