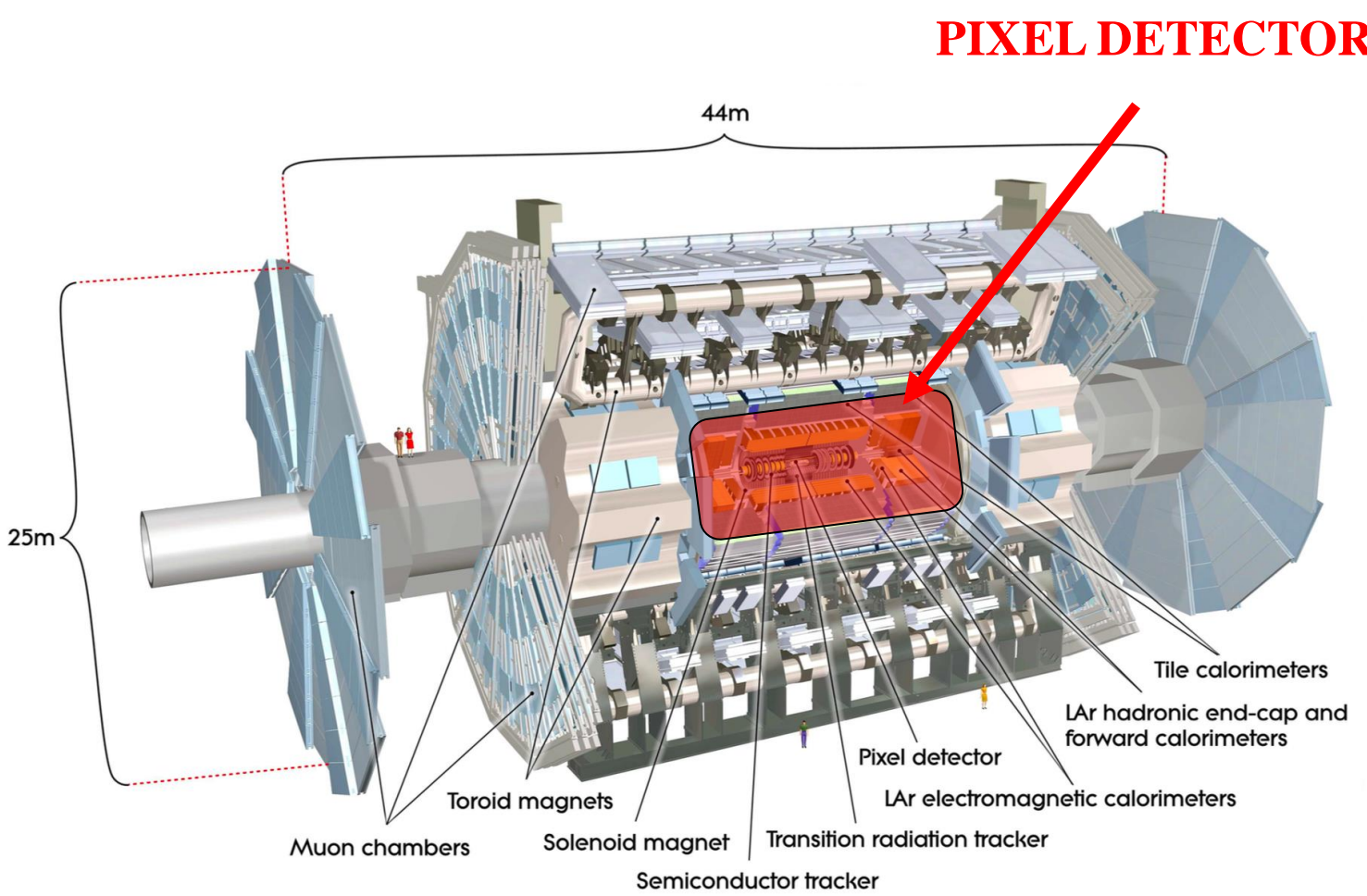


## THE ATLAS DETECTOR AT LHC



	Outer layers/ disks (B-Layer/L1/L2)	Inner Layer (IBL)
Sensor Technology	n-in-n only planar	n-in-n / n-in-p (planar/3D)
Sensor Thickness	250 $\mu\text{m}$	200/230 $\mu\text{m}$
Front end Technology	FE-13 250 nm CMOS	FE-14 130 nm CMOS
Pixel Size (typical)	50 x 400 $\mu\text{m}^2$	50 x 250 $\mu\text{m}^2$
Radiation	50 Mrad	250 Mrad
Hardness	1 x 10 <sup>15</sup> (1 MeV) neq cm <sup>-2</sup>	5 x 10 <sup>15</sup> (1 MeV) neq cm <sup>-2</sup>
Chip size	7.6 x 10.8 mm <sup>2</sup>	20.2 x 19.0 mm <sup>2</sup>
Radius	50.5/88.5/122.5 mm	33 mm

ATLAS is a general-purpose particle physics experiment at the Large Hadron Collider (LHC), built to investigate the Standard Model (SM) and beyond at TeV scale. One of the main parts of the ATLAS detector is the Inner Tracker constituted by the Pixel detector, the Silicon Strip detector (SCT) and the Transition Radiation Tracker (TRT). The Pixel detector is the innermost of them and it can be depicted as a 4-Layer (Insertable B-Layer, B-Layer or L0, Layer1 and Layer2) tracking detector in the barrel region with 3 disks on each endcap side. The Pixel detector was built with different technologies.

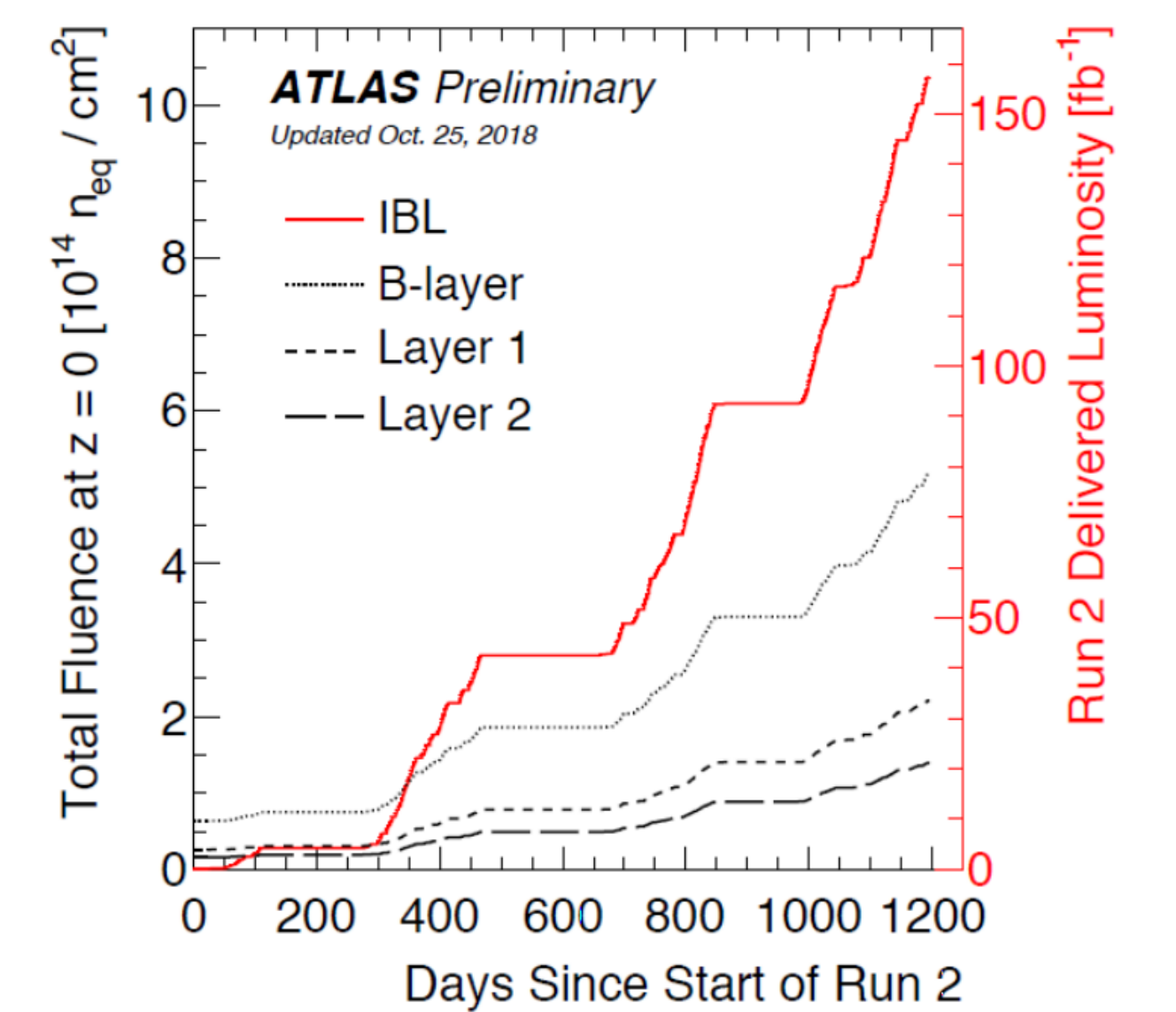
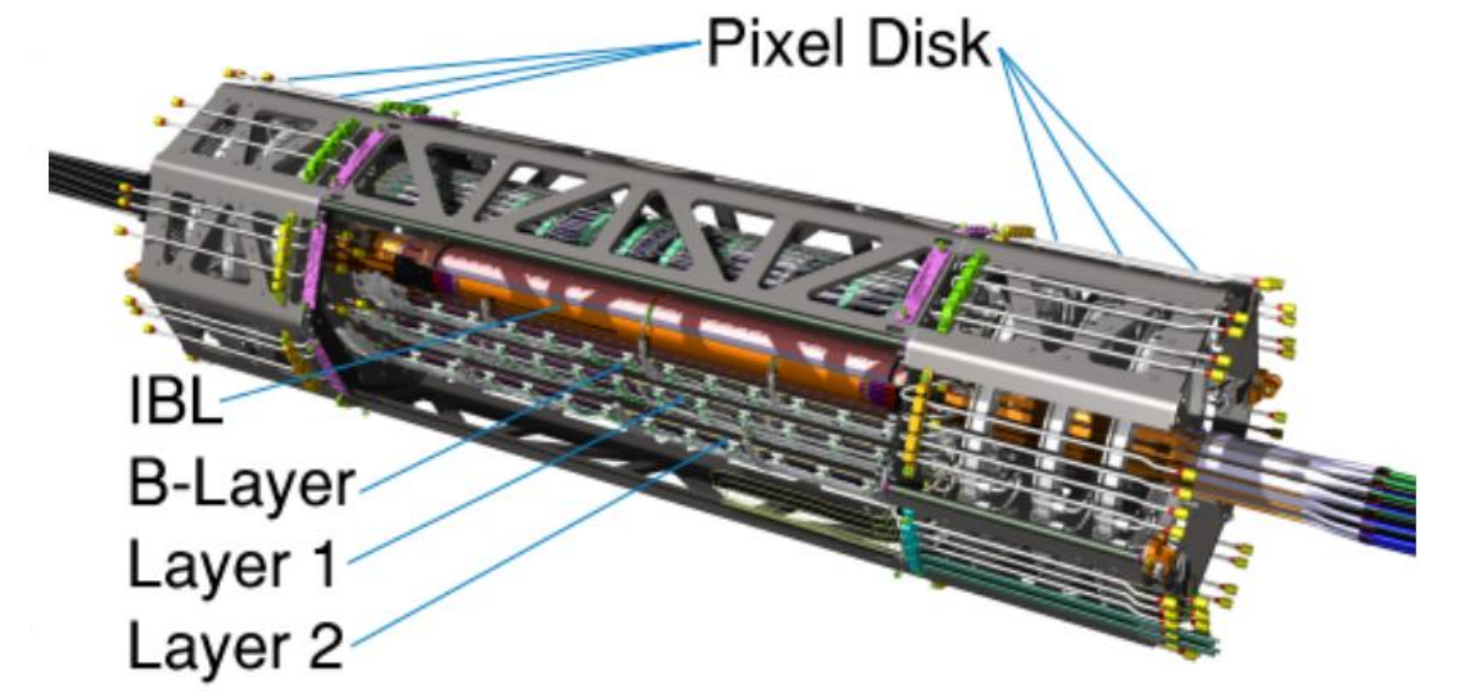
The outer layers L0, L1 and L2 installed in 2007 are built with hybrid pixel modules. Each module is composed by:

- 16 front-end chips FEI3 (250 nm CMOS technology)
- a planar n-in-n sensor

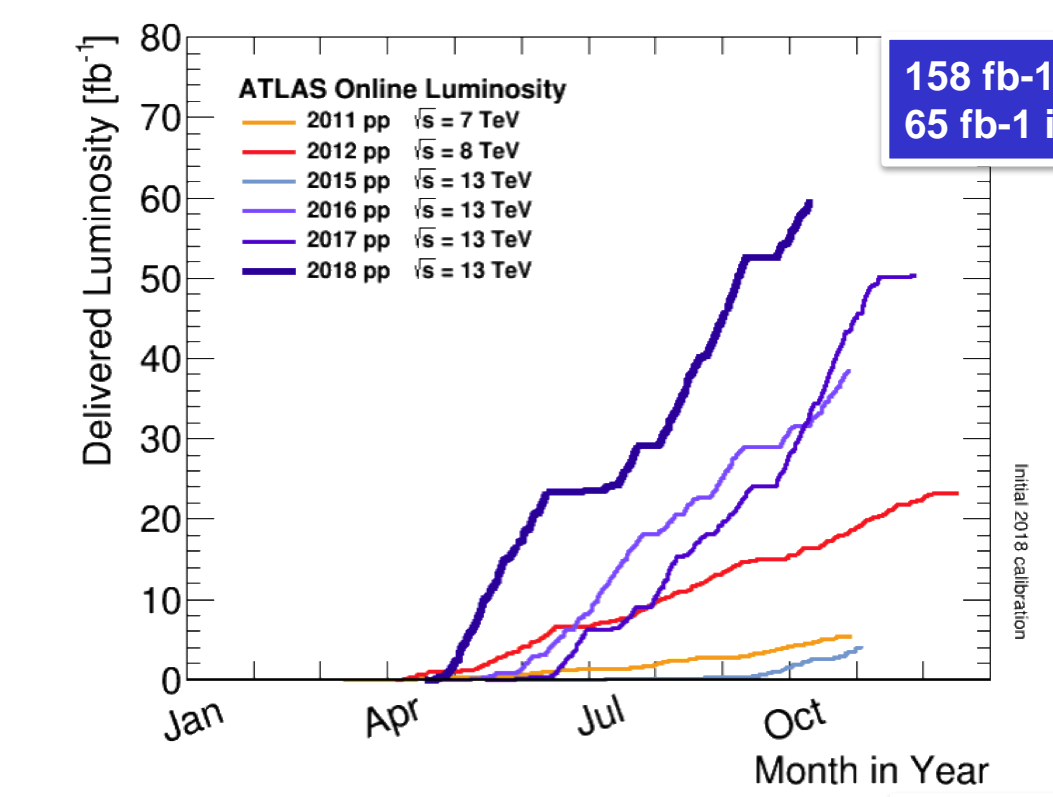
The most recent layer Insertable B-Layer (IBL), added during the LS1 in 2014, is built by modules made up of:

- a front-end chip FEI4 (130 nm CMOS technology)
- a planar n-in-n (or 3D n-in-p) sensor

The detector covers the range of  $|\eta| < 2.5$  with a resolution of  $10 \times 115 \mu\text{m}^2 / 8 \times 40 \mu\text{m}^2$  per layer (PIX/IBL). The radiation level is very challenging. The accumulated fluence at the end of Run 2, depending on the layer, ranges from  $4.5$  to  $9 \times 10^{14}$  [neq/cm<sup>2</sup>] corresponding to 40-50 % of the total fluence that can nominally be tolerated by the modules.

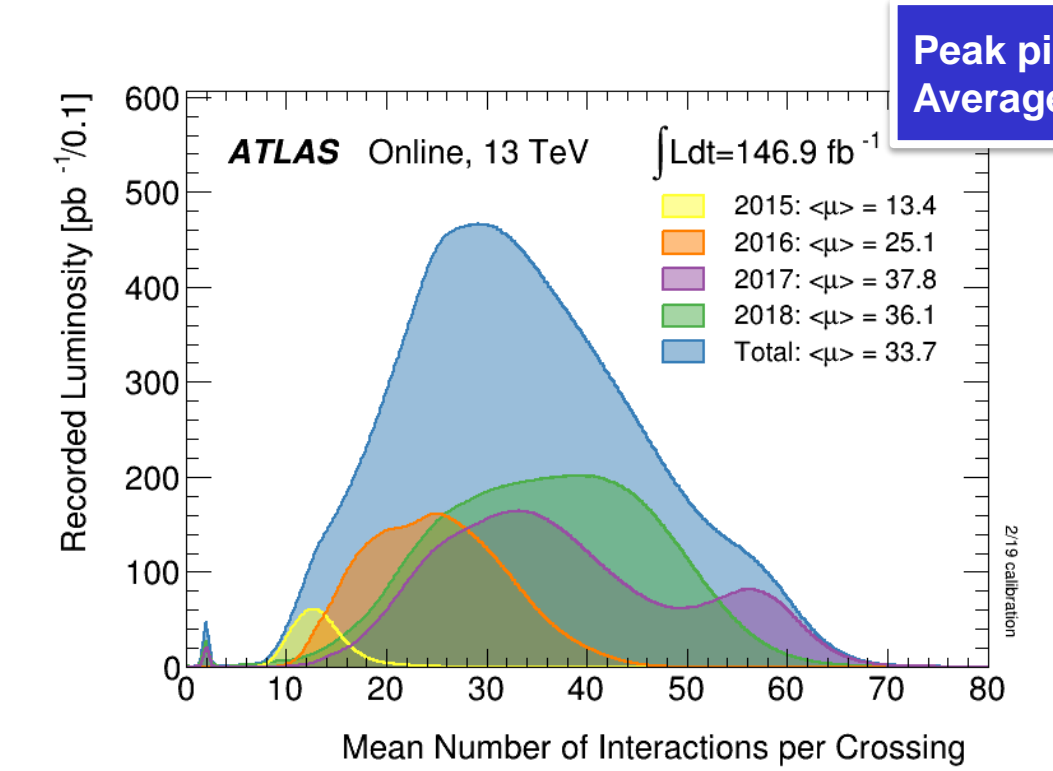


## LHC CONDITION



158 fb<sup>-1</sup> in Run 2  
65 fb<sup>-1</sup> in 2018

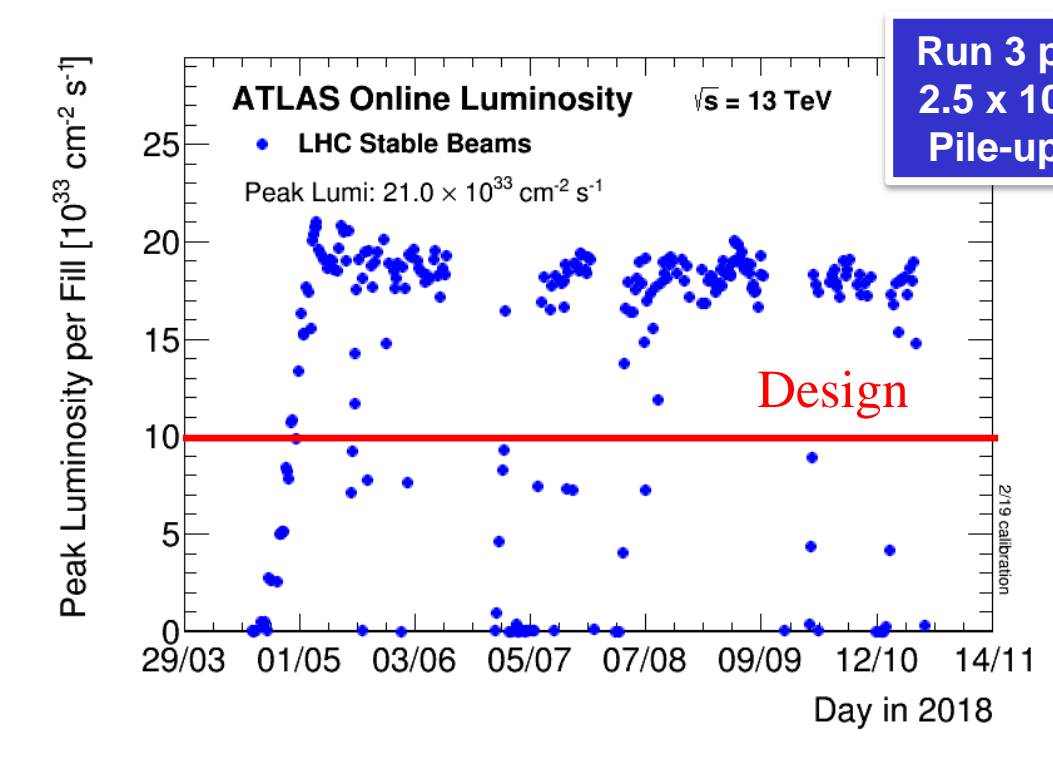
- The design conditions for the ATLAS Pixel Detector were overtaken during the Run 2
- Instantaneous peak luminosity  $L \approx 2 \times 10^{34}$  cm<sup>-2</sup> s<sup>-1</sup> and peak pile-up  $\mu \approx 60$  are abundantly above the nominal values ( $L_{\text{nom}} = 1 \times 10^{34}$  cm<sup>-2</sup> s<sup>-1</sup> and  $\mu_{\text{nom}} \sim 20$ )



Peak pile-up  $\mu \approx 60$   
Average (Run 2) - 34

- ✓ Pixel data taking over LHC Run 2 has been particularly challenging due to radiation level and number of tracks

- ✓ Big stress for hardware (Single Event Effects, damages in the FE chips and in the sensor bulk)

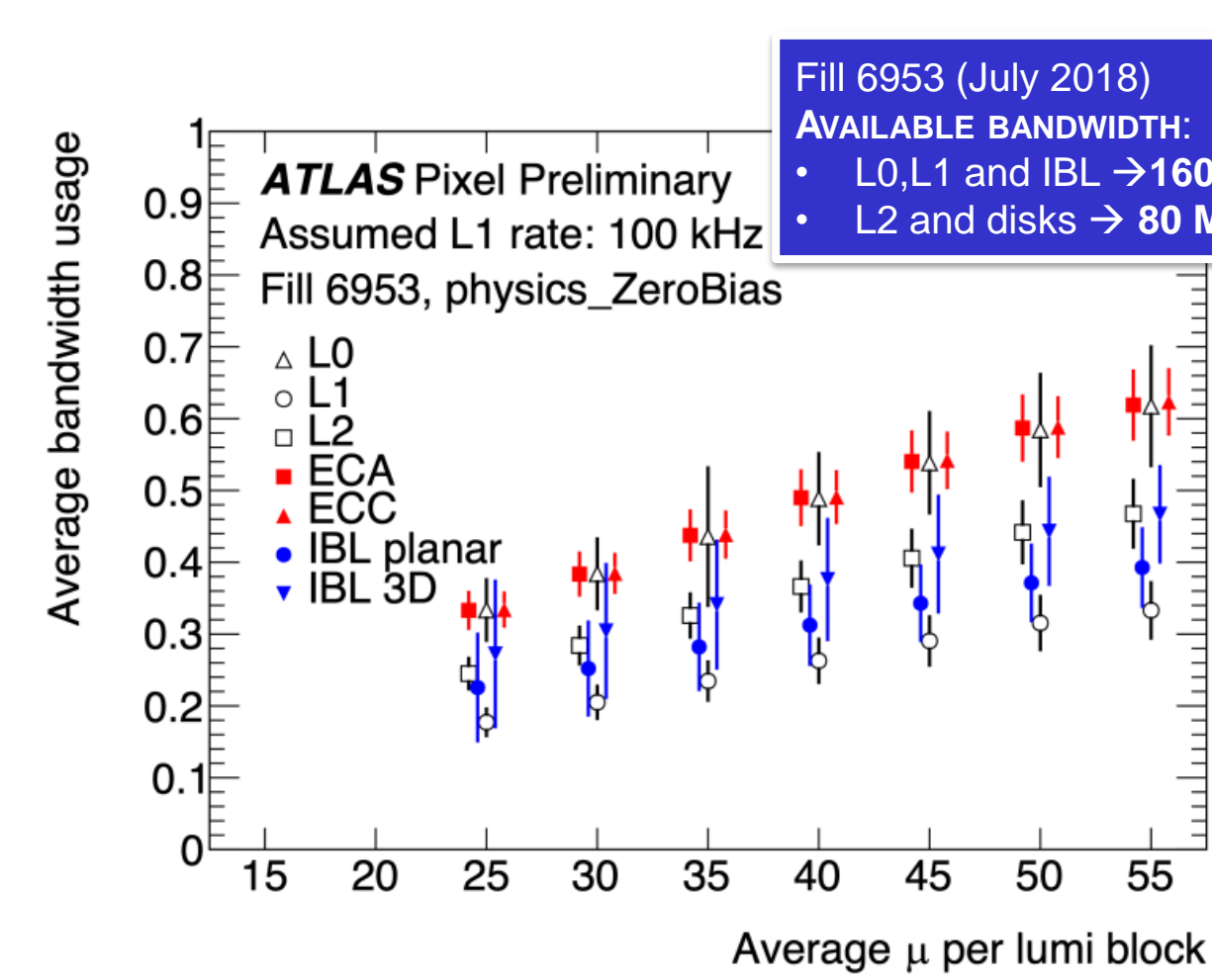


Run 3 prediction:  
2.5 x 10<sup>34</sup> cm<sup>-2</sup> s<sup>-1</sup>  
Pile-up:  $\mu \approx 61.5$

More than 11 years after its first installation in ATLAS and at twice the LHC design luminosity, the Pixel Detector is performing well.

By the end of Run 3, the expected delivered luminosity will reach  $\sim 400$  fb<sup>-1</sup>, a very impressive and challenging scenario for Pixel detector

## DETECTOR OPERATION

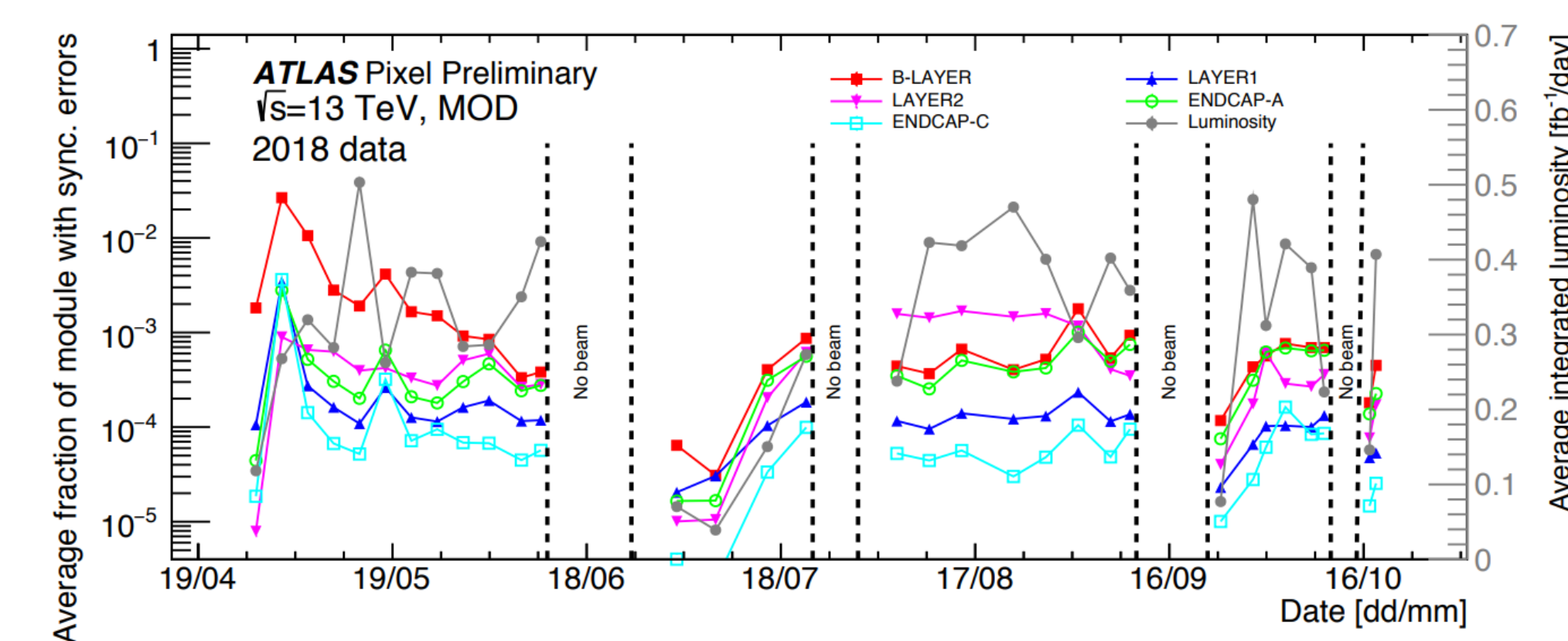
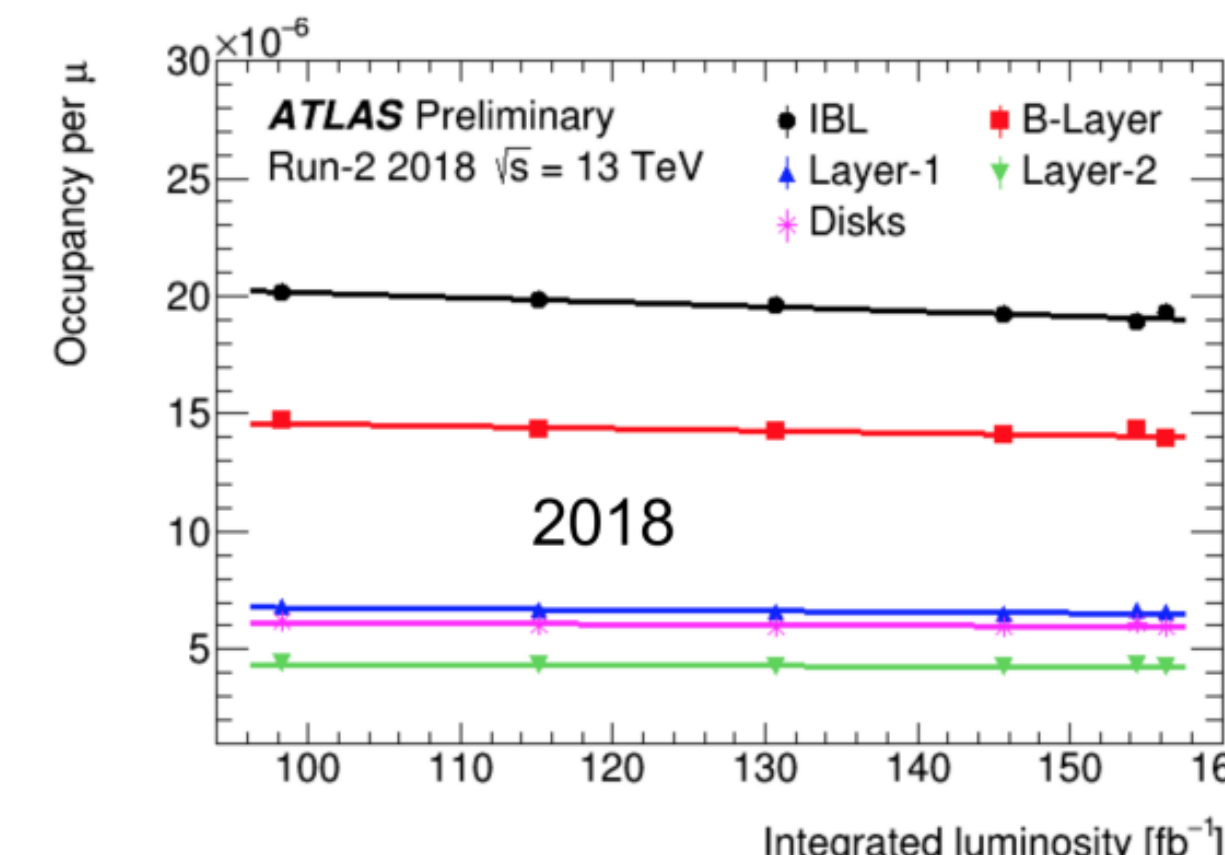


ATLAS Pixel Preliminary  
Assumed L1 rate: 100 kHz  
Fill 6953, physics\_ZeroBias

**GREAT STABILITY OF THE DAQ OF PIXEL DETECTOR**

- Bandwidth usage rises with rising pile-up  $\mu$   
→ Crucial attention to bandwidth saturation, buffer overflow
- Pixel hit occupancy (number of hits per pixel per event) per unit of  $\mu$  decreases due to radiation damage  
→ Thresholds were decreased for the first time in 2018
- Dead time and desynchronization issues reduced drastically since the begin of Run 2  
→ Pixel dead time below 0.2% by the end of 2018. Continuous improvements along the years of Read Out Driver (ROD) Fw and Sw

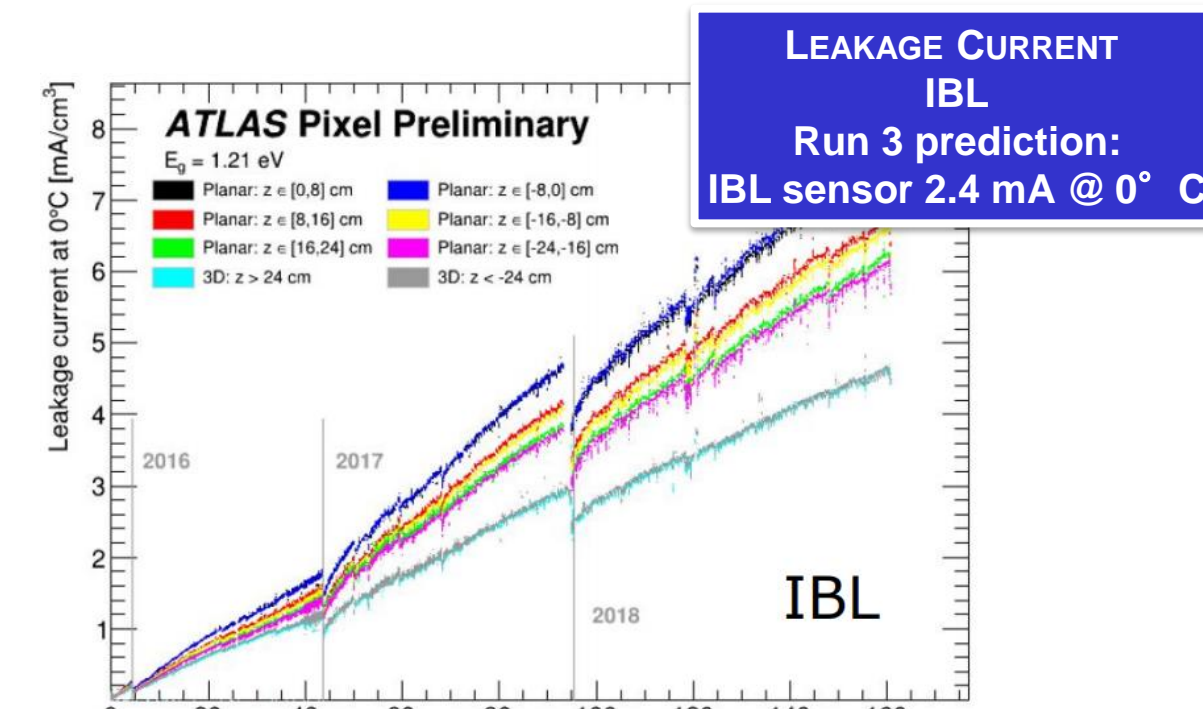
Further progress are foreseen in terms of data recovery/quality with the deployment of a ROD PowerPC (PPC) equipped with a custom Linux version in Run 3



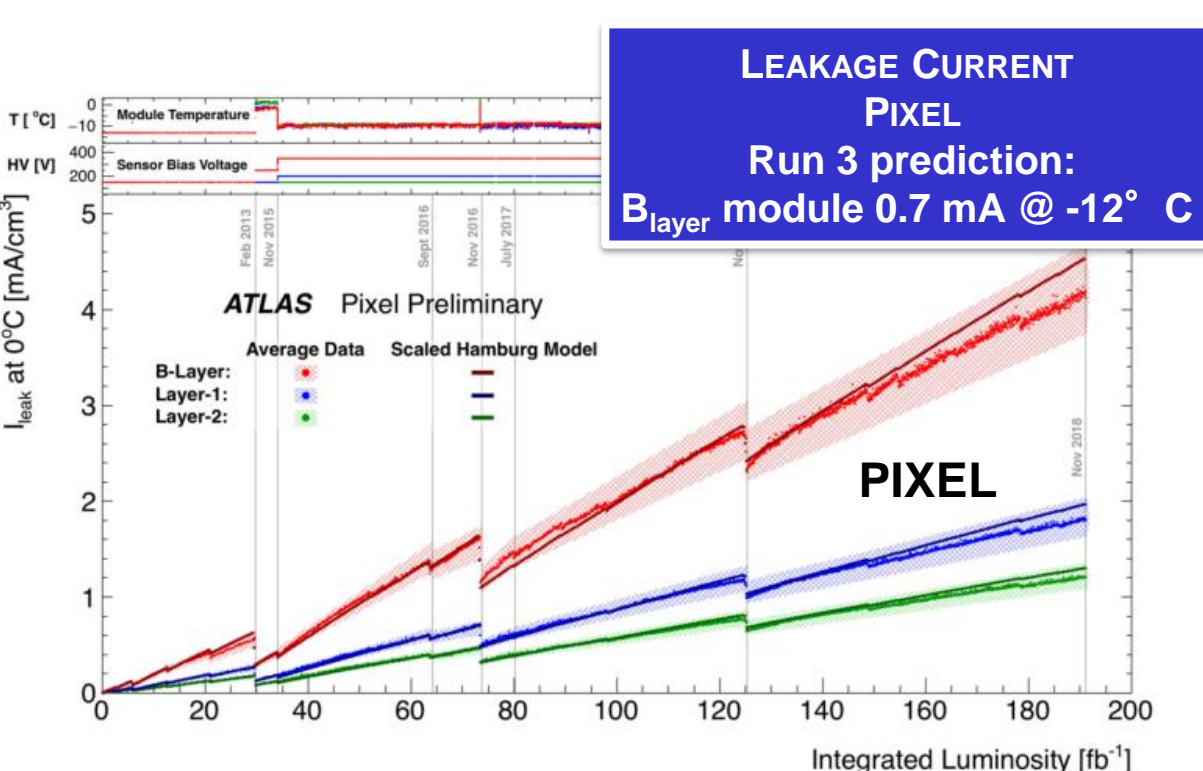
Average fraction of Pixel modules with any synchronization errors at the module level per event in 2018 runs

## EFFECTS OF RADIATION

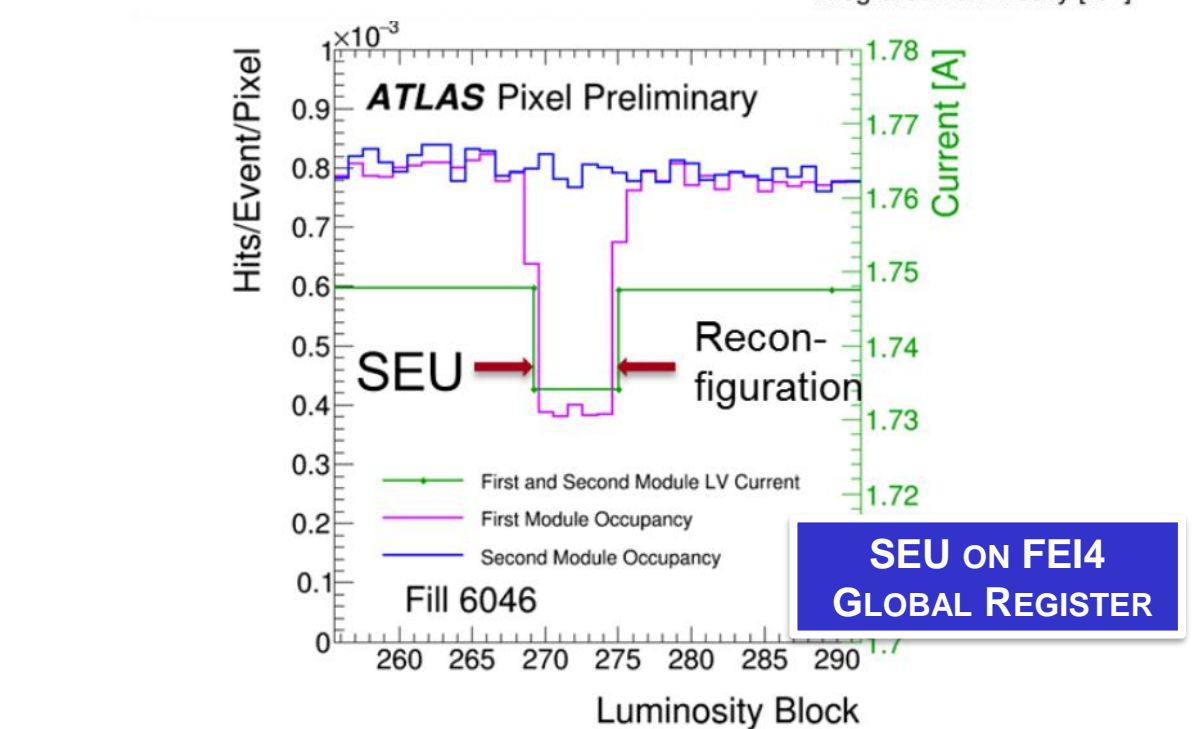
- Radiation damage changes the charge collection. This effect is stronger closer to beam pipe, so it is stronger for IBL
- Adjustment of thresholds, HV and temperature allows these effects to be contrasted
- The ATLAS measured leakage current grows linearly with delivered luminosity and it can be described quite well by the Hamburg Model, but scaling factor is however required
- The ratio of the leakage currents between layers remains quite constant
- Frontend chips of the ATLAS innermost pixel layer (IBL) experienced single event upsets (SEU) in local or global configuration registers.



LEAKAGE CURRENT IBL  
Run 3 prediction:  
IBL sensor 2.4 mA @ 0° C



LEAKAGE CURRENT PIXEL  
Run 3 prediction:  
B-layer module 0.7 mA @ -12° C

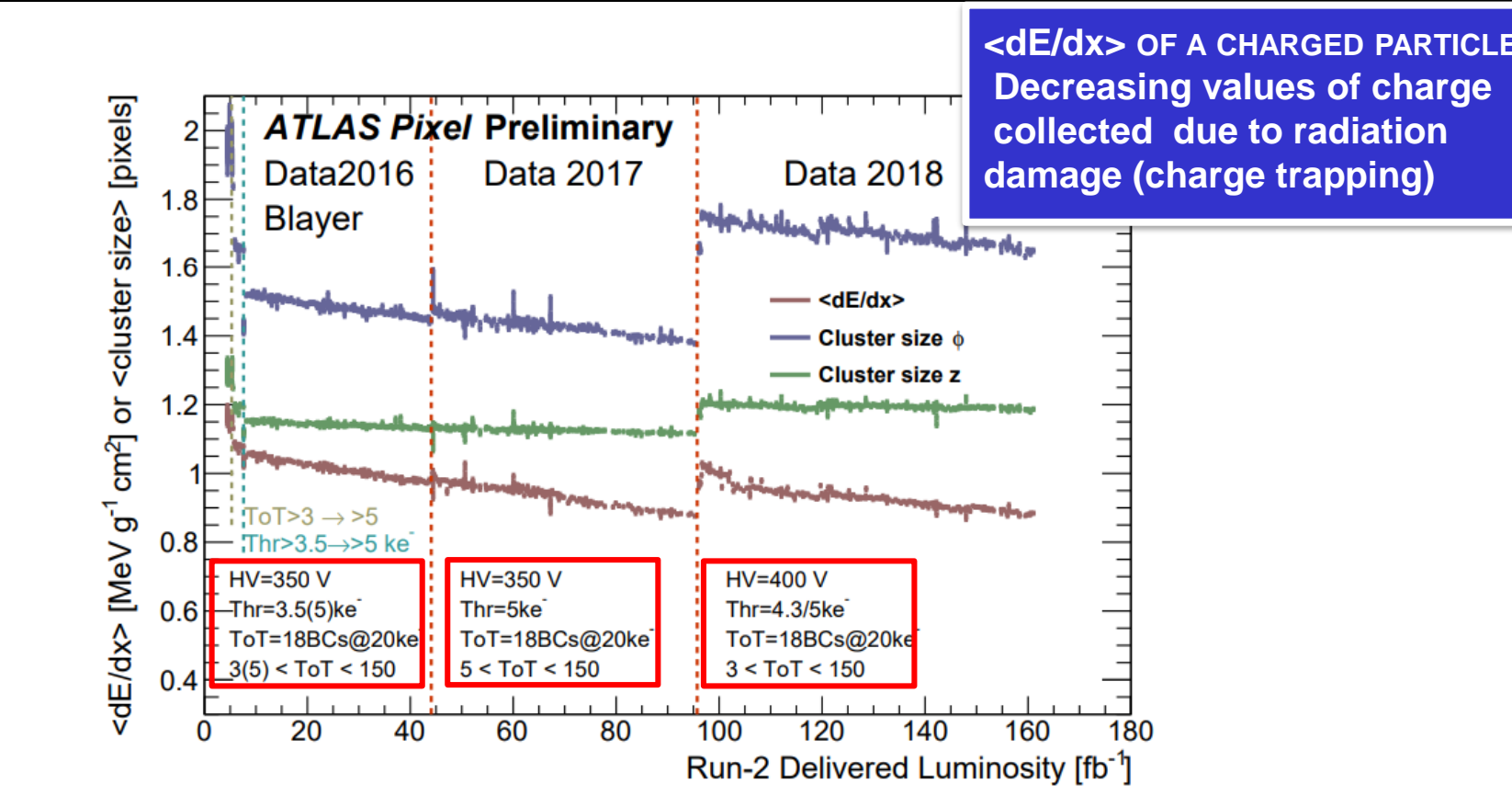


SEU on FEI4 GLOBAL REGISTER

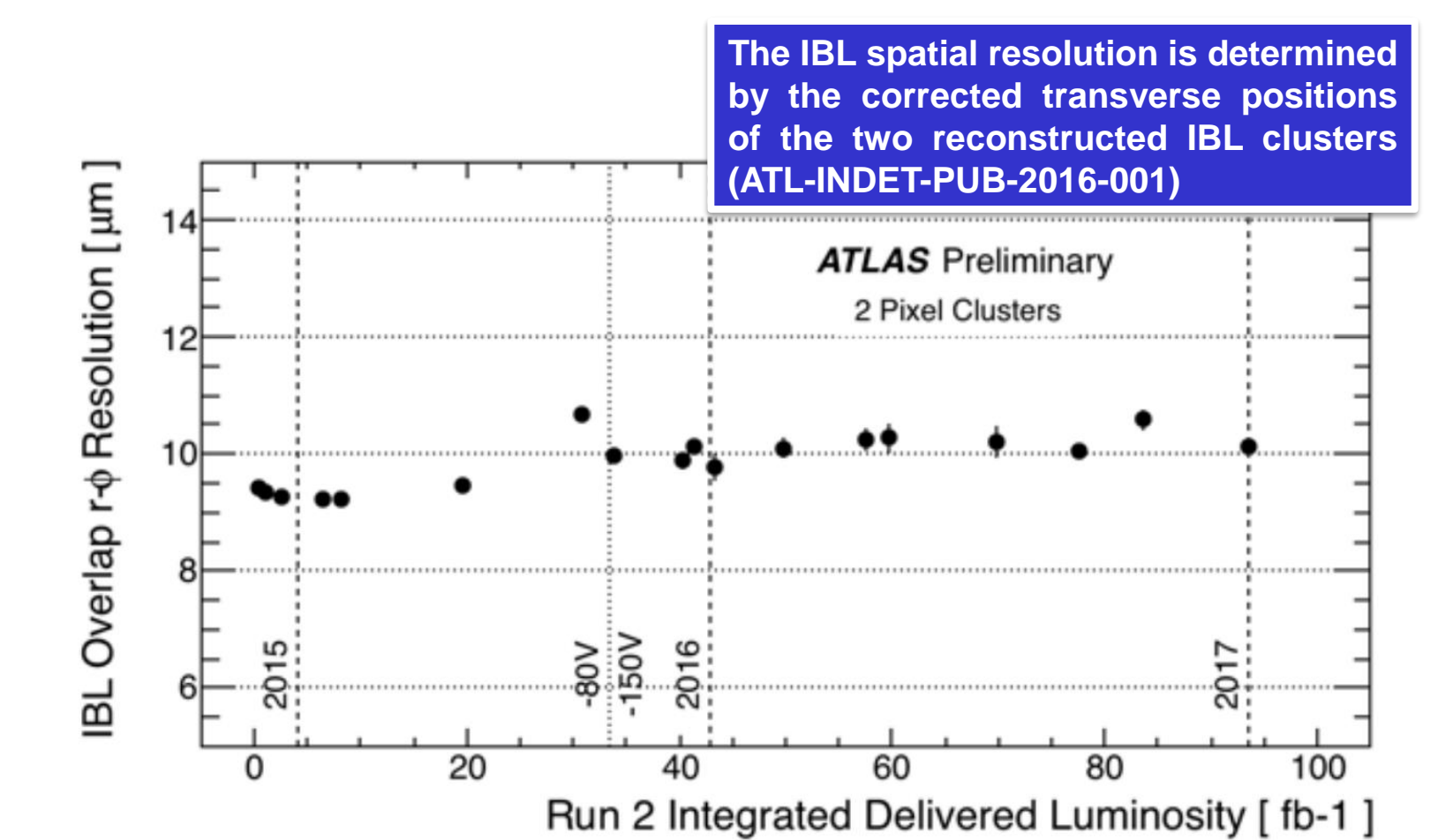
- EFFECTS ON FEI4 GLOBAL REGISTER**
- Step on LV current consumption of the FEI4 chip
  - Drop of the module occupancy
  - Lowering of the data taking efficiency due the timeout

- EFFECTS ON FEI4 SINGLE PIXEL REGISTER**
- Increase noisy pixels
  - Increase broken clusters and quiet pixels
  - No major impact on tracking performances

## DETECTOR PERFORMANCE



- Due to the decreasing charge collection efficiency the observed dE/dx decreases
- Spatial resolution stable despite increasing radiation damage → New radiation damage model presented (JINST 14 (2019) P06012 DOI: 10.1088/1748-0221/14/06/P06012)



B-Layer Hit-on-track efficiency above 98%

