Hardware production quality control for the ATLAS Phase-I readout upgrade
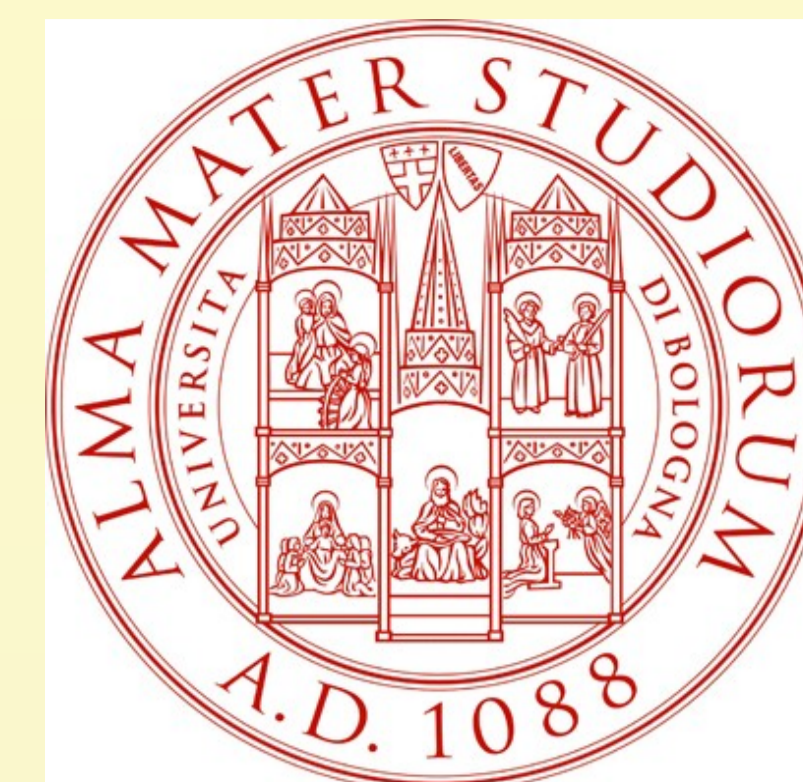
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on behalf of the ATLAS TDAQ Collaboration

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The upcoming upgrade of the readout system of the ATLAS experiment at the LHC at CERN is based on the Front-End LInk eXchange (FELIX) system. As part of this upgrade, approximately 120 custom PCIe cards are being produced by an industrial partner, based on a hardware design developed within the collaboration by several Institutes and Universities. Such a large production requires detailed Quality Assurance/Quality Control procedures (QA/QC) to ensure the hardware being produced is fully functional and robust.

FELIX project

The FELIX idea derived from the plan of using the radiation hardness CERN GBT data protocol as a single interface for detectors. A scheme of the FELIX infrastructure, which will be used to readout several upgraded ATLAS subsystems after the Long Shutdown 2, is shown in Fig. 1a. Figure 1b shows the custom FPGA based card called FLX-712, which is a central part of the infrastructure. The data transmission is based on 48 links tested at 9.6 Gb/s using the fastest serializer-deserializers available on the card. The FLX712 use two data protocols: the GBT (4.8 Gb/s) and the FELIX custom FullMode (9.6 Gb/s). An AN2814 clock and data recovery and a Si5345 jitter cleaner manage respectively the TTC input and the high quality clock for the high speed transmission in the FPGA.

Opto-electrical transduction performed by 8 devices called miniPOD, 4 in transmission and 4 in reception, clustering 12 links each one
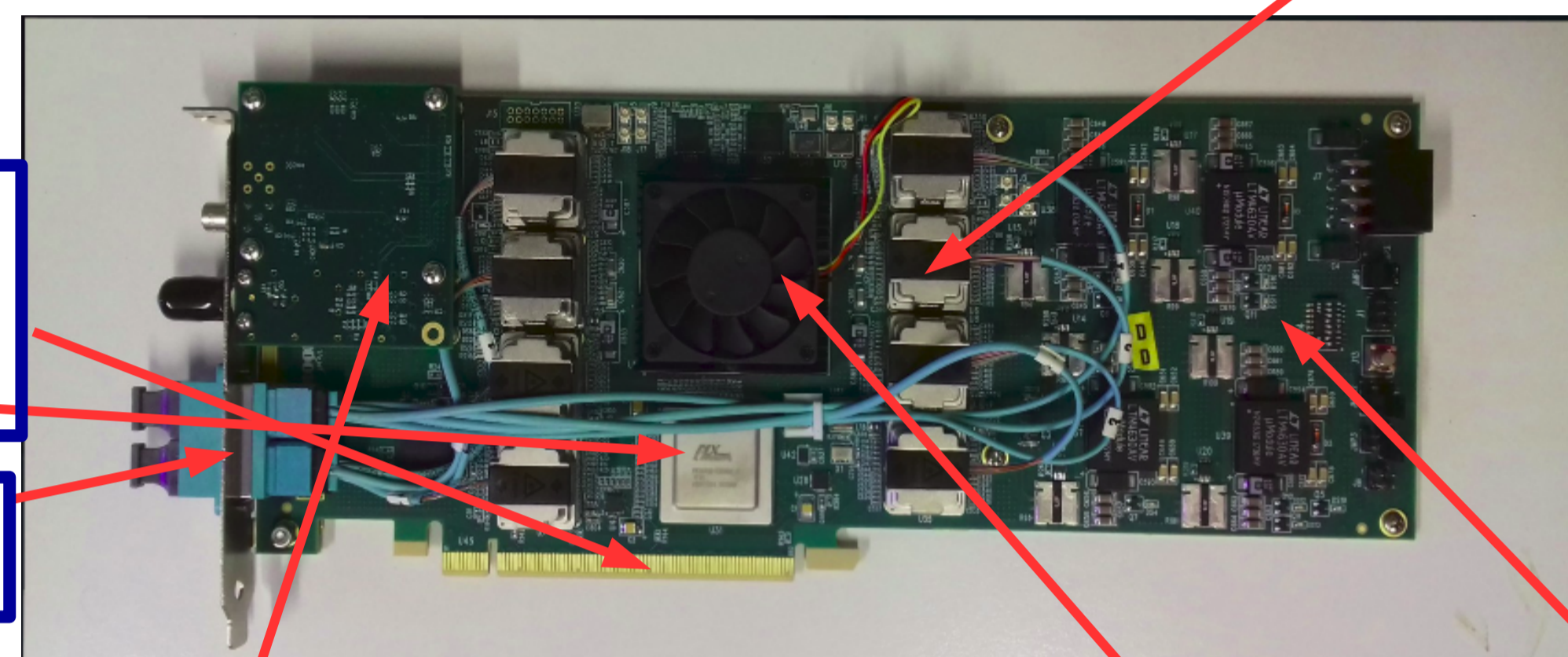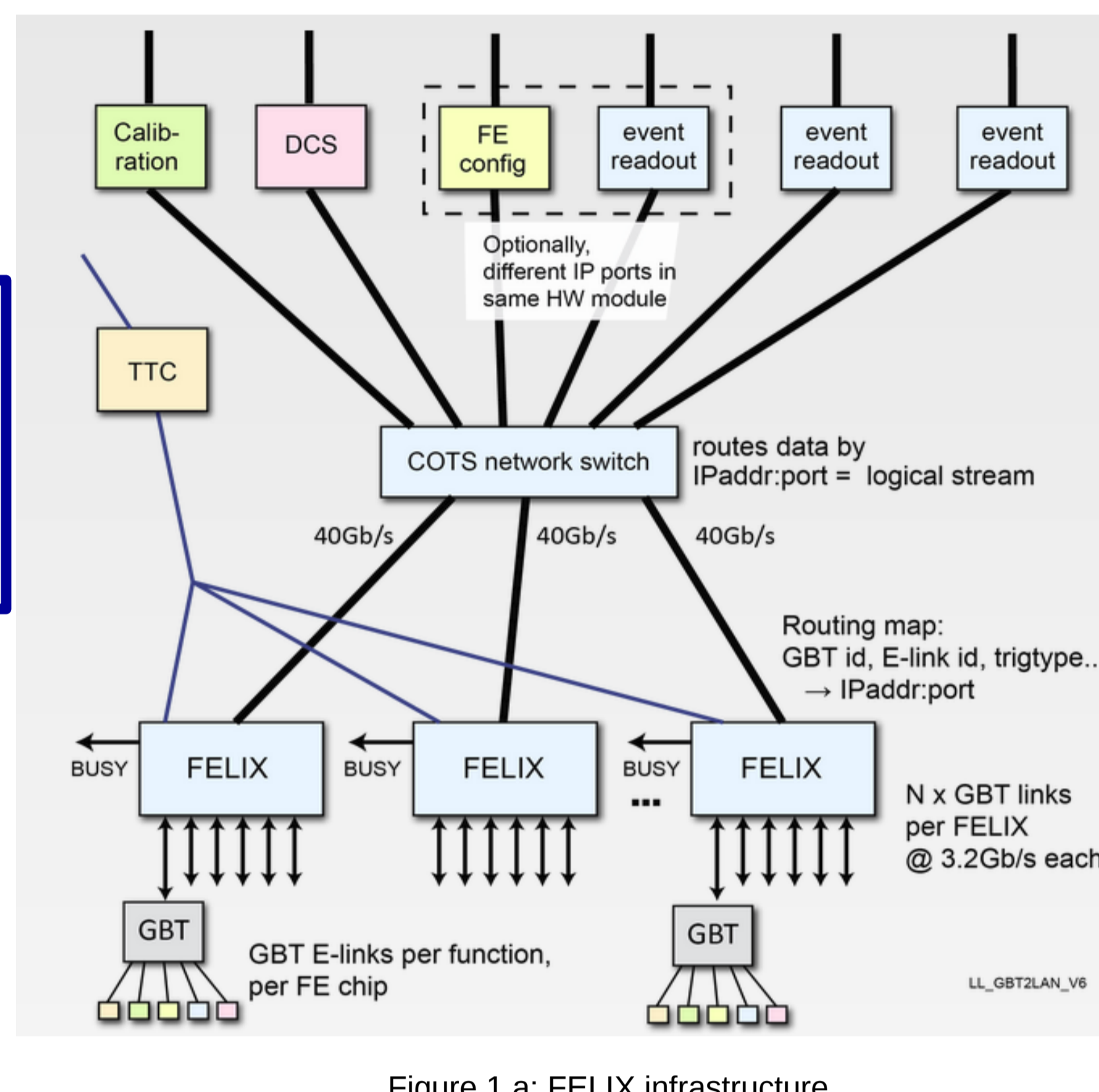
PCI Express Gen3 16 lanes managed in a 8x2 structure with a PCIe switch

Optical fibers as data input and output

TTC acquisition mezzanine

Figure 1.b: FLX-712 card

XCKU115 FPGA

16 stackup PCB

Figure 1.a: FELIX infrastructure

Tests setup

The motherboard used for the tests done after the mechanical assembly is a SUPERMICRO X10DRG-Q (shown in the Figure 2 below) with 5 available PCI Express Gen3 16 lanes connections, 2 CPU slots populated with 2 Intel Xeon E5-2660 v3 at 2.60 GHz. This configuration allows to manage 4 cards concurrently in the PCIe bus. The operating system used is Scientific Linux CERN 6. The system has been setup by the author with the support of the Bologna group. The required scripts to run all the tests have been prepared following the FELIX team requests, using the FPGA tools to study specific performance and the FELIX software to check the card functionalities.
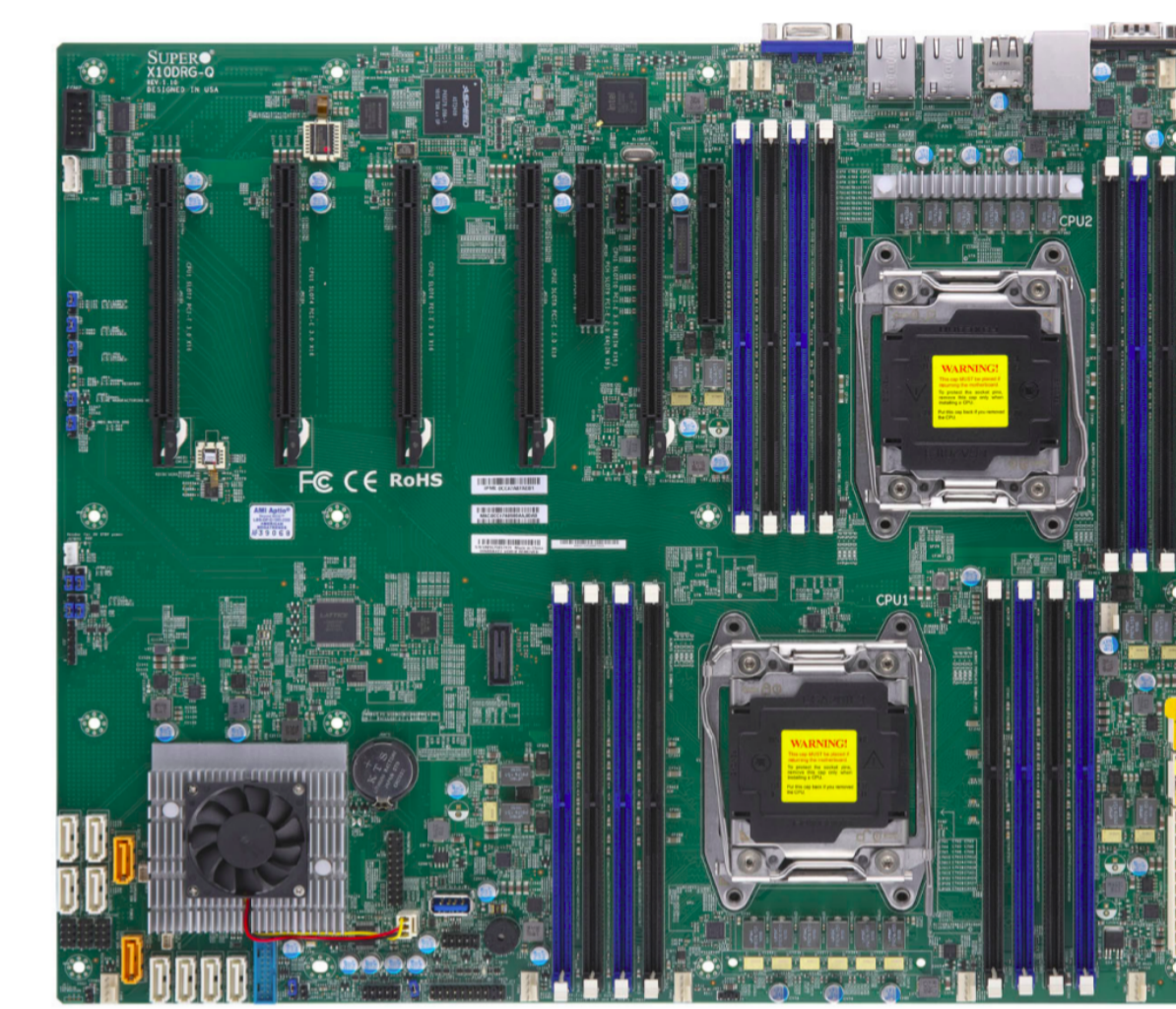
Figure 2: Test setup motherboard

ATLAS TDAQ Phase-I hardware validation tests

To ensure the quality of the FLX-712 cards after the production several checks and tests has been prepared. This test suit includes standard industrial tests and specific checks prepared by the FELIX group. These tests have been required due to the high complexity of the cards in terms of the standard needed for the PCB and the components used. The QA/QC is designed to ensure synchronism and quality of the high speed communications, firmware stability, functionality of the communication between the linux software tool commands and the cards through PCI Express.

AFTER PCB PRODUCTION

NADCAP — High quality standard in the PCB manufacture

INPUT QUALITY CONTROL OF ALL THE COMPONENTS — Check of the basic functioning of all the components before mounting them

= Contractor (standard industrial procedures)

= CERN (tests prepared by the FELIX group)

AFTER COMPONENTS MOUNTING

THERMAL CYCLE — 2 thermal cycles 0-to-100 °C 10-15 °C/min

AUTOMATED OPTICAL INSPECTION — Automated camera scans to search for several types of defects

BGAs X-RAYS

X-rays of the FPGA

FLYING PROBE — Mechanically controlled probe for PCB measuring operations

IMPEDANCE MEASURING — Impedance measuring of important passive components before and after power on

AFTER MECHANICAL ASSEMBLY

EYE DIAGRAM

BIT ERROR RATIO — Bits erroneous on total bits sent (required 10^{-13}) using a Pseudo Random Binary Sequence

GENERAL FUNCTIONALITIES — Test of the complete software functionalities of the cards as monitoring, firmware parameter configuration, software tools, etc..

VISUAL INSPECTION — Visual inspection of the card to check the cleaning, the quality of the soldering and of the mechancail assembly

BUSY OUTPUT CHECKING — Checking if the "busy" signal sent by the card is transmitted by the TTC card

JITTER CHECKING — Jitter measurements of several clocks in input and output (must be below 10 ps)

LONG TIME STABILITY — 8 hrs test to check long time stability

SLOW CONTROL — Checking the front-end communications for managing and reconfiguration

FIX LATENCY CHECKING — The propagation time of L1A signals to front-end must be Constant (~500 ns)

JTAG cable to program the FPGA

FLX-712

X10DRG-Q motherboard

Loopback optical cable for transmission and reception during tests

4U system

Figure 3 : Test setup for fully assembled cards

Summary and plans for the future

On December 2018 the Long Shutdown 2 started the ATLAS Phase-I upgrade. The FLX-712 electronic boards, developed by the FELIX group, will be used to readout many upgraded subdetectors such as the New Small Wheel. A new batch of FLX-712 cards has been produced and validated at the hardware level. The tests were all passed, showing the stability of the hardware design, which was the goal of these tests. Some minor modifications will be done to avoid rare events to occur. Problems occurred were about the firmware stability and the test PC capability to manage long time test. All these issues have been solved, demonstrating the efficiency of the firmware and the good choice of the hardware and software environment. The pre-series produced is made of 20 cards. Part of them has been delivered to the ATLAS subdetectors for deployment in their DAQ system an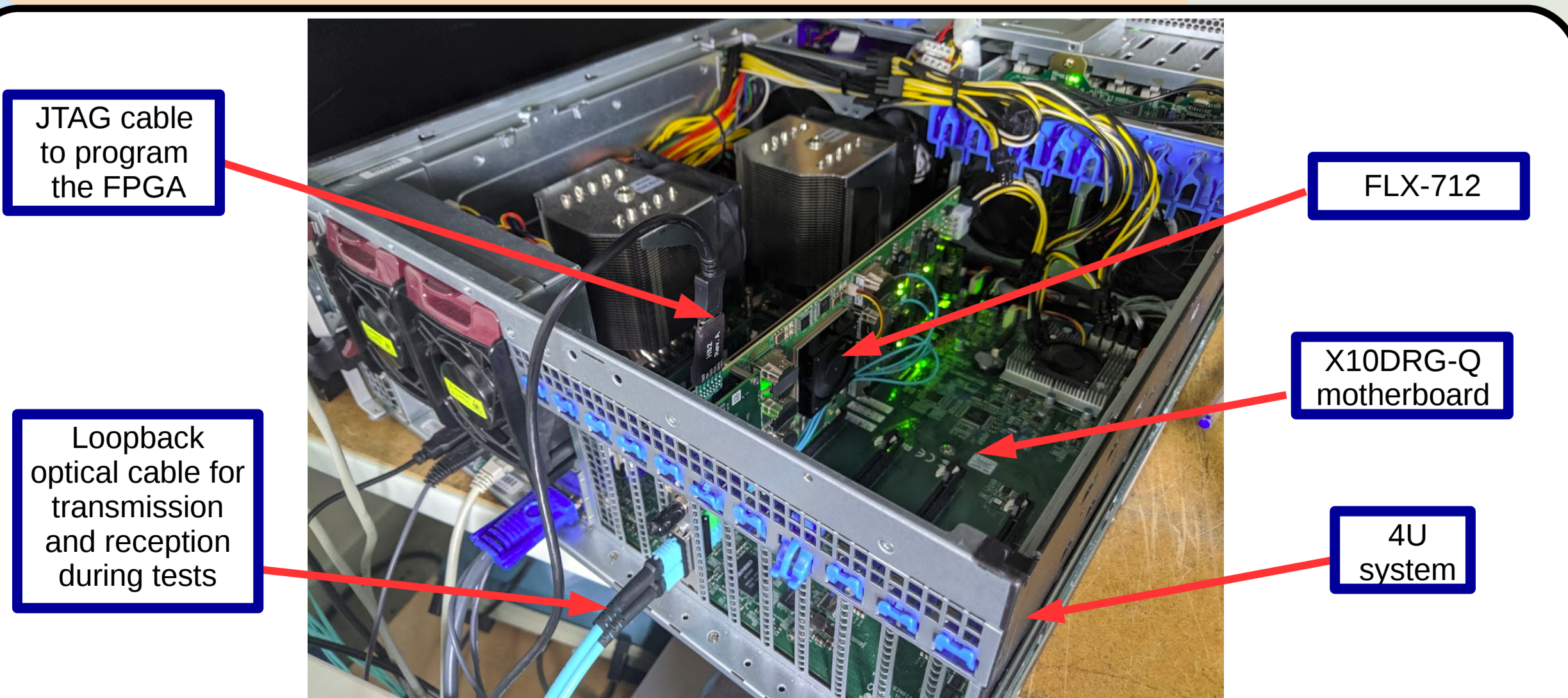d testing in the final environment.