Published by IOP Publishing for Sissa Medialab

Received: *March 18, 2019*
Revised: *July 1, 2019*
Accepted: *July 1, 2019*
Published: *July 16, 2019*

A monolithic ASIC demonstrator for the Thin Time-of-Flight PET scanner

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Abstract: Time-of-flight measurement is an important advancement in PET scanners to improve image reconstruction with a lower delivered radiation dose. This article describes the monolithic ASIC for the TT-PET project, a novel idea for a high-precision PET scanner for small animals. The chip uses a SiGe Bi-CMOS process for timing measurements, integrating a fully-depleted pixel matrix with a low-power BJT-based front-end per channel, integrated on the same 100 µm thick die. The target timing resolution of the scanner is 30 ps RMS for electrons from the conversion of 511 keV photons. The system will include 1.6 million channels across almost 2000 different chips. A full-featured demonstrator chip with a 3×10 matrix of 500×500 µm^2 pixels was fabricated to validate each block. Its design and experimental results are presented here.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Gamma camera, SPECT, PET PET/CT, coronary CT angiography (CTA); Timing detectors

ArXiv ePrint: 1811.10246

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https://doi.org/10.1088/1748-0221/14/07/P07013

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1 The TT-PET project

Conventional PET imaging techniques use scintillating crystals to detect two back-to-back photons produced by a positron-electron annihilation to determine where the annihilation occurred. Without additional information, the event is placed anywhere on the line of response between the two acquired signals and, with enough statistics, an accurate image can be reconstructed. The addition of a Time of Flight (TOF) measurement can restrict the initial placement of the interaction point on the line of response, reducing it to a segment. A more precise timing information corresponds to a shorter segment, resulting in a less noisy image, or in a reduced dose to the patient due to the smaller statistics required. In order to extract valuable information on the position of the annihilation point, a high TOF precision is required (at least 200 ps), as the particles travel at the speed of light.

Goal of the TT-PET (Thin TOF-PET) project is to build a novel small-animal PET scanner with a target of 30 ps RMS time resolution for photon detection [1]. This value is well beyond the state-of-the-art for time-of-flight PET systems [2], and is obtained by a radically different approach compared to traditional scanners. Multiple layers of monolithic silicon pixel detectors[1] and high-Z photon-converters are stacked to convert incoming photons and digitize hits, providing their 3D position and timing. Data are reconstructed off-line to correct for systematic offsets, discriminate coincidences and reconstruct the acquired image.

The TT-PET project is funded by the Swiss National Science Foundation. The front-end design was carried out by the University of Geneva and the INFN Rome Tor Vergata.

[1] Monolithic detectors are commonly used in High Energy Physics [3, 4], but have not been used yet for PET scanners.

2 System design aspects

The TT-PET scanner is formed by 16 identical wedges, called towers, containing the detector stack, the mechanical support structures, the cooling and the interconnections (figure 1). Each detection layer is composed by two 100 µm thick monolithic pixel silicon detectors placed side by side, a 50 µm lead converter and dielectric glue layers, as shown in figure 2.[2] Pixels have an area of 500 µm by 500 µm, which corresponds to an input capacitance for the Front-end of about 500 fF including routing.

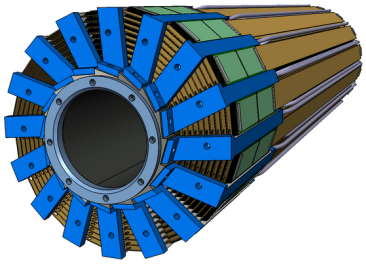

Figure 1. CAD image of the TT-PET scanner, with the 16 towers and the cooling blocks between them represented in blue. The wedge-shaped towers are formed by ASICs of three sizes, with larger ones at larger radii.

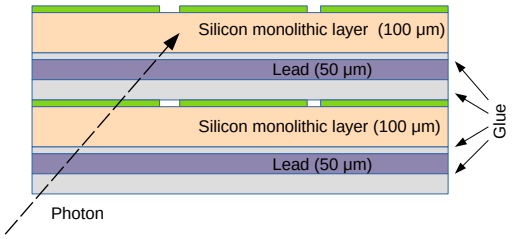

Figure 2. Two detection layers, including a monolithic detector, a lead converter and glue. The 60 detection layers of a tower are divided in 12 stacks of 5 layers each (called "supermodules"). The lead and silicon layers are glued together with 5 µm and 50 µm thick adhesive tape.

Detectors are grouped every 5 layers in a "super-modules", sharing services and interconnections. The chips in a super-module are all connected to the same flex cable with stacked wirebonds and are daisy-chained to minimize the number of connections needed for the readout.

Cooling is provided by a microchannel liquid flow in the blocks between the towers. This solution minimizes the dead area, but it can only dissipate a limited amount of power. Heat transfer simulations by FEA, confirmed by measurements on a mechanical mock-up, were used to calculate the power budget of the detectors, which was set to 200 µW per channel [6].

Three different chip sizes (25 mm long and 7, 9 or 11 mm wide), are foreseen to form wedges. The number of chips was optimized with GEANT4 simulations that simulations that made it possible to calculate the scanner sensitivity and efficiency.

3 The TT-PET small-size demonstrator chip

After some small-scale test structures, a 3×10 matrix of fully-featured pixels (shown in figures 3, 4 and 5) was submitted in a MPW run in Spring 2017. The chip has been fully characterized with radioactive sources and in the SPS beam test facility at CERN [7].

Each of the 500 µm × 500 µm pixels includes a BiCMOS preamplifier, a fast discriminator and an 8-bit calibration DAC for threshold equalization, placed in a column next to the active collection

[2] A more comprehensive explanation of how the multi-layer structure works can be found in [5].

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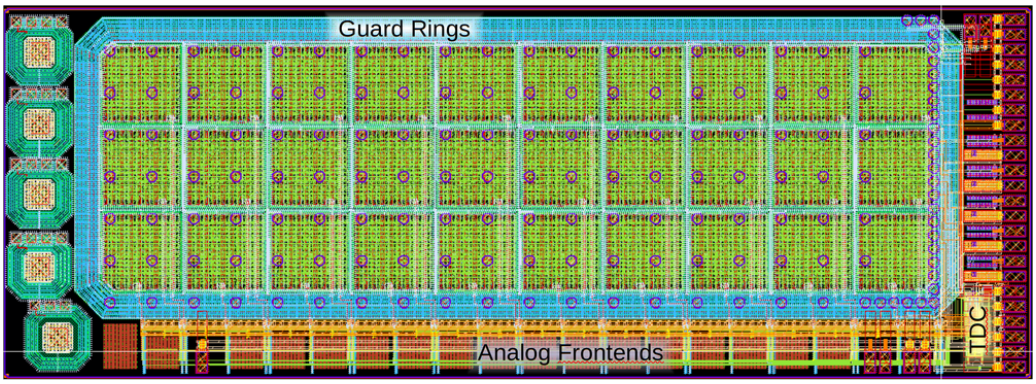

Figure 3. Layout of the TT-PET demonstrator chip, with a 3×10 pixel matrix. The pixel diodes are clearly visible (in green) as they occupy the vast majority of the available area. Each pixel is connected to a front-end (preamplifier, discriminator, calibration DAC) placed outside of the matrix (on the lower edge in the figure). The TDC and the readout logic are placed close to the wire-bond pads, on the right. On the left, five guard-ring test-structures are visible, that were submitted to independently test the high-voltage insulation of the pixels.

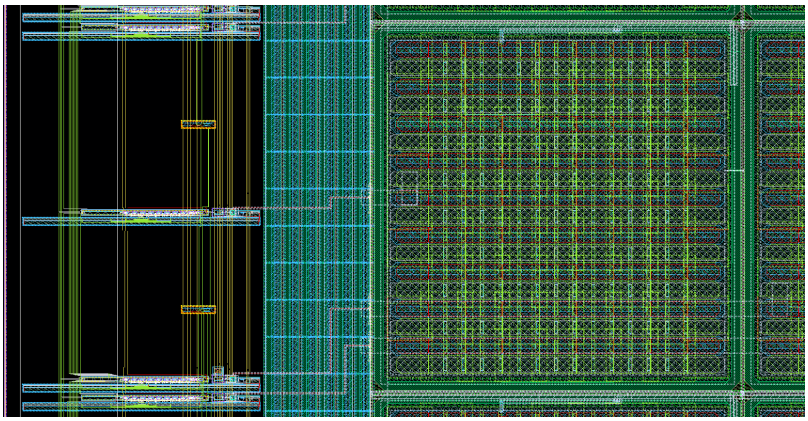

Figure 4. Closeup of the layout of a pixel. The active area is on the right, with a large capacitor made using the routing metals on top. This capacitor is connected to the analog front-end (on the left) which is separated from the pixel with a series of 8 guard-rings.

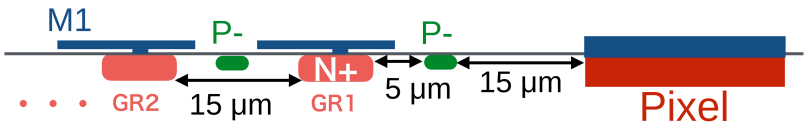

Figure 5. Cross-section of the active area, including two of the 8 consecutive guard-rings that isolate the high-voltage part of the chip from the front-end electronics.

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area. In the periphery a single TDC is used to digitize timing information, with all the pixels multiplexed to it. A digital logic block encodes the digitized data along with the hit position and implements a simple I/O protocol for chip readout and configuration. Other blocks include tunable biasing structures for the analog circuits. A block diagram of the pixel electronics can be found in figure 6.

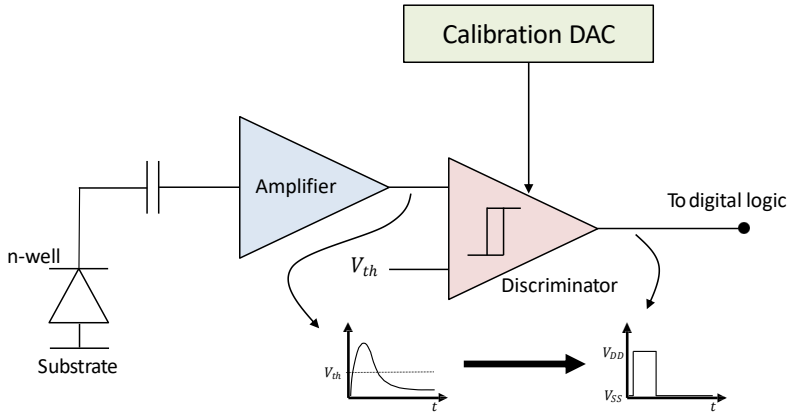

Figure 6. Block diagram of the pixel electronics. The pixel is shown as a diode, connected to the BJT-based preamplifier. Its output is discriminated by an open-loop MOS amplifier, controlled by a local DAC to adjust its threshold. The digitized output is sampled by a latch and sent to the periphery to the TDC.

3.1 Specifications

The main specifications for the front-end are shown in table 1.

Table 1. Main specifications of the simulated analog front-end for a 500 fF input capacitance. The disparity between the expected and measured gain is due to a well-to-well capacitance in the layout which was not correctly extracted by the simulation tool.

Power supply	1.8 V
Gain (simulated)	90 mV fC^{-1}
Gain (measured)	40 mV fC^{-1}
Equivalent Noise Charge (for a 1 pF input capacitance)	600 e^-
Minimum threshold	0.4 fC
Power consumption	135 µW
Peaking time	1.3 ns
Simulated ToA jitter (for a 1 fC signal)	82 ps

The pixel size is a compromise between input capacitance and power consumption. Having smaller pixels would lead to better spatial resolution of the scanner, but since a PET image has an intrinsic resolution of about 500 µm[8], the image quality would not improve. A smaller pixel would result in a smaller input capacitance for the amplifier, and thus lower noise, leading to more accurate timing. On the other hand, more channels would be required to cover the same area, so power consumption would increase.

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Noise is the main contributor to the timing resolution. Given an accurate enough TDC (TDCs with precision of a few ps can be found in literature [9]), the uncertainty is dominated by the effect of the analog front-end. This includes different factors, such as the pixel-to-pixel threshold variation, the intrinsic electronic noise of the preamplifier and the distribution of charge collection time in the substrate.

3.2 Front-end design

The front-end features a preamplifier using a Silicon-Germanium Heterojunction Bipolar Transistor (specifically, IHP 130 nm SiGe-HBT BiCMOS technology), which was chosen to minimize the series noise which represents the main contribution to the noise performance. [10]. This front-end was already tested and found to perform well, with the capability of achieving a 100 ps jitter for up to 1 pF input capacitance [11].[3]

The amplifier is connected to the input diode, which is integrated in the electronics substrate. The chip has a 1 kΩcm substrate and is thinned to 100 µm in order to optimize the charge collection time and increase the electric field uniformity. Ground reference is provided to the cathode through a back-plane metalization, while the anode is capacitively coupled to the front-end input. Figure 7 shows the I-V characteristic of the pixel matrix up to a voltage of 200 V. Full depletion is achieved at about 45 V. The leakage current is less than 0.6 nA per channel, making its contribution to shot noise negligible, and it is mostly due to the implantation process performed on the backplane. Since the front-end is capacitively coupled to the sensor, the dark current is filtered out and it has a negligible impact on the chip performance.

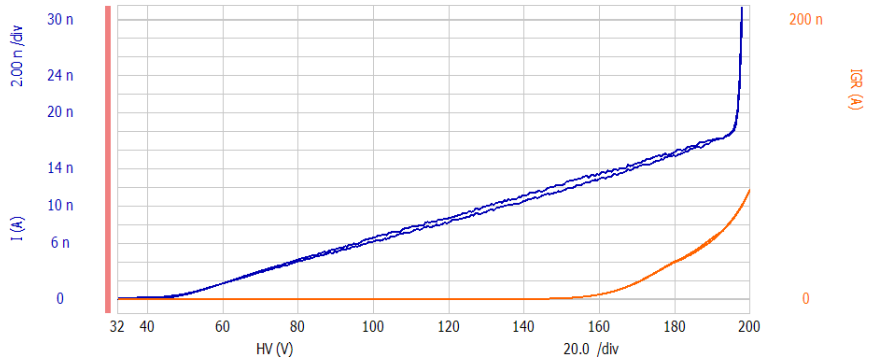

Figure 7. I-V curve of the 3×10 pixel matrix, connecting the backplane to ground and HV through a resistive distribution network. The current going through the diode is in blue (measured when both increasing and decreasing the voltage to show the hysteresis), while the current flowing through the guard ring is in orange. The resistive effect shown is due to the non-ideal ground contact through the chip backplane.

The preamplifier schematic is shown in figure 8. The BJT is used in a simple common-emitter configuration, with an active PMOS load and a MOSFET feedback emulating a large resistor [12], which can be tuned to adjust the equivalent feedback impedance.

[3]This value is compatible with the target of 30 ps for 511 keV photons [5]. Detailed GEANT4 simulations showed that the average charge deposited by a PET photon would be more than three times larger than the one deposited by a minimum ionizing particle. This target depends on the absence of second-order effects that are negligible compared to the expected front-end jitter for MIPs, but that could limit the time resolution for higher energies.

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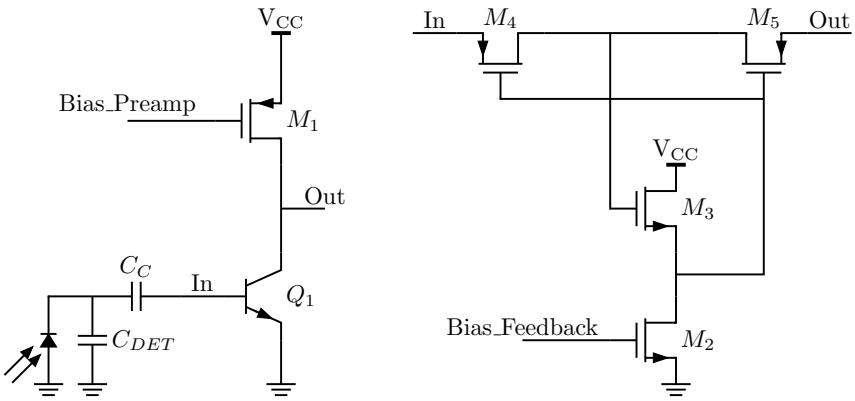

Figure 8. Schematics of the preamplifier. The left block is a common-emitter configuration capacitively coupled to the sensor through a metal capacitor of about 5 pF covering the entire pixel area, while the right one emulates a floating MOS-based feedback resistor which can be tuned from the periphery with a current DAC.

The choice of a common-emitter configuration comes from the need to minimize the input and output capacitances to achieve a high gain while keeping the rise time as short as possible. Indeed, the time resolution is directly proportional to the rise time and inversely proportional to the signal-to-noise ratio [13]. This implementation features a 20%-80% rise time of about 600 ps. Total charge integration time is about 1.3 ns, which is compatible with the charge collection time in silicon. A plot of the simulated output of the preamplifier is shown in figure 9. Due to the much larger peaking time compared to the target time resolution, time walk must be taken into account and compensated when calculating the time of arrival because different input charges can change the time stamp by hundreds of ps, as shown in figure 10. This is possible by estimating the charge performing a time-over-threshold measurement and then correcting the time-walk error off-line. Figure 11 shows the Equivalent Noise Charge referred to the input of the preamplifier for different values of input capacitances.

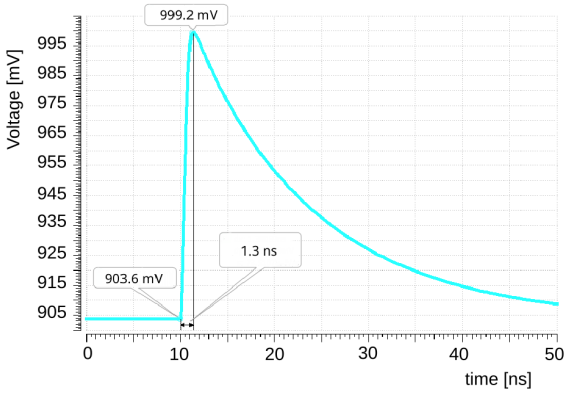

Figure 9. Typical output of the preamplifier for an input charge of 1 fC, extracted from a Cadence Spectre simulation. The most probable value for the deposited charge for a MIP is 0.91 fC[7].

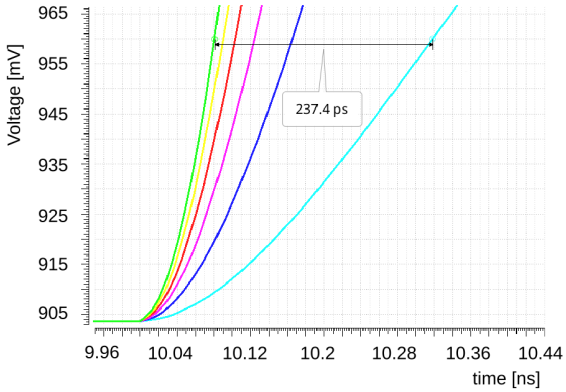

Figure 10. Effect of time-walk on the measurement, showing the difference in timing for different input charges, ranging from 1 to 20 fC.

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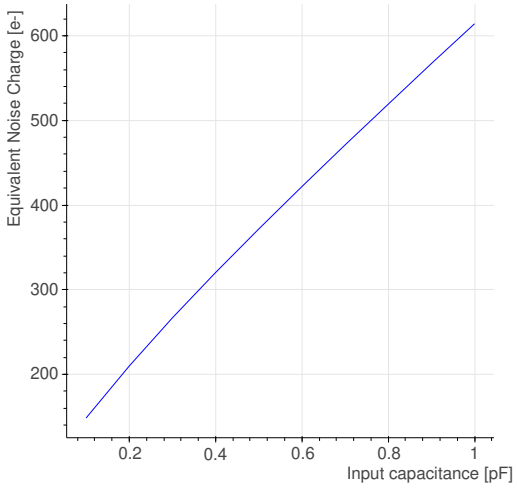

Figure 11. Simulated Equivalent Noise Charge of the preamplifier as a function of the input capacitance of the detector. This plot doesn't include the contribution of the discriminator.

Each preamplifier is connected to a 3-stage MOS discriminator with a 4 mV hysteresis to compare its output with a fixed threshold. In order to minimize the load capacitance of the amplifier the input stage of the discriminator uses very small NMOS transistors, leading to a significant pixel-to-pixel threshold mismatch (simulations showed a $\pm 3\sigma$ range of 100 mV that needs to be corrected). To compensate for this effect, an 8-bit calibration DAC is included in each front-end. It is a binary-weighted, current-steering DAC connected to the first stage of the discriminator that is used to unbalance the current flowing in the two branches and moves the effective threshold of the discriminator. This can compensate for other pixel-to-pixel effects, due for example to the DC output of the preamplifier. The total current produced by the DAC can be tuned to change the calibration range.

3.3 Readout logic and other blocks

A block diagram of the readout logic of the chip is shown in figure 12.

Given the low hit rate that we expect in any of the TT-PET chips, all pixels are multiplexed to the same TDC, so that the chip will not be able to detect simultaneous particles. Since this event is very rare [5], this approach was chosen to simplify the design and reduce the power consumption of the chip. A single 50-ps binning TDC is placed in the chip periphery and all pixels are connected to it through a balanced multiplexing ladder. The TDC measures both time of arrival and time over threshold of the signal, used to compensate for time-walk effects. A separate set of row and column lines are used to extract the pixel address and store it in a readout buffer. Pixel-to-pixel delay, while minimized by the balanced multiplexing network, is still larger than the time resolution, so it requires off-line calibration. The contribution to the time resolution of the digital chain was measured using a testpulse injection circuit and found to be in the order of 1 ps.

The chip features a simple serial interface for both readout and programming, with data shifted in the pixel configuration memories being connected as a long shift register. Since the chip can only store a single hit at a time, there is a dead time of about 5 µs (this value is much lower than the expected time between events) after every hit to allow for the readout of the TDC data. A trigger

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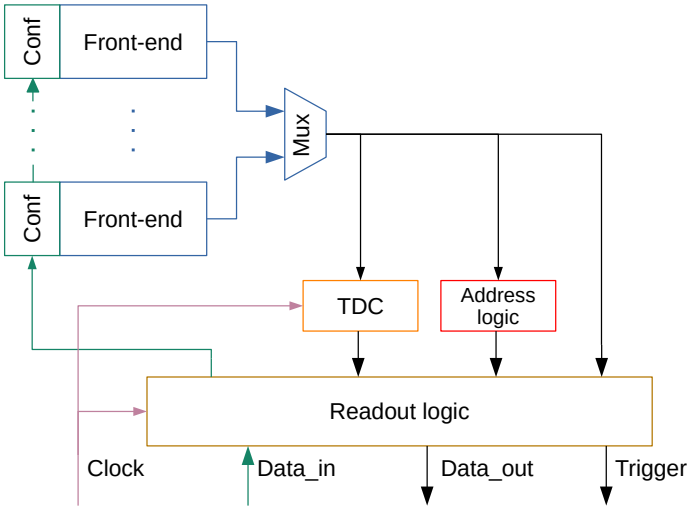

Figure 12. Block diagram of the readout logic. All the pixels in the matrix have their output multiplexed and measured by a TDC, while a separate circuit calculates and stores the address of the hit. An asynchronous trigger signal is provided to let the DAQ know when the chip was hit. A simple serial I/O interface is implemented to read out data and to load the pixel configuration.

signal, produced by a fast OR of all the pixels, is also available in output to implement a trigger logic or for debugging purposes.

4 Results

The demonstrator chip was thoroughly tested with a ^{90}Sr source at the University of Geneva. For testing purposes the inclusion of a fast trigger signal was very useful as it made it possible to characterize and debug the pixel front-end and the TDC separately. The chip is fully working at the nominal power consumption.

Time-of-flight measurements were performed with a ^{90}Sr source. Two chips were put on top of each other and time differences between them recorded and analyzed. The time-of-flight distribution between the two chips is shown in figure 13, fitted with a double Gaussian in order to exclude hits coming from the edges of the chip.[4] The measured time resolution of 130 ps for the core of the distribution is a very promising result, far better than what was previously achieved by monolithic particle detectors (for example [14]).

Combined simulations of the sensor and the electronics showed an expected resolution of 92 ps[5]. The larger measured value can be attributed to a non-ideal correction for time-walk and to an added input capacitance due to pixel routing, in addition to possible system-level cross-talk from the readout system.

The same demonstrator chip has also been characterized at the SPS beam test facility at CERN, showing similar results to the ones obtained with a ^{90}Sr source [7]. In that context the chip was also operated at different operating conditions in terms of power supply and bias currents.

[4]This cut would not be required if accurate hit tracking was available, as in [7].

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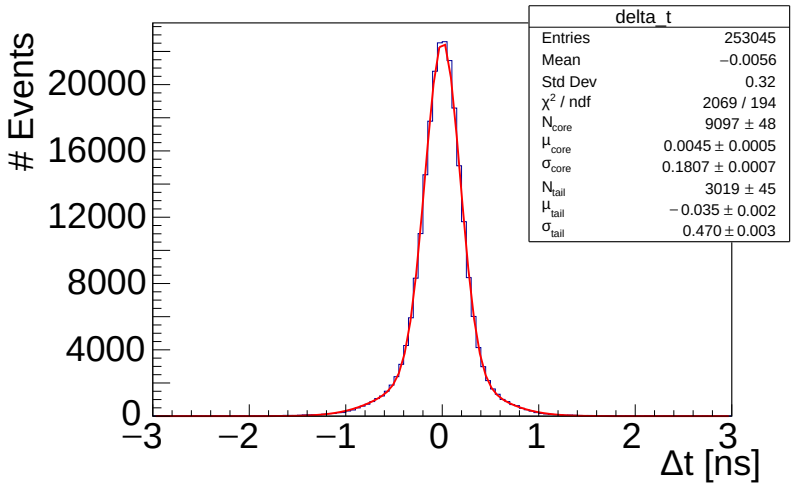

Figure 13. Time-of-flight distribution between two chips obtained with a ^{90}Sr source. This distribution is fitted with a double Gaussian; the standard deviation σ_{core}=180±0.7 ps hints to a time resolution of approximately 130 ps, assuming equal performance for the two chips. This measurement was taken with a threshold of about 3000 e^- (to have no noise hits) at the nominal power consumption of 135 µW per channel, averaging all the pixels.

5 Conclusions

The design of the demonstrator of a monolithic pixel detector for the TT-PET project was presented, together with test results. The chip includes a novel SiGe BiCMOS-based front-end to achieve better than state-of-the-art time resolutions. A time resolution of 130 ps was measured with a ^{90}Sr setup, with a power consumption as little as 135 µW per channel.

Acknowledgments

We would like to thank the Electrical Engineering team of the University of Geneva as well as the colleagues of the University of Bern and INFN Tor Vergata for their help with the readout system. This study was funded by the SNSF SINERGIA grant CRSII2_160808.

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