AIDA-2020-MS96

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

Milestone Report

Test report of deliverable D4.2

De la Taille, Christophe (CNRS)

28 February 2019

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

This work is part of AIDA-2020 Work Package **4: Micro-electronics and interconnections**.

The electronic version of this AIDA-2020 Publication is available via the AIDA-2020 web site <http://aida2020.web.cern.ch> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-2020-MS96>

Grant Agreement No: 654168

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDA-2020

MILESTONE REPORT

TEST REPORT OF DELIVERABLE D4.2

MILESTONE: MS96

Document identifier:	AIDA-2020-MS96
Due date of deliverable:	End of Month 46 (February 2019)
Report release date:	28/02/2019
Work package:	WP4: Micro-electronics and interconnections
Lead beneficiary:	CERN
Document status:	Final

Abstract:

The large-scale 130 nm CMOS integrated circuit HGCROC1 designed to read out high granularity silicon calorimeters was fabricated and extensively tested since its delivery at the end of 2017. The HGCROC1 chip is the main item of Deliverable D4.2. The experimental results for HGCROC1 are good and provide the basis for the design of the full scale high granularity silicon calorimeters readout chips for CMS at the High Luminosity LHC.

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 5 years.

Delivery Slip

	Name	Partner	Date
Authored by	Christophe de La Taille	CNRS	15/02/2019
Edited by	S. El yacoubi	CERN	25/02/2019
Reviewed by	D. Bortoletto [Deputy Scientific Coordinator]	UOXF	28/02/2019
Approved by	D. Bortoletto [Deputy Scientific Coordinator]		28/02/2019

TABLE OF CONTENTS

1. INTRODUCTION 4
2. 130 NM CMOS CALORIMETER READOUT CHIP HGCROC1 4
3. HGCROC1 TEST RESULTS 6
4. CONCLUSION 8
5. REFERENCES 9

Executive summary

A large scale 130 nm CMOS chip called HGCROC1, with 32 channels of preamplifier, shaper, ADC, TDC and high speed readout was designed for the readout of high granularity calorimeters described in WP13 and WP14. The HGCROC1 chip is the main item of Deliverable D4.2. After fabrication, the chip was delivered in December 2017. A long testing campaign was carried out by several institutes with the goal of understanding the chip performance before and after irradiation. The successful results confirm the suitability of the 130 nm CMOS process and of the analog and digital architectures that were implemented.

1. INTRODUCTION

Readout ASICs are a crucial element of modern "imaging" calorimeters, where the number of channels has increased tremendously to allow particle flow algorithms. More recently, picosecond timing capability has been developed to provide useful additional information and pileup rejection. The deliverable of WP4.3 consisted of the readout ASICs for the imaging calorimeters of WP14 and timing detectors of WP13. The technology chosen in Milestone MS36 was TSMC130 nm. The chip developed is called HGCROC1 for High Granularity Calorimeter Read Out Chip. It includes blocks designed by several AIDA2020 partners : CERN, Imperial and IRFU. It was fabricated in summer 2017, received by the end of the year and extensively tested since then. The results are good and were presented at the TWEPP conference in Antwerpen 2018.

2. 130 NM CMOS CALORIMETER READOUT CHIP HGCROC1

HGCROC is a 32-channels ASIC for charge and time readout. It has been designed originally for the CMS HGCAL calorimeter [1] and can be used with SiPMs and RPCs for accurate charge and time measurements. The specifications are the following :

- **low noise** (2500 e^-) and **large dynamic range**, from 0.2f C to 10 pC
- **linearity** better than 1% over the full range
- ability to provide **timing information** with a precision better than 50ps for pulses above ~12 fC (corresponding to about 3MIPs in the 300 um silicon)
- **fast shaping time** (peaking-time <20ns) to minimize the out-of-time pileup
- **compensation of the leakage current** which will develop in the silicon devices after irradiation (DC coupled sensors)
- **compatibility with negative and positive inputs** sensors, to be able to read both. p-on-n and n-on p
- on detector digitization and **data processing for zero suppression, for linearization and summing of the trigger data**
- **maximum latency** of 36 bunch crossings for the trigger primitives at the output of the detector
- **buffering** of the data to accommodate the 12.5 us latency of the L1 trigger;
- high speed readout links to interface with the 10Gb/s low power GBT serialiser
- **low power budget** <20 mW
- **high radiation resistance** (> 1.5 MGy and 10^{16} neq) and SEU compliance

Figure 1 shows the layout of the HGCROC1 chip, which has a size of 5 mm x 7 mm, providing the readout and digitization of 32 channels connected to sensors made of ~1 cm^2 silicon. The

32 channels are split 16/16 with the bias and clock distribution in the middle. The analog inputs are on the left side and the digital outputs on the right side.

The chip was designed by CERN, Imperial, CEA IRFU and OMEGA and assembled by OMEGA. It was sent to TSMC in July 2017 and received back in October.

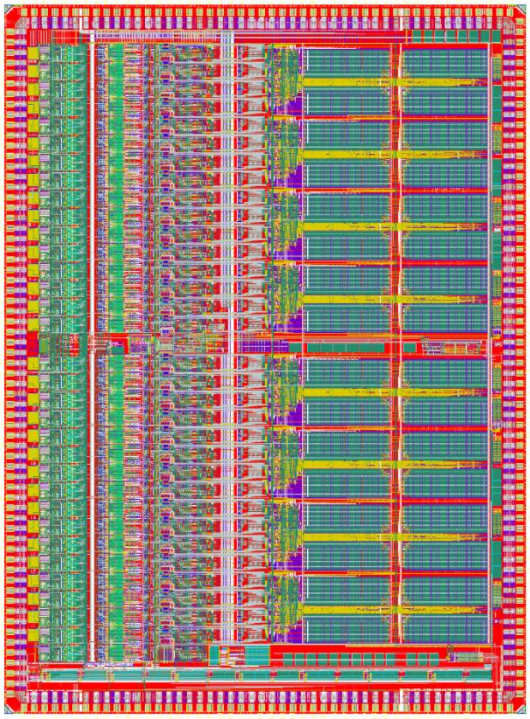

Figure 1: Layout of the 130 nm CMOS calorimeter readout ASIC HGCROC1

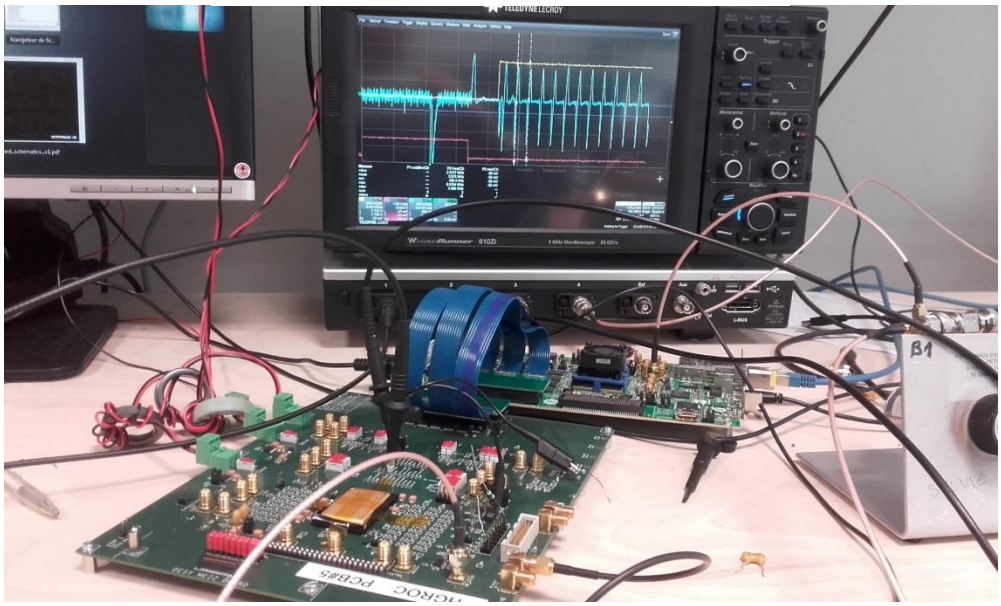

Figure 2: Testboard for HGCROC with the chip bonded directly on the PCB. High speed data are read by a Xilinx Kintek KCU5 digital board. First signals can be seen on the oscilloscope

3. HGCROC1 TEST RESULTS

The HGCROC1 chip is largely functional, and test results confirmed the demanding performance, in particular on the analog chain. As an illustration, the noise is shown in Figure 3. The chip achieves an excellent spectral density of en=0.79 nV/√Hz and an input capacitance of 13 pF, which allows the Equivalent Noise Charge specification of 2500 e^- rms to be met at a detector capacitance of 50 pF and a peaking time of 20 ns.

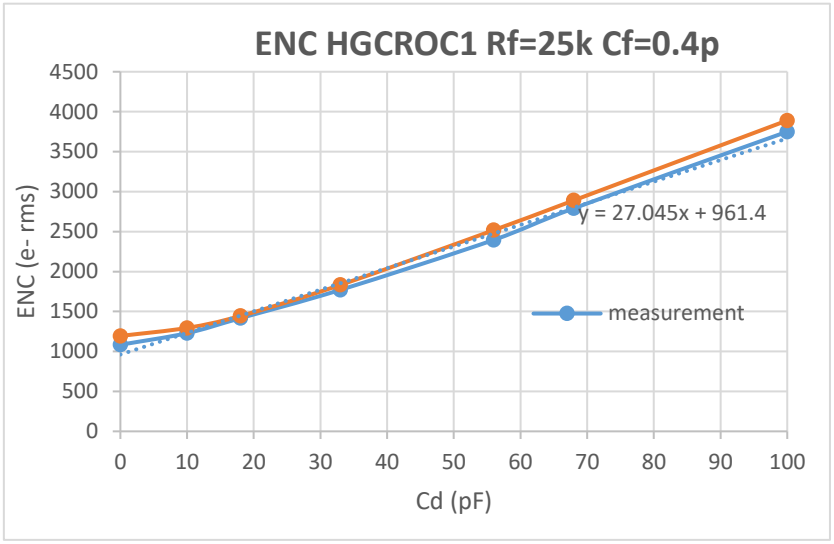

Figure 3: Equivalent Noise Charge as a function of detector capacitance.

The time over threshold (ToT) technique is used to measure large input charges that saturate the input preamplifier. This allows to extend the dynamic range up to 10 pC.

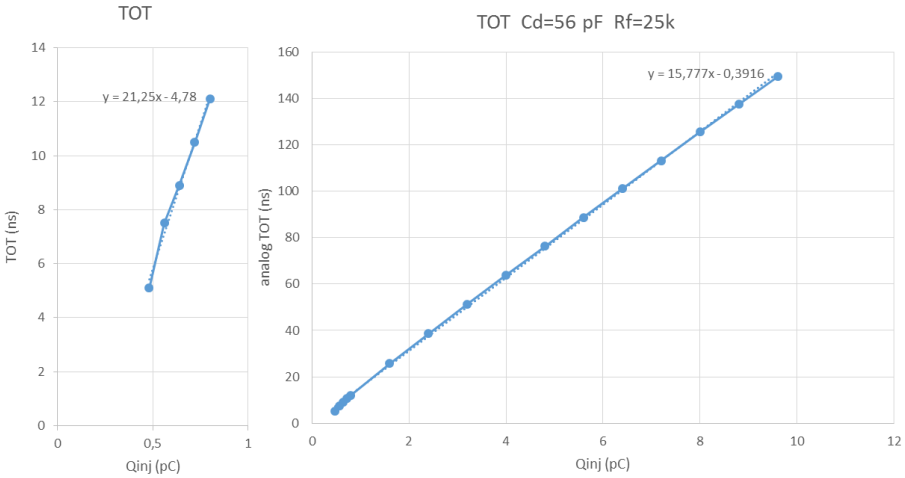

Figure 4: Time over Threshold measurement for changes up to 10 pC.

The timing accuracy is also an important parameter for the chip especially for the high accuracy timing applications. Thanks to its fast rise time (< 5 ns) and low noise, the timing performance can be lower than 100 ps down to 100 fC input charge on a 50 pF sensor. The jitter measurement

is shown in Figure 5. Although the performance is very good, there is still some work needed to understand the difference with the simulation results.

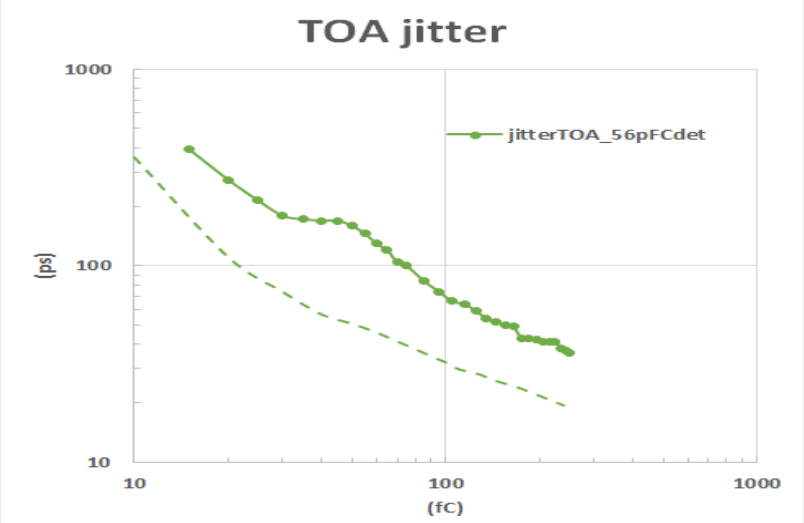

Figure 5: Measured jitter as a function of the input charge

The internal digitization at 40 MHz is a key feature of the chip. There are 32 40 MHz 11 bit SAR ADCs, inspired from the Krakow design running simultaneously. The reconstructed waveforms are shown in Figure 6, showing the satisfactory on-chip digitization. However, the noise is dominated by digital noise, which increases significantly the preamplifier noise. This will be addressed in the next version HGCROC2, which is using the original Krakow design and was sent to fabrication in February 2019.

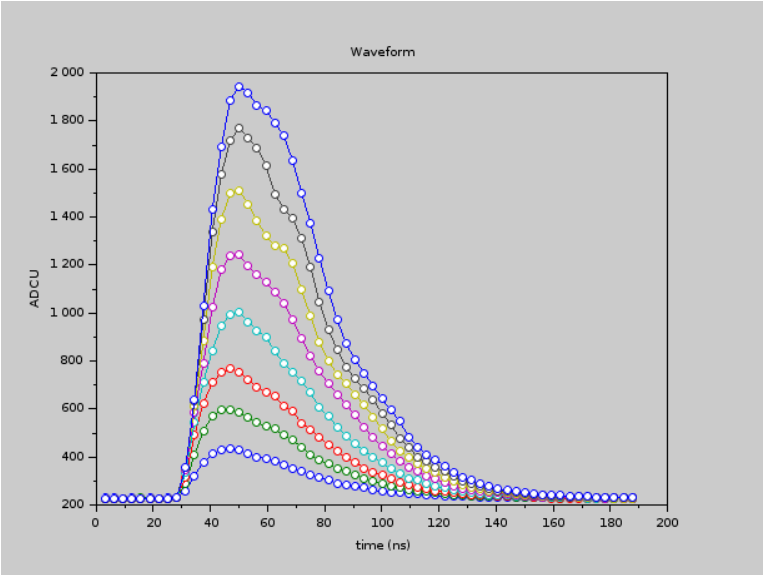

Figure 6: Reconstructed waveforms with the internal ADC

4. CONCLUSION

The 130 nm CMOS HGCROC1 chip was fabricated and successfully tested. The chip was delivered to WP14 for highly granular calorimeter R&D. Current work is focused on the design of the next 130 nm CMOS chip generation HGCROC2 that implements full functionality readout for Si and SiPM sensors readout to be used for the CMS HGCAL experiment.

The experimental results were presented at the TWEPP conference, Antwerpen 2018.

Milestone MS96 can be considered to be accomplished.

5. REFERENCES

[1] **Technical Proposal for the Phase-II Upgrade of the CMS Detector** - Contardo, D. *et al.* CERN-LHCC-2015-010, LHCC-P-008, CMS-TDR-15-02