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Monolithic pixel development in TowerJazz 180 nm CMOS for the outer pixel layers in the ATLAS experiment

I. Berdalovic,[a,1] R. Bates,[b] C. Buttar,[b] R. Cardella,[a] N. Egidos Plaja,[a] T. Hemperek,[c] B. Hiti,[d] J.W. van Hoorne,[a] T. Kugathasan,[a] I. Mandic,[d] D. Maneuski,[b] C.A. Marin Tobon,[a] K. Moustakas,[c] L. Musa,[a] H. Pernegger,[a] P. Riedler,[a] C. Riegel,[a,e] D. Schaefer,[a] E.J. Schioppa,[a] A. Sharma,[f] W. Snoeys,[a] C. Solans Sanchez,[a] T. Wang[c] and N. Wermes[c]

[a]*CERN Experimental Physics Department, CH-1211 Genève 23, Switzerland*

[b]*SUPA School of Physics and Astronomy, University of Glasgow, Glasgow G12 8QQ, United Kingdom*

[c]*Physikalisches Institut, Rheinische Friedrich-Wilhelms Universität Bonn, D-53115 Bonn, Germany*

[d]*Jozef Stefan Institute, SI-1000 Ljubljana, Slovenia*

[e]*University of Wuppertal, Gaußstraße 20, Wuppertal, Germany*

[f]*University of Oxford, Oxford OX1 3PA, United Kingdom*

E-mail: ivan.berdalovic@cern.ch

ABSTRACT: The upgrade of the ATLAS tracking detector (ITk) for the High-Luminosity Large Hadron Collider at CERN requires the development of novel radiation hard silicon sensor technologies. Latest developments in CMOS sensor processing offer the possibility of combining high-resistivity substrates with on-chip high-voltage biasing to achieve a large depleted active sensor volume. We have characterised depleted monolithic active pixel sensors (DMAPS), which were produced in a novel modified imaging process implemented in the TowerJazz 180 nm CMOS process in the framework of the monolithic sensor development for the ALICE experiment. Sensors fabricated in this modified process feature full depletion of the sensitive layer, a sensor capacitance of only a few fF and radiation tolerance up to 10^{15} n_{eq}/cm^2.

This paper summarises the measurements of charge collection properties in beam tests and in the laboratory using radioactive sources and edge TCT. The results of these measurements show significantly improved radiation hardness obtained for sensors manufactured using the modified process. This has opened the way to the design of two large scale demonstrators for the ATLAS ITk. To achieve a design compatible with the requirements of the outer pixel layers of the tracker, a charge sensitive front-end taking 500 nA from a 1.8 V supply is combined with a fast digital readout architecture. The low-power front-end with a 25 ns time resolution exploits the low sensor

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[1]Corresponding author.

capacitance to reduce noise and analogue power, while the implemented readout architectures minimise power by reducing the digital activity.

Contents

1 Introduction

The inner tracking system of the ATLAS detector [1] at the Large Hadron Collider (LHC, CERN, Geneva, Switzerland) will undergo a major upgrade (ITk) in view of the High-Luminosity LHC phase [2]. For the future upgrade of the pixel tracker, the ITk Pixel Detector, we are actively developing novel radiation hard CMOS sensors. They hold the promise to become the next generation of solid-state detectors for ATLAS and beyond HL-LHC. Due to their cost advantage, they are also interesting for equipping larger surfaces in future trackers. Therefore, ATLAS has recently established a dedicated ATLAS CMOS sensor development programme with the aim to design, manufacture and test novel CMOS sensor designs along the specifications for the ITk outer pixel layers. This encompasses radiation hardness up to several times 10^{15} n_{eq}/cm^2, hit rates between 1 and 10 MHz/mm^2 and readout architectures compatible with the ATLAS data taking in HL-LHC.

Depleted monolithic active pixel sensors (DMAPS), which can be produced in commercial CMOS technologies, are being proposed as an alternative to standard hybrid devices for the outer layers of the ITk Pixel Detector. Prototype chips have been designed by the ALICE collaboration in TowerJazz[1] 180 nm technology [3]. Originally conceived for studies for the upgrade of the ALICE Inner Tracking System (ITS) [4], the prototype chips are being investigated for application in the more challenging ATLAS ITk environment. The chips have been produced in a process modified to enhance the depletion of the sensitive layer. After encouraging results, also detailed below, design activity has been started to develop designs compatible with requirements for the outer pixel layers in the ATLAS ITk upgrade.

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[1]Tower Semiconductor Ltd, Israel.

2 Sensors produced in the modified TowerJazz 180 nm CMOS process

A key target of the design is to achieve a low capacitance of the collection electrode together with full depletion of the sensitive volume. A sketch of the pixel cross section in the standard TowerJazz process is shown in figure 1a. The charge generated by the energy deposition of an ionising particle is collected by an n-well diode, while the CMOS pixel electronics are shielded by a deep p-well. Reverse substrate bias increases the size of the depletion region, but its lateral extension over the full pixel width is difficult to obtain. To achieve full depletion of the epitaxial layer, a process modification has been developed together with the foundry [5] (see figure 1b). In this case, the sensor junction is planar and extends over the full pixel width. Since depletion starts at the junction, it immediately extends over the full width of the pixel. By applying sufficient reverse substrate bias, the depletion will extend to the n-well collection electrode and yield a small capacitance for this small electrode. Since the modification does not interfere significantly with the circuit layout, the same design can be produced in both processes, allowing a direct comparison between the two.

(a)

(b)
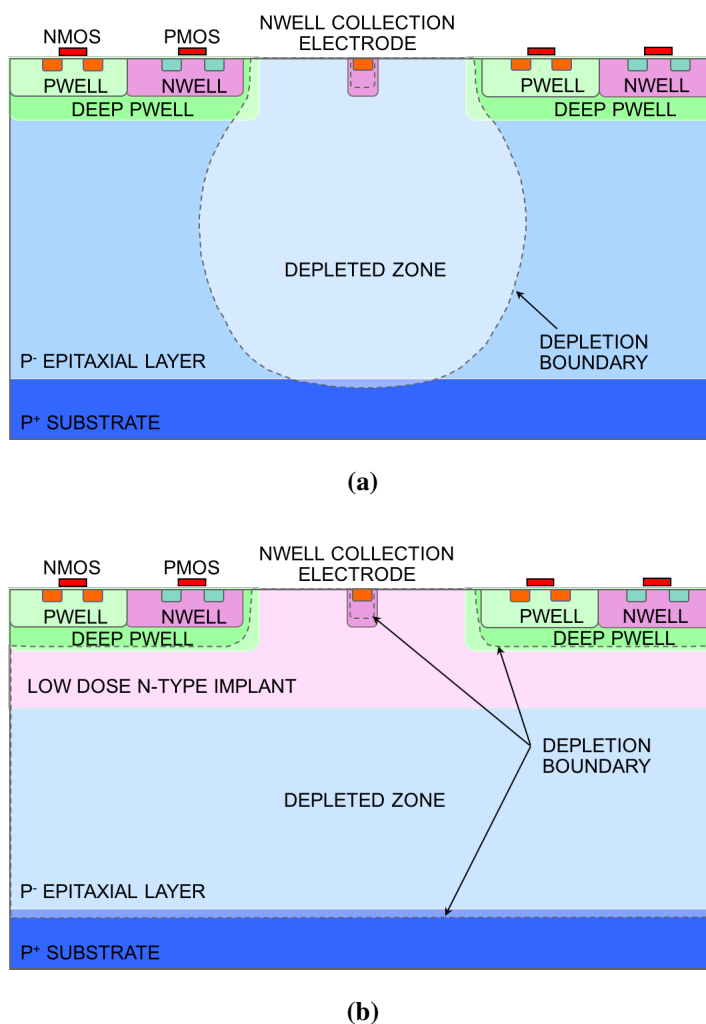
Figure 1. The standard TowerJazz 180 nm CMOS process (a) and the modified process (b). Reproduced from [5]. CC BY 4.0.

The Investigator chip [6, 7] was produced within the ALICE ITS upgrade project to study the analogue performance of monolithic CMOS sensors implemented in the TowerJazz technology. The chip consists of a collection of 134 pixel sub-matrices, each composed of 8×8 active pixels surrounded by a frame of dummy pixels. The analogue outputs of the 64 pixels of a sub-matrix can be read out simultaneously at the periphery of the chip. The sub-matrices differ among each other in terms of a few parameters, some of which affect the shape and extension of the depleted region: pixel size, electrode size, electrode-to-deep-p-well distance. The chip has a 25 μm thick epitaxial layer with a resistivity of about 1 kΩ·cm.

A number of Investigator chips produced in the modified process have been irradiated with neutrons at the Triga reactor in Slovenia. The received fluence is 10^{14} n_{eq}/cm^2 and 10^{15} n_{eq}/cm^2 (non-ionising energy loss, NIEL), together with 100 krad and 1 Mrad total ionising dose (TID), respectively, coming from the γ background at the facility. During irradiation, the samples were unbiased. After irradiation (including during measurements), the chips were always kept at $-15°$C or below to prevent annealing effects and maintain the leakage current at sufficiently low levels.

3 Measurements before and after irradiation

3.1 Characterisation with radioactive sources

Due to the different structure and depletion depth between the standard and modified process, we expect a significant improvement of radiation hardness for the modified process at higher fluences. Figure 2 compares the results of ^{90}Sr source tests on an unirradiated sample, a sample irradiated to a fluence of 10^{14} n_{eq}/cm^2 and a sample irradiated to a fluence of 10^{15} n_{eq}/cm^2. All samples were produced using the modified process and were tested at a substrate bias of $V_{sub} = -6$ V.

The red curve in figure 2a shows excellent signal response after a fluence of 10^{15} n_{eq}/cm^2, much in contrast to a sensor in the standard process after this irradiation fluence, from which no useful signal could be extracted anymore. Figure 2b shows the signal rise times. The sensor maintains a fast signal response even after a fluence of 10^{15} n_{eq}/cm^2. A small increase of signal rise time
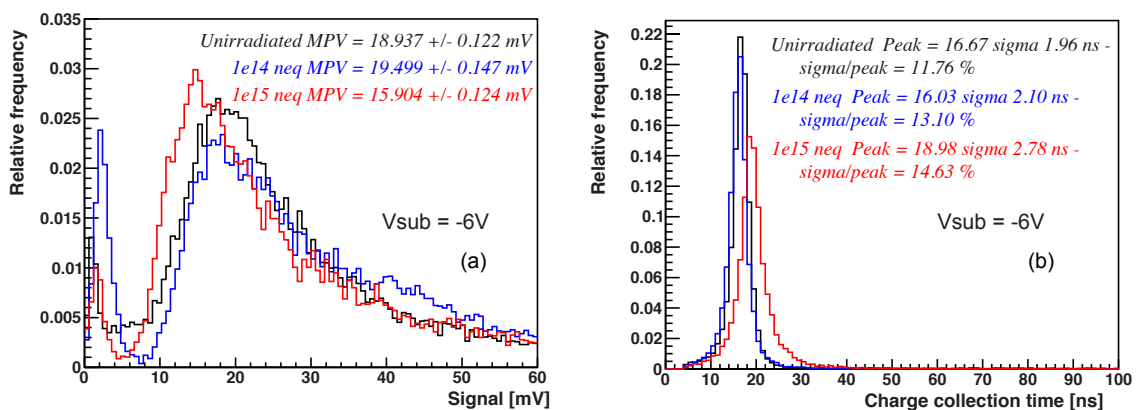

Figure 2. Signal response of a sensor with a 50×50 μm^2 pixel pitch produced in the modified process before irradiation (black curve), after 10^{14} n_{eq}/cm^2 (blue curve) and after 10^{15} n_{eq}/cm^2 (red curve). Figure (a) shows the amplitude distribution for ^{90}Sr source tests and figure (b) shows the signal rise time.

from 16.7 ns to 19 ns is observed, with a slight increase of spread from $\sigma = 1.96$ ns to $\sigma = 2.78$ ns. The time spread after 10^{15} n_{eq}/cm^2 is still significantly less than for the unirradiated sensor of the standard process, which gave $\sigma = 4.6$ ns. Note that the signal rise time is not only affected by the charge collection time, but also by the limited speed of the readout circuit.

3.2 Beam test results

Beam test measurements have been carried out to establish the effect of irradiation on the detection efficiency [8]. The chips were exposed to a beam of 180 GeV/c pions in the CERN SPS test beam area. The device under test (DUT) was placed between the two arms of a reference telescope [9], which could provide a 9 μm position resolution for hits on the sensor surface. For each of the measured Investigator sub-matrices, a 2×2 pixel group was read out using external amplifiers. Due to high noise in the measurement setup, the signal discrimination threshold was kept at relatively high values (≈ 600 e$^-$), which prevented the efficiency from reaching 100%.

The main results for samples produced in the modified process are shown in figure 3. After correcting for edge effects due to the telescope resolution, for unirradiated 50×50 μm^2 pixels with a 3 μm electrode and 18.5 μm deep p-well spacing, the efficiency is found to be 98.5% $\pm$ 0.5% (stat.) $\pm$ 0.5% (syst.), uniform across the pixel surface. For 10^{15} n_{eq}/cm^2 irradiated sensors with a 3 μm electrode and 3 μm spacing, the measured efficiency is 98.5%$\pm$1.5% (stat.)$\pm$1.2% (syst.) and 97.4% $\pm$ 1.5% (stat.) $\pm$ 0.6% (syst.), for the cases of 25×25 μm^2 and 30×30 μm^2 pixel size, respectively. For both pixel sizes, the efficiency is uniform across the pixel surface.

(a)

(b)

(c)
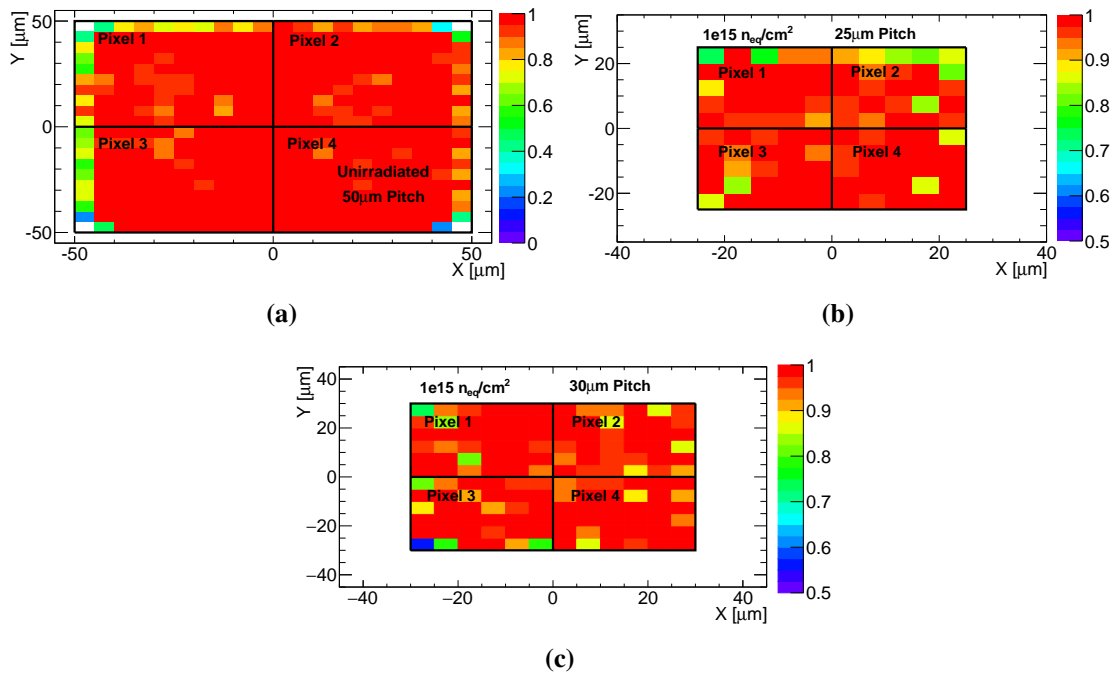
Figure 3. Detector efficiency across the 2×2 pixel group for the following samples produced in the modified process: (a) unirradiated 50×50 μm^2 pixel with 3 μm electrode and 18.5 μm spacing, (b) 10^{15} n_{eq}/cm^2 irradiated 25×25 μm^2 pixel with 3 μm electrode and 3 μm spacing, (c) 10^{15} n_{eq}/cm^2 irradiated 30×30 μm^2 pixel with 3 μm electrode and 3 μm spacing.

3.3 Edge TCT

Charge collection efficiency along the depth of the depletion region is measured using the edge transient current technique (e-TCT). The Investigator chips are mounted on a special carrier board that allows for a focused pulsed diode infrared laser (wavelength 1060 nm) to be directed onto the side of the chip. The DUT is held on a micrometric x-y stage for scanning the depth of the depletion region.

Preliminary results on unirradiated samples have been produced for a single $50 \times 50 \, \mu m^2$ pixel on an unirradiated chip in the modified process. Figure 4a shows a depth scan of the pixel edge performed with the substrate biased at -3.5 V in steps of $2 \, \mu m$. The horizontal axis gives the laser position as a function of depth in the epitaxial layer, the vertical axis scans along the pixel surface. From this map, the signal profile along the sensor depth at a central position in the pixel width ($y = 13.79$ mm) is extracted (figure 4b). The measurement of the same profile is repeated at different substrate bias voltages, yielding the results shown in figure 4c. The double-peak structure in the x direction is currently under investigation.

Figure 5a shows the charge collection profile as a function of the laser position in e-TCT measurements of the sub-matrix with a pixel pitch of $20 \times 20 \, \mu m^2$ before irradiation (left) and after

(a)

(b)

(c)
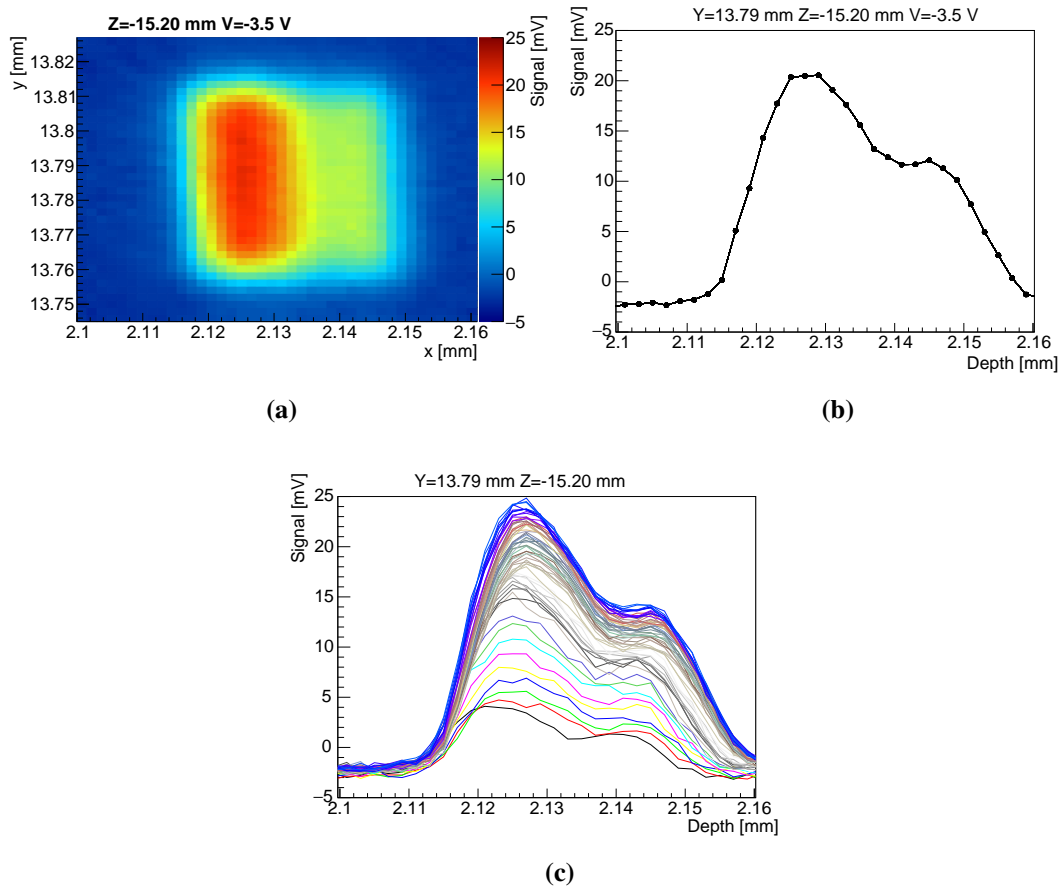
Figure 4. Edge TCT on unirradiated $50 \times 50 \, \mu m^2$ pixels produced in the modified process. Side scan of a single pixel (a), signal profile along the sensor depth at a fixed y position ($y = 13.79$ mm) (b), same profile at different bias voltages (c).

neutron irradiation to 10^{15} n_{eq}/cm^2 (right). For these measurements, 3 adjacent pixels were read out together in order to investigate the pixel boundaries better. Figure 5b shows the same plots for a pixel pitch of $50 \times 50\,\mu m^2$. While there is some limitation in spatial resolution due to the laser spot size, the active area of the pixel regions can clearly be identified. The depth of charge collection is 25 μm to 30 μm, which corresponds well to the thickness of the epitaxial layer. The signal uniformity of the $50 \times 50\,\mu m^2$ pitch sensor after irradiation is shown in figure 5c. The charge collection is uniform within 10% across the pixels at a substrate voltage of −6 V. We attribute the slight reduction in charge on the pixel boundaries to the very large spacing (18.5 μm) between the deep p-well and the collection n-well, which is a peculiarity of this sensor. The measured width of the full charge collection area is 155 μm, which agrees well with 3 times the pixel pitch.
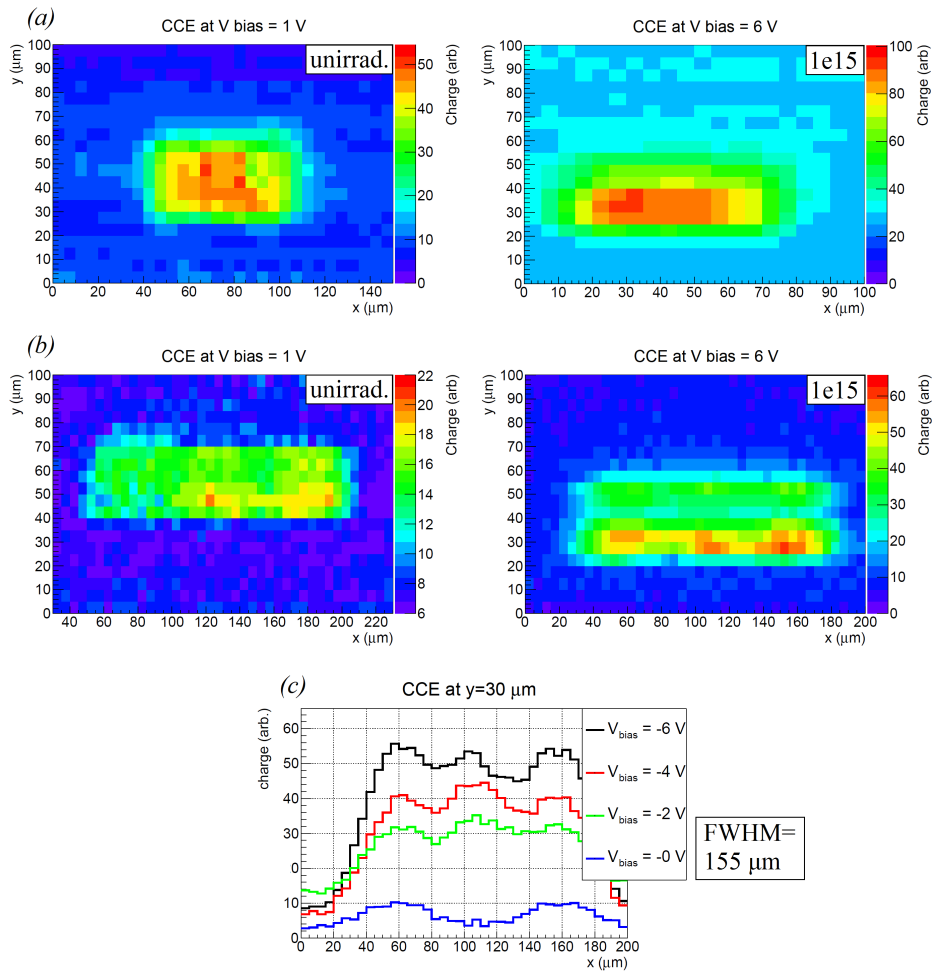
Figure 5. (a) Charge collection profile in edge TCT measurements of the sub-matrix with a pixel pitch of $20 \times 20\,\mu m^2$ before irradiation (left) and after neutron irradiation to 10^{15} n_{eq}/cm^2 (right). (b) Charge collection profile of a $50 \times 50\,\mu m^2$ pixel pitch sub-matrix before irradiation (left) and after neutron irradiation to 10^{15} n_{eq}/cm^2 (right). (c) Charge collection profile of the $50 \times 50\,\mu m^2$ pixel pitch sub-matrix after neutron irradiation to 10^{15} n_{eq}/cm^2, at different values of the substrate voltage. The shown profile is a section at $y = 30\,\mu m$.

4   Small electrode-size CMOS sensors for ATLAS

In the TowerJazz 180 nm technology, CMOS sensors implement a small collection diode sitting outside the deep p-well which contains all electronics. It is best suited for small pixels, as this limits the time the signal charge has to travel to the collection electrode and hence the probability that it is captured by radiation induced charge traps. A small collection electrode offers the advantage that the analogue circuitry in the pixel matrix can be quite simple and thus requires only a small fraction of the pixel area. Therefore, a comparatively large fraction of the surface is available for digital circuitry. Due to the small surface needed for the analogue parts, generally smaller pixel pitches can be obtained, while still featuring the required complex digital in-pixel electronics needed for the ITk. Present designs include the full analogue front-end and all the in-pixel digital readout logic in pixel pitches of approximately 36 μm to 40 μm.

Two different readout architectures have been designed and implemented for small electrode size CMOS sensors in the modified TowerJazz 180 nm process: an asynchronous readout scheme ("MALTA") and a synchronous readout scheme ("TJ MonoPix").

The asynchronous design avoids the propagation of the clock in the active pixel matrix region, which reduces risks of crosstalk and provides an optimal low-power operation. The address, timing and charge information for each hit is encoded in the asynchronous signals propagated through a column bus to the periphery, where the decoding of the address, as well as the measurement of the time of arrival and the deposited charge is performed. The decoded information is then buffered and transmitted off the sensor.

The synchronous design is based on the column drain architecture. Hits are buffered in the pixel cell and a "token" clock signal is passed from the top of the column to the bottom through each pixel. If a pixel is hit, the pixel address is asserted to the column bus when the pixel is clocked. At the end-of-column, the time-stamp is added and the time-over-threshold is encoded using the 40 MHz bunch crossing clock. In both architectures, the end-of-column logic buffers all hits on the sensor and transmits the hits off-chip.

The 31 $\times$ 25.5 mm^2 reticle of the ATLAS TowerJazz 180 nm engineering run is shown in figure 6. The reticle includes the following chips: MALTA (a full ATLAS size sensor with a 36.4 $\times$ 36.4 μm^2 pixel pitch and asynchronous readout of the 512 $\times$ 512 pixel matrix), TJ MonoPix (a half-size ATLAS sensor with a 36.4 $\times$ 40 μm^2 pitch and synchronous readout of the 224 $\times$ 448 pixel matrix), two versions of the Investigator chip, LAPA (a dedicated 5 Gbps LVDS driver test chip with programmable pre-emphasis), TID Test (a dedicated transistor level test chip to assess the effects of TID damage) and a memory and SEU test chip (with different memory configurations for future use in the final periphery).

The MALTA and MonoPix share the same analogue front-end designs which target low noise and low power consumption. The analogue front-end includes a charge sensitive amplifier followed by a discriminator and hit buffer. The designs target analogue currents in the range of 250 nA to 500 nA per pixel, which gives an analogue power consumption below 70 mW/cm^2, while the estimated digital power consumption for matrix readout in the outer layers is below 100 mW/cm^2 for MonoPix and below 10 mW/cm^2 for MALTA. The analogue front-end and in-pixel logic are full custom designs for optimal performance and best use of the pixel area. The collection electrode is surrounded by a 3 μm to 4 μm spacing. Slight variations of pixel geometries and the front-end
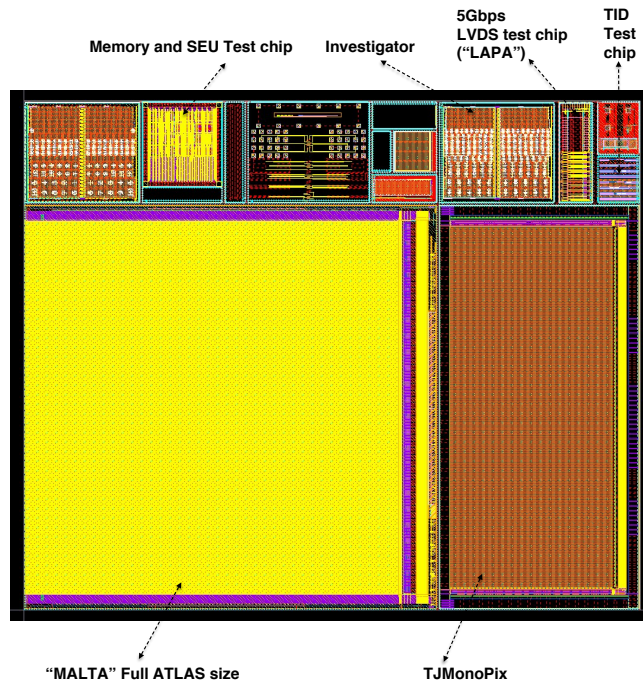
Figure 6. The TowerJazz 180 nm process ATLAS engineering run reticle.

circuit are implemented in different column regions of the sensors to further optimise the design towards ATLAS in test measurements.

4.1 Expected performance of the analogue front-end design for ATLAS

The design of the analogue front-end for use in ATLAS encompasses a source-follower input amplifier, which is connected to the signal collection n-well. The amplifier output is transmitted to a hit discriminator with a per-chip adjustable threshold. The front-end design is conceptually similar to the one used for the ALICE experiment [10], with the important distinction that a much faster signal rise time and baseline restoration time can be achieved, in order to meet the ATLAS requirements on 25 ns beam bunch crossing. Figure 7 shows the signal response at different stages of the front-end circuit: the top curve displays the analogue signal at the sensing node for a stimulus of $400\,e^-$ and $3000\,e^-$. The middle curve shows the analogue signal at the output of the amplification stage. The circuit includes a signal clipping mechanism, which limits the pulse amplitude and duration of large input signals and guarantees a fast baseline restoration. The bottom curves show the output of the discriminator for the two stimuli: the first signal is the discriminator output after the large input signal, the second after the small input signal.

Full extracted analogue simulations predict ENC noise of less than $10\,e^-$ at 500 nA, a time-walk of less than 25 ns and a threshold dispersion of around $10\,e^-$, as shown in figure 8. Note that the front-end is quite non-linear and that simulation of the S-curve is required to extract the noise at threshold. The targeted operating in-time threshold is approximately $300\,e^-$. Integrated charge on the input transistor is reset using either a diode (MALTA) or a PMOS transistor (MALTA and MonoPix). The pixel's functionality also includes analogue test pulses and pixel masking.
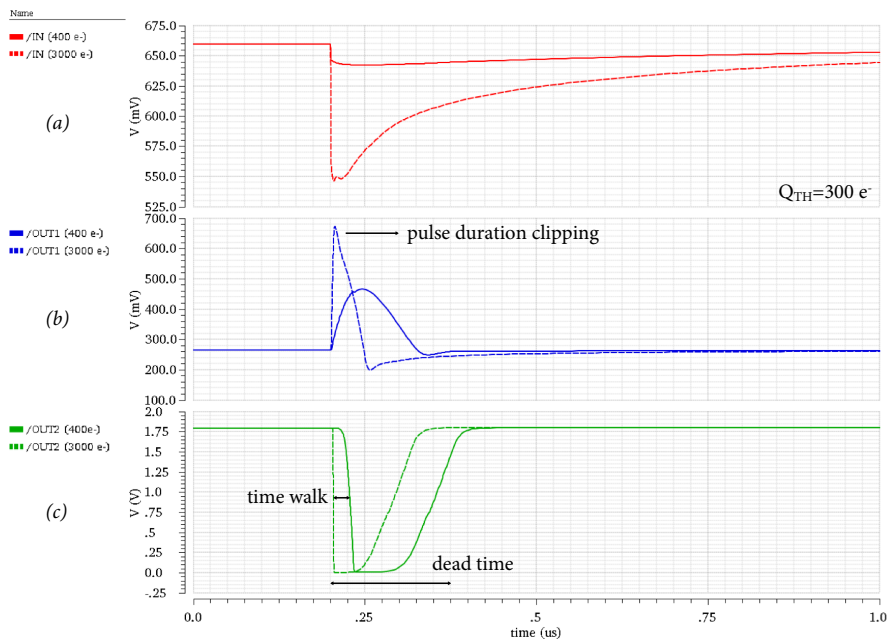
Figure 7. Simulated signal response of the MALTA chip analogue front-end circuitry: (a) signals at the sensing node, (b) signals at the output of the amplifier, (c) signals at the output of the discriminator

(a)

(b)
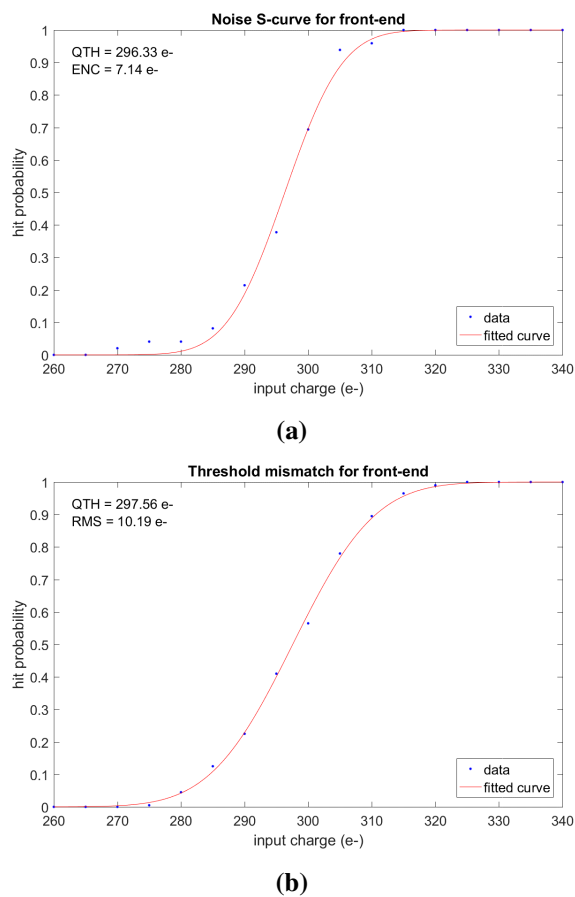
Figure 8. Simulated ENC noise performance (a) and threshold dispersion (b), shown as S-curves.

4.2 MALTA - High speed asynchronous matrix readout for ATLAS

The readout of the MALTA chip pixel matrix of 512×512 pixels is organised in double-columns. Each double column is subdivided into 64 pixel groups with 16 pixels, alternating as "red" and "blue", as shown in figure 9. A full double column has 32 red and 32 blue groups. The output of each pixel discriminator generates a hit signal of programmable width (0.5 ns to 2 ns) on one line of a 16 bit wide pixel bus. This bus transmits the pattern of hit pixels inside a group (usually stemming from the same cluster which is generated by one traversing particle). Furthermore, a static pixel group number is generated on the 5-bit group address bus with each hit, to identify the hit pixel's group. This process happens separately and in parallel in red and blue groups of a double column, in order to minimise any hit loss due to simultaneous signals on the double column bus. All signals are asynchronously transmitted on the column bus down to the end-of-column with a maximum latency of around 5 ns of signal propagation along the double column.

At the end of the double column, at the chip periphery, all signals of red and blue groups are merged onto a common bus. An arbitration logic is implemented at the end-of column, which time-sorts the pulses in case of simultaneous signals. When signals arrive simultaneously, they are delayed to avoid collisions and hit losses on the bus, while keeping track of the amount of delays for later correction. Additional column address bits and time-stamping information is added to each hit signal inside the periphery logic in order to identify bunch crossings for later trigger processing. The process of arbitration and merging of signals is repeated on 10 levels to merge the signals of all double-columns onto a 40 bit wide chip bus. Finally, the asynchronous hit signals are transmitted off the chip via LVDS drivers which are designed to operate at up to 5 Gbps.
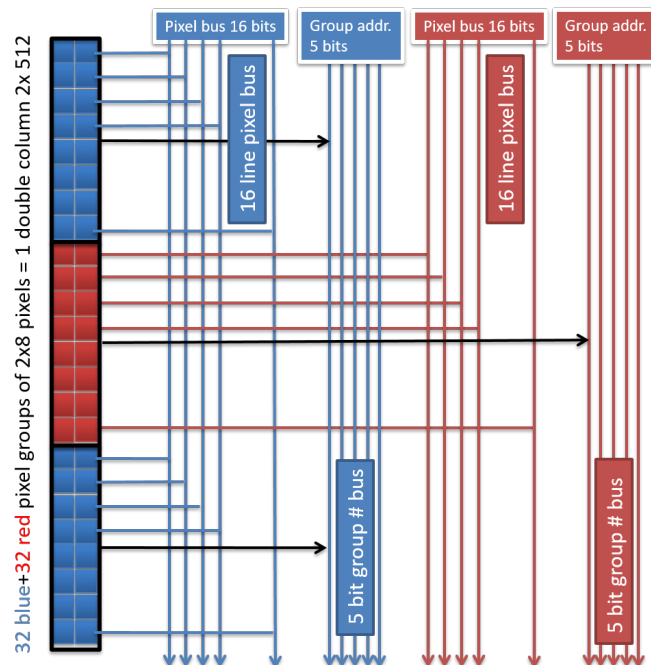

Figure 9. Schematic view of the MALTA double column readout.

5 Conclusion

Monolithic pixel detectors designed in the TowerJazz 180 nm CMOS technology are being proposed for the upgrade of the ATLAS Inner Tracker (ITk). The prototype Investigator chip, developed by the ALICE collaboration, has been used to evaluate the performance of this technology under the radiation conditions foreseen in the ATLAS pixel detector for the High-Luminosity LHC.

First measurements with sources and test beams show that chips produced with the standard TowerJazz technology are not capable of withstanding non-ionising energy loss up to 10^{15} $n_{\text{eq}}/\text{cm}^2$. However, the chips produced using a process modified to fully deplete the sensitive layer and improve radiation tolerance, remain fully functional and show high efficiency even after irradiation. Edge TCT measurement results also confirm the effectiveness of this process modification.

Based on these results, a full implementation of a radiation hard monolithic CMOS sensor for the ATLAS experiment was prepared. The MALTA and MonoPix monolithic sensors focus on an analogue front-end optimised for low capacitance, fast signal response and low noise, compatible with ATLAS specifications. MonoPix implements the more conservative and well-known column-drain architecture. For MALTA, a novel asynchronous readout architecture has been developed in view of the high hit rates expected in ATLAS, which avoids clock signals in the active matrix and focuses on low power dissipation and minimal analogue-to-digital crosstalk.

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