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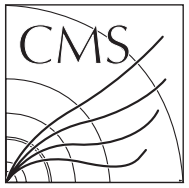

The Compact Muon Solenoid Experiment

Conference Report

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Operational Experience of the Phase-1 CMS Pixel Detector

Benedikt Vormwald for the CMS Collaboration

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This talk gives an overview of the detector performance in 2018 and describes the improvements made and challenges faced in the last two years of the detector operation.

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Operational Experience of the Phase-1 CMS Pixel Detector

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Abstract

In 2017, CMS has installed a new pixel detector with 124 million channels that features full 4-hit coverage in the tracking volume and is capable of withstanding instantaneous luminosities of $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and beyond. Many of the key technologies of modern particle detectors are applied in this detector, like efficient DC-DC low-voltage powering, high-bandwidth μTCA back-end electronics, and light-weight CO_2 cooling. By now the detector has been successfully operated for two years in proton and heavy ion collisions and very valuable experience has been collected with the aforementioned components. During the long shutdown of LHC from 2019 to 2021 the CMS pixel detector will be extracted and the modules of the inner most layer that suffered the most from radiation damage will be replaced. For that reason, a better readout chip as well as a new token bit manager chip will be used for these modules that fixes problems observed during operation.
This talk gives an overview of the detector performance in 2018 and describes the improvements made and challenges faced in the last two years of the detector operation.

Keywords: Silicon pixel detector, large detector system, radiation hard detector

1. The CMS Phase-1 pixel detector

In 2017, the CMS collaboration [1] installed a new pixel detector. The new detector features a 4-hit coverage in the tracking volume of $|\eta| < 2.5$. Compared to the old detector, the new layer 1 is located closer to the interaction point at a distance of $r = 2.9\,\mathrm{cm}$ and the fourth layer is located further outside at $r = 16\,\mathrm{cm}$. All details concerning the design of the detector can be found in reference [2].

The detector makes use of key technologies of modern particle detectors, which play also a key role in many Phase-2 upgrades of the LHC experiments:

DC-DC powering. The number of channels has been almost doubled in the Phase-1 upgrade of the pixel detector, but the number cables had to stay the same due to space limitations in the service channels. In order to limit the losses along the cable, 9 V (11.4 V in 2017) are converted only very close to the detector to the needed 2.4 – 3.0 V. The core of the DC-DC converters [3] is the FEAST2 chip [4], which is a radiation-hard and magnetic field tolerant ASIC developed by CERN.

μTCA back-end electronics. The back-end electronics are separated into front-end controllers (FEC), which are responsible for programming the detector as well as the fast signal (trigger, clock) distribution, and front-end drivers (FED), which act as receiver of the data from the front-ends. All components use a generic AMC card (FC7 [5]) which features a Kintech 7 FPGA and 4 GB of fast DDR3 RAM memory. Specialized FPGA mezzanine cards and special firmware determines whether the board is serving as FED or FEC. This scheme is highly flexible and has quite some advantages in the spare component management.

Evaporative CO_2 cooling. Evaporating CO_2 is a very efficient coolant [6]. Therefore, the technology allows to significantly minimize the material spent for cooling. In the CMS pixel detector, stainless steel cooling loops with a diameter of 1.7 mm and a wall thickness of 50 μm are used. The operation point of the cooling plant was $-22.0\,^{\circ}\mathrm{C}$ in the last two years.

Digital detector read-out. All the data transmitted from the detector is fully digital. This is possible because of a makeover of the old front-end chips. In layers 2 to 4 as well as in all disks, a digital version of the chip is used called psi46dig [7]. Apart from an on-chip 8-bit ADC it has larger hit and timestamp buffers with respect to the original read-out chip (ROC). The maximal expected hit rate in this region is $120\,\mathrm{MHz/cm}^2$ which can still be read out efficiently based on the column drain architecture. In layer 1, however, hit rates up to $600\,\mathrm{MHz/cm}^2$ are expected. In order to cope with those conditions, a new readout architecture was adopted (dynamic cluster column drain) and implemented in a new read-out chip (PROC600 [8]). All the modules have also a new, digital communication chip (TBM) that connects the ROCs with the back-end electronics.

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2. Operation experience

2.1. Single event upsets

Electronics that is exposed to ionizing radiation is expected to suffer from single event upsets (SEU). Also during the operation of the CMS pixel detector SEUs have been observed in almost every electric component along the signal path in the radiation area. The impact of those SEUs can range from inefficient single pixels to complete ROCs or even complete read-out groups if global delay or opto transmitter chips are affected by the SEU. For that reason, an advanced recovery algorithm has been developed that, depending on the severeness of the incident, reprograms the affected component or waits until a certain threshold of inactive components is reached. For this action the triggers are stopped globally.

In addition to the expected SEUs, the TBM could end up in an unexpected latched-up state. In this state, the ROCs behind the affected TBM could not transmit their data. This could not be resolved by reprogramming the chip, but only by a power-cycle. In 2017, the disable/enable feature of the DC-DC converter, which powers up to four modules in BPix, was used to reset the latched-up TBM. This, however, revealed a flaw in the FEAST chip as discussed in Section 2.2.

2.2. Operation of the DC-DC converters

In October 2017, a series of DC-DC converter broke in the process of power-cycling modules. From an extrapolation of the failure rate, it was clear that by mid of 2018 track seeding would be affected that severely from inactive components that no sufficient tracking would be possible anymore. For this reason, the detector has been extracted in the year end technical stop of LHC in 2017/2018 and all DC-DC converters have been replaced with the same version as upto the moment of the re-installation the origin of the failure was not understood. As only difference, the DC-DC board was equipped with a larger fuse that allowed to operate the DC-DC converter at a lower input voltage in 2018. A current-voltage characterization of all extracted converters showed that 65 of the total about 1200 converters were broken (as expected), but 333 had a higher power consumption in the disabled state compared to the specifications.

The failure could finally be traced back to a single transistor in the FEAST chip which developed some leakage current after irradiation [9]. In the disabled state, this current cannot be drained, but instead it is amplified and charges up a capacitor that in turn can damage the connected components when discharging. If, however, the discharge forms a new (persistent) path to ground, the leakage currents can be drained at the cost of a higher power consumption in the disabled state, as observed.

As a consequence, power-cycles were no longer performed with DC-DC converters, but directly by disabling/enabling the power supply. Together with the operation at a lower input voltage, this lead to the fact that in 2018 no single DC-DC converter broke.

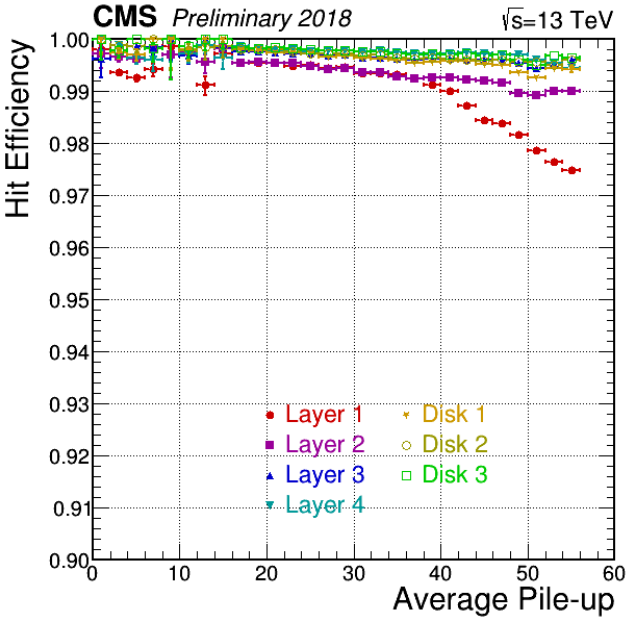

Figure 1: Measured hit efficiency for different numbers of pile-up events. In layer 1, inefficiencies towards very high and low number of pile-up events are visible. This effect comes from an understood feature of the read-out chip which will be addressed in the next version of the chip.

2.3. Layer-1 challenges

In the operation of layer 1, a couple of challenges have been faced. The front-end chip PROC600 turned out to be half a clock cycle (12.5 ns) faster than the psi46dig. Due to the design of the service electronics, layer 1 and layer 2, share the same clock and trigger distribution which does not allow for an individual delay adjustment of the two layers. A common delay setting could be found that allows for a fully efficient operation although the overlap of the efficiency plateau is only about 2 ns wide. The timing has been adjusted in a way that layer 1 is read out slightly too late while layer 2 is read out too early. This optimizes the charge collection in layer 1, while it is sub-optimal in layer 2.

Another issue that has been found was the appearance of noise hits a couple of bunch crossings after a real hit. In order to suppress this cross-talk and to be able to operate the chip efficiently, thresholds in layer 1 were artificially increased by 1000 electrons to about 2200 electrons in 2017 and 2018. It was found recently that the cross-talk is induced by active circuit paths running over injection pads of pixels. A special programming sequence of the chip can disable these lines and greatly suppress the cross-talk. Also a better shielding design will further mitigate the effect in the future.

In Figure 1, the hit efficiency is shown. It is visible that the performance of layers 2–4 and all disks is excellent being efficient more than 99% up to the highest number of pile-up events. Layer 1 has some larger inefficiency for very high and very low instantaneous luminosities. This effect comes from desynchronization of the double column periphery and will be addressed in a new version of the chip.

Tracking performance was not noticeably affected by all

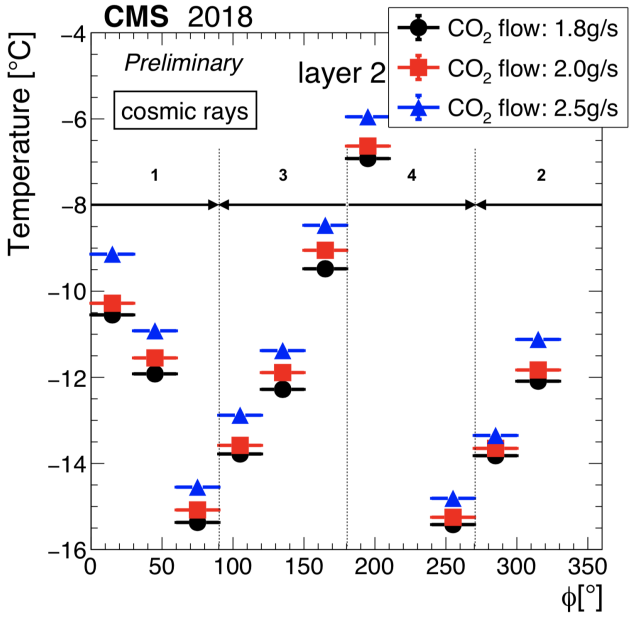

Figure 2: Measured temperature at different positions in ϕ in layer 2 of the BPix detector. Sections that are cooled by an independent cooling loop are indicated with horizontal lines. The arrow shows the direction of flow of the CO_2. A temperature drop of up to 6 °C from the inlet to the outlet has been observed. A reduction in the mass flow mitigates the effect slightly.

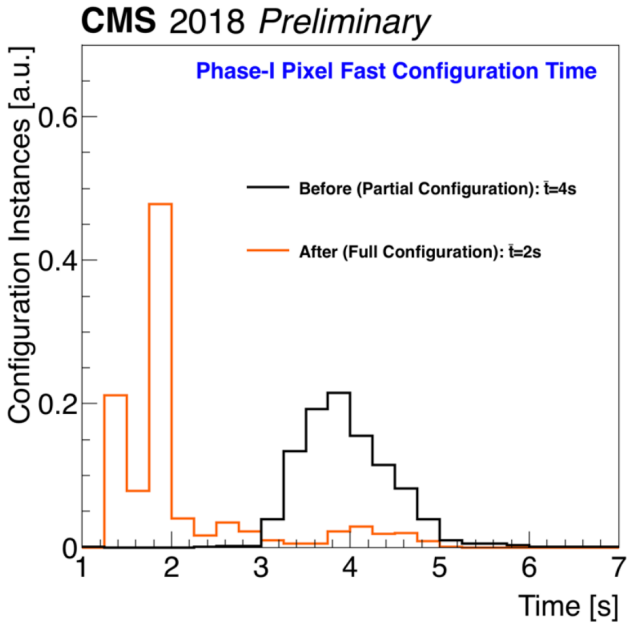

Figure 3: Difference in time needed for the front-end configuration before and after the update of the firmware of the front-end controller (FEC). In the new version, the detector configuration is pre-loaded into DDR memory and therefore the front-end chips can be configured very efficiently. Note that the time before the update comprises only global ROC-level configuration parameters, where after also pixel-level settings are sent.

above mentioned effects.

2.4. *Evaporative CO_2 cooling*

The operation of the cooling system was very efficient and no down-time was assigned to the cooling system in 2017 and 2018. Inside of the detector a temperature gradient of up to 6 °C has been observed along a cooling loop (c.f. Figure 2. The vertical lines in the figure indicate the sections covered by a single cooling loop. The arrow show the direction of the flow of the CO_2. It is a feature of evaporative CO_2 cooling that the temperature decreases along the path inside of the detector as there is a non-negligible pressure drop within the tiny cooling pipes of the detector.

The effect could also be verified with a small-scale, thermal mock-up which is equipped with many more temperature probes and, thus, was an invaluable tool in understanding the thermal behaviour of the detector.

One important lesson learned in the context of the operation of a very light-weight CO_2 cooling system is the fact that it is not possible to efficiently warm up a detector without active heat dissipation. This might especially have an impact on planned annealing campaigns of silicon detectors as well as in safety matters.

2.5. *DAQ system*

The μTCA back-end system worked very reliably in the last two years and no hardware failures occurred. For both, FED and FEC, improvements of the firmware were developed and deployed. The design of the FED firmware was changed in order to allow for a parallelized read-out of its channels. This increased the maximal data throughput significantly. The FEC firmware was improved in order to make optimal use of the on-board DDR memory of the FC7 card. With this change the entire front-end configuration could be pre-loaded to the fast memory and sent to the front-end much faster than in the conventional method. Figure 3 shows the configuration time with the old and new firmware. Sending global ROC and TBM settings lasted with the old firmware on average 4 s, while after the upgrade all settings (TBM, ROC, and pixel trim/mask settings) are transmitted in only 1.5 – 2 s. While an improvement of the configuration speed might appear irrelevant on these scales, in case of SEU recovery procedures during data taking it makes a significant difference if just the global or all front-end settings can be refreshed in a short time.

3. Measurement and modulation of radiation damage

In order to measure the effect of radiation on the silicon sensor, bias scans have been performed every 5 – 10 fb^{-1} on a set of representative modules from each layer. The modules have been selected such that overlap and potential inefficiencies in the same solid angle are ruled out during the bias scan. For that reason, the bias scan could be performed in parallel to normal data taking. From the collected data, the depletion voltage of the sensors could be derived and compared to a radiation damage model based on the Hamburg model [10]. Agreement has been found on the level of 30−40%. Further optimization of the depletion voltage prediction is work in progress. In addition to the depletion voltage, the model also predicts the leakage currents of a given silicon volume based on its thermal history and

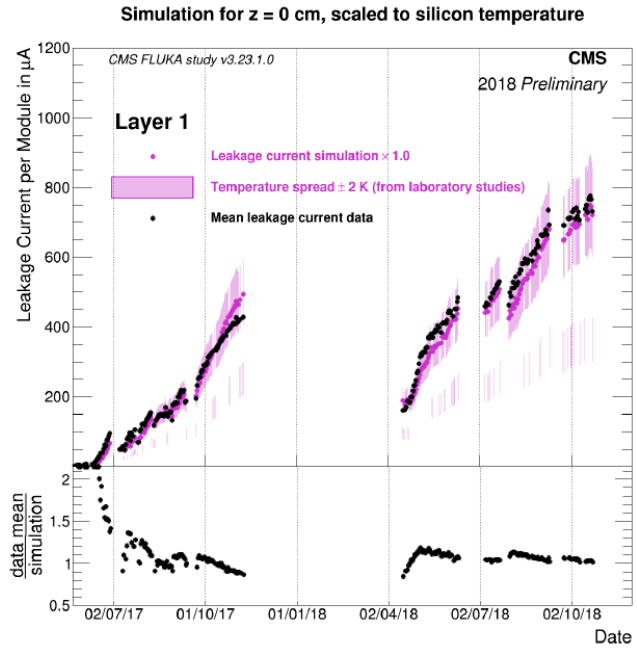

Figure 4: Measured and predicted leakage current in layer 1 modules. The measured values in a layer are averaged. The prediction is based on the Hamburg model [10] and uses the full temperature history as well as the fluence profile as input. For layer 1, the agreement between model and data is very well while for other layers a scale factor needs to be applied.

particle fluence. Both, the thermal model of the detector and the fluence model are receiving a lot of attention at the moment and might be adjusted in the future. Figure 4 shows the predicted and measured leakage currents in layer 1. The agreement for this layer between prediction and measurement is excellent. In the other layers, the prediction underestimates the measurements and needs to be corrected by a scale factor.

4. Plans during LHC long-shutdown 2

During the LHC long shutdown 2 (LS2), most of the time the CMS Phase-1 pixel detector is inactive and stored in clean rooms on the surface. In order to prevent reverse annealing, the detector temperature is kept below 5 °C. Nevertheless, significant improvements and interventions are planned for the next two years:

- Replacement of all DC-DC converters with a new version that is protected against the failure scenario described in Section 2.2.
- Repair of accessible problematic channels.
- Upgrade of power supplies from 600 V to 800 V.
- Replacement of layer 1.

The replacement of layer 1 was already foreseen in the TDR in order to cope with the radiation damage in the silicon sensor in the innermost detector layer and to ensure the detector performance until the end of its lifetime. At this occasion an improved version of the PROC600 as well as of the TBM will be used which will mitigate all the shortcomings described in Section 2.3.

5. Conclusions

The CMS Phase-1 pixel detector has been successfully operated for two years. Due to a massive DC-DC failure at the end of 2017 an unforeseen extraction took place and all the DC-DC converters were replaced. In 2018, operation went very smooth and no DC-DC converter broke. Significant improvements of the detector are scheduled for LHC LS2 such that the detector will be in the best possible shape at the beginning of LHC Run-3.

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