AIDA-2020-MS94

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Advanced European Infrastructures for Detectors at Accelerators

Milestone Report

PCB development using HDI-technology and 3D-mounting of chips for MPGD readout

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Advanced European Infrastructures for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDA-2020

MILESTONE REPORT

PCB DEVELOPMENT USING HDI TECHNOLOGY AND 3D-MOUNTING OF CHIPS FOR MPGD READOUT

MILESTONE: MS94

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Abstract:

The purpose of this project is to develop readout electronics for MPGD detectors where the channel occupancy is compatible with a pad size of approximately 1x6 mm^2. The readout electronics is based on the SALTRO-16 ASIC developed at CERN and the readout board is designed in HDI technology. The chip combines analogue and digital signal processing.

AIDA-2020 Consortium, 2019

For more information on AIDA-2020, its partners and contributors please see www.cern.ch/AIDA2020

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Executive summary

This report summarizes the various phases of the development of a miniaturized and flexible readout system for Micro Pattern Gas Detectors, with ASICs mounted on small Multi-Chip Modules designed in High Density Interconnect technology.

1. INTRODUCTION

The purpose of this project is to develop a readout system for Micro Pattern Gas Detectors (MPGD), for which the size of the channel occupation of the front-end electronics is comparable to the size of the readout pads of the detector. The pad size aimed for is 1 x 6 mm^2. This geometry combines a large enough area to collect sufficient charge with a narrow pad width to provide excellent spatial resolution. The readout electronics is based on the SALTRO16 ASIC [1], developed at CERN. This chip combines highly sensitive analogue front-end with digital signal processing in the same compact circuit.

The SALTRO16 ASIC has 16 channels. It allows for power pulsing, since the voltage can be switched off over the time when no signals are expected. This enables for a potential significant reduction in power consumption, which has an impact on the amount of cooling that has to be provided.

The SALTRO16-chip provides a very versatile system in the sense that it offers the possibility to set various readout parameters (polarity, shaping time, gain, decay time) in the SALTRO pre-amplifier. It is optimized for low capacitance detectors, sensitive to femtocoulomb signals with digital correction of the base line, followed by advanced pulse recognition and zero suppression.

The small units of the readout system are suitable for applications and detector R&D, not only in particle physics but in a variety of other fields using Micro Channel Gas Detectors for imaging, like medical diagnostics, material science at XFEL, and for investigations at ESS. The proposed front-end electronics enables a large number of channels to be mounted in a reasonably short time, which will significantly improve the usage in test beam infrastructures.

2. MOUNTING OF SALTRO16 ASICS ON A CARRIER BOARD

2.1. DESIGN OF THE CARRIER BOARD AND TESTS

Design phase

At the start-up of this project, it was not possible to identify a company able to package the SALTRO16 ASICs in small enough capsules to match the pad size that we were aiming for. As a consequence, it was decided to develop a carrier board of the adequate size (12.0 x 8.9 mm^2) onto which the dies, with the size of 8.7 x 6.2 mm^2, were going to be bonded. The design of the carrier board was successfully completed in Lund and the printed circuit board was produced (see Figure 1).

After mounting of the die, the top side of the board was covered with a thin epoxy layer as protection of the die, the bonding wires and the passive components. On the bottom side of the board, small tin balls in a BGA footprint were applied for later soldering onto the so-called Multi-Chip-Modules (MCM). The MCM board should house eight of these carrier boards together with a CPLD chip, connectors and passive components on an area of 32.5 x 25 mm^2. This corresponds to a channel occupancy of 6.4 mm^2, essentially consistent with our goal.

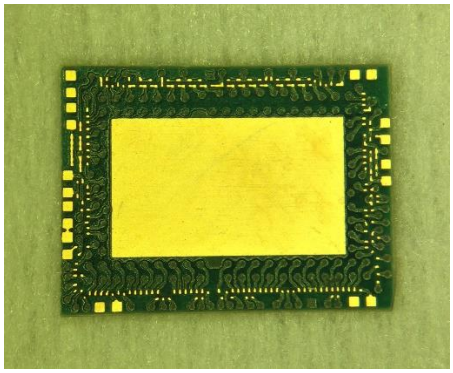

Figure 1: The Carrier board

Design of a Test board and its read-out

In order to test the functionality of the SALTRO16-chip mounted on a carrier board, a test board, containing a test socket onto which the mounted carrier should fit with high precision, was designed in Lund and produced (see Fig. 2). This board was connected to the PGA socket on the test board, used at CERN for testing QFP packaged chips. For the test set-up a Low Voltage supply board was also designed and produced (see Fig. 3). The test set-up is read out via the readout system used in the EUDET TPC test beam. The test set-up was assembled and ready for tests in 2015.

Another test board equipped with a QFP packaged SALTRO16 chip, which had been successfully tested at CERN and re-tested in Lund, was produced in order to verify the functionality of the test board itself and for development of the readout software. This board is read out via an SRU (Scalable Readout Unit) developed by RD51 at CERN.

However, the FPGA firmware on the SRU had to be modified for full functionality in our application. Since we do not have this expertise in the group, we had to find someone from outside. In 2015, we engaged an FPGA-programmer from the ALICE-experiment on part time, who unfortunately had to leave the project after some time due to employment circumstances. Next, a master student from the Faculty of Engineering in Lund entered the project. Before he could finish he was offered an employment in Industry.

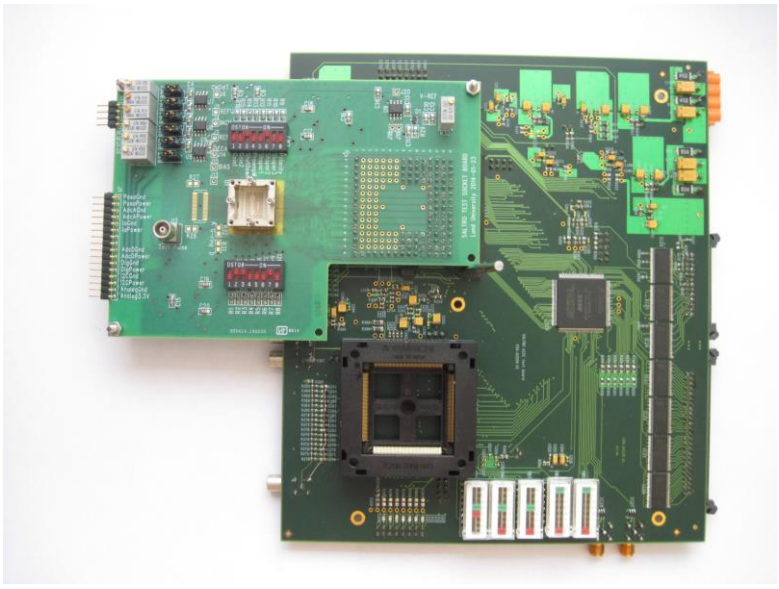

Figure 2: The test board for testing chips on carrier board

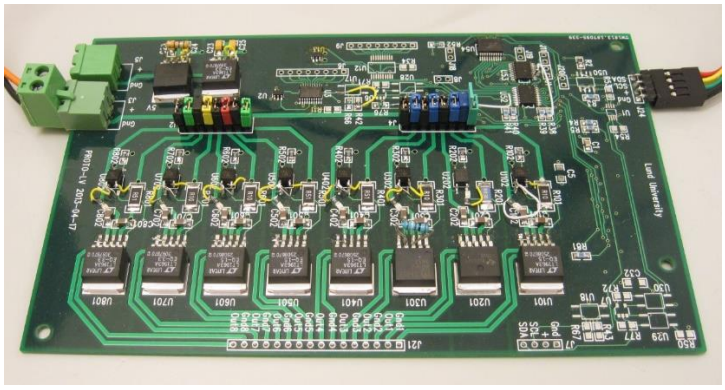

Figure 3: The Low Voltage supply board.

The present status of the readout system is that we are limited to a simultaneous full read out of 2 out of 16 channels, which severely limits our test capacity. All 16 channels can be read, but then only a fraction of the data memory in the chip can be used.

Mounting of ASICs and test phase

Contact with a company was established, for developing a method to mount and package the SALTRO16 chip on the carrier board. As we received the first fully mounted carrier board (see Figure 4), it turned out that the surface of the epoxy layer was not flat enough to allow for adequate electrical contact to the test board. This would also not provide sufficient conditions for an efficient cooling. From electrical tests it became clear that some wires were shorted and there were some other problems. Another fully assembled carrier board was ordered and delivered but it had the problem that some channels had no connection and that disturbances were seen on the digital control signal. Some further iterations were made but without any significant improvement.

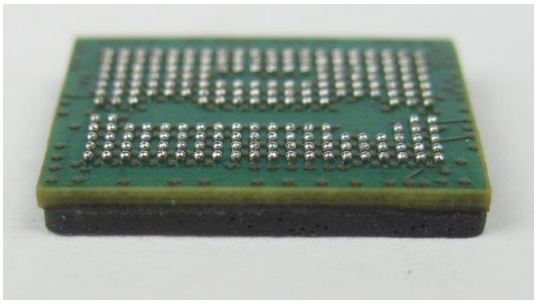

Figure 4: A carrier board with mounted SALTRO16 ASIC, showing the soldering balls on the bottom side and the epoxy glop on the top side.

In order to be completely convinced that the problems were not caused by an error in our test board, an assembled carrier board was soldered directly onto an adaptor board that fit into the PGA-socket of the CERN test board. The problems remained and this convinced us that there was something wrong with the mounted chip boards themselves.

In the beginning of 2017 an X-ray investigation was performed, which revealed that some bonding wires did not have a sufficient loop but were essentially resting on the edge of the die. As the board

was heated up, in the process of applying the tin balls, these wires were ripped off due to the different expansions of the printed circuit board and the epoxy layer.

In all the test which were performed there was nothing indicating an error in the design of the carrier board.

In the meantime, we had found a company, which was able to package the ASICs in a capsule of adequate size. The contract with the first company was terminated on 25/2/2017, almost two years after the start of AIDA-2020.

2.2. THE MULTI CHIP MODULE

The MCM board is the smallest unit in this readout electronics for MPGDs. The small size enables high flexibility and adaptation to various detector geometries. In order to make sure that the spatial constraints were fulfilled a mechanical sample was manufactured (see Fig. 5). A design in HDI (High Density Interconnect) technology was carried out, the advantage of which is a higher routing density compared to conventional PCB design. This results in fewer layers in the board. However, due to the failure of mounting the dies on the carrier boards it did not make sense to have the final MCM board produced.

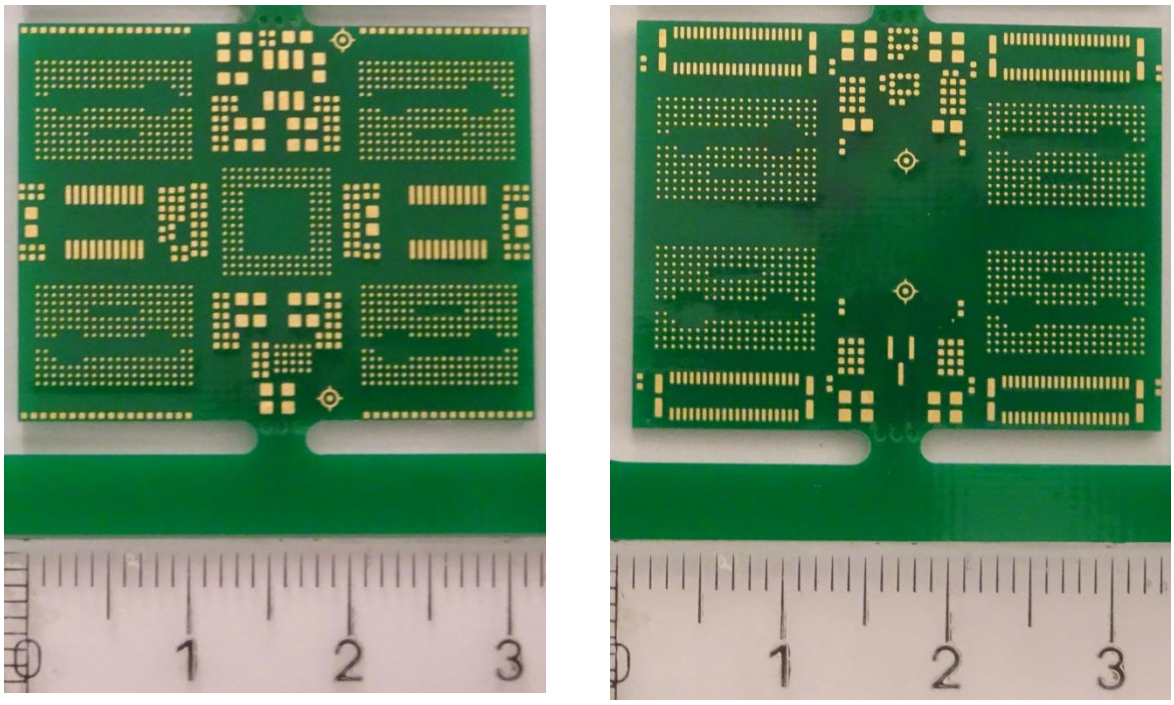

Figure 5: The Multi-Chip-Module printed circuit board, top-side left and bottom side right.

3. PACKAGING ASICS INTO CAPSULES

A contract with the new company was signed on 17/2/2017 and the dies were transferred. An initial visual inspection and measurement of a small die sample revealed that some of the dies had scratches or other damages that made them unusable and that the variation in size within this sample was 165 µm in one direction and 120 µm in the other direction. This presents a potential problem for successful packaging.

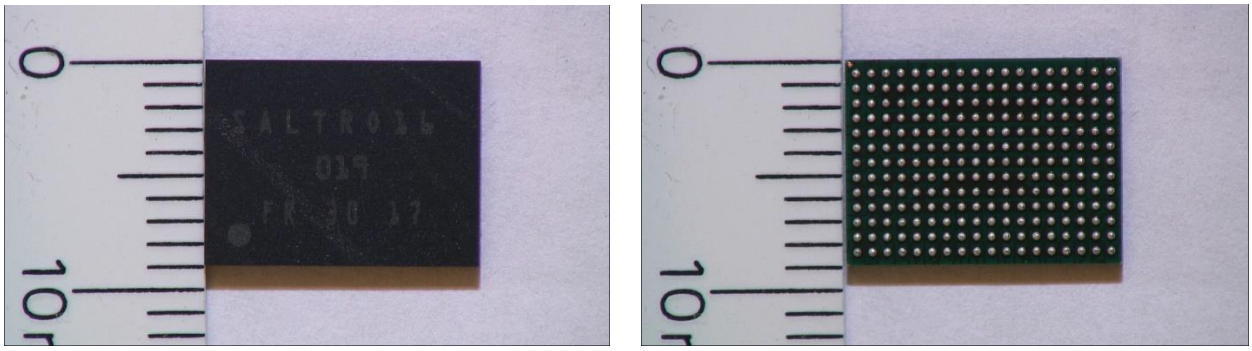

Figure 6: A packaged ASIC showing the top side (left) and the bottom side (right).

The first pre-series of 34 chips had a perfect surface quality and the packages had very precise dimensions (see Figure 6). However, in the subsequent tests only 20 chips passed the requirements. The tests required a re-design of the test board as described in Section 3.1. It was carefully checked that there was no bug in our test board with a QFP package. It was agreed with the company on a procedure for selecting and positioning the dies before the bonding. The subsequent pre-series of 55 chips gave a yield of 85%, well beyond the expectations. The order to package the full sample followed and recently we received 705 chips, which were judged as successfully packed by the company. The test of these will be performed as soon as the problem with the FPGA programming has been solved.

3.1. DESIGN OF A NEW TEST BOARD

The test board used for developing the readout software was modified in such a way that the QFP packaged chip was replaced by a socket for the new packaged chip. The new version of the test board (see Figure 7) was used to test the packaged pre-samples.

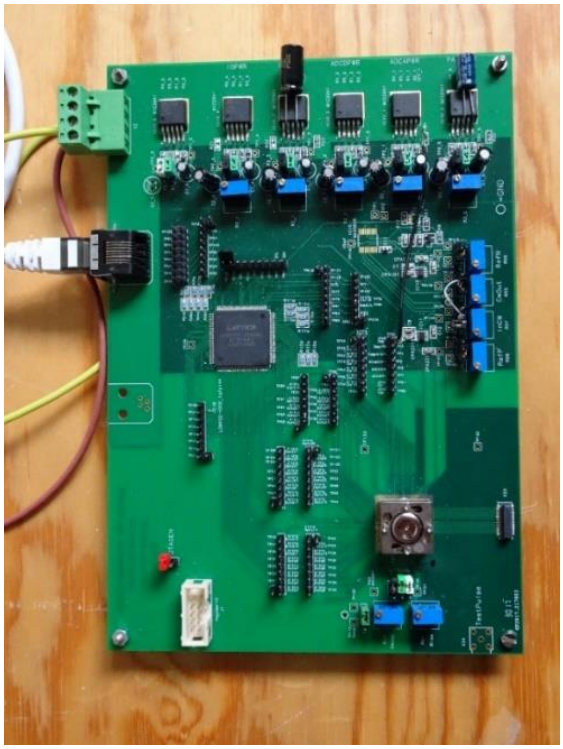

Figure 7: The test board for testing packaged chips

Later a new and smaller CPLD was found, which will provide somewhat more space for mounting the other components on the final MCM board. This led to further modifications of the test board, which were implemented and the PCB has been produced. The electronics components have just been mounted at DESY (see Figure 8). The test socket and the various connectors will be mounted at Lund. The aim is to test all the packaged chips with this test board. Before this can begin, we have to find an FPGA-programmer who can finalize the programming of the CPLD and the SRU.

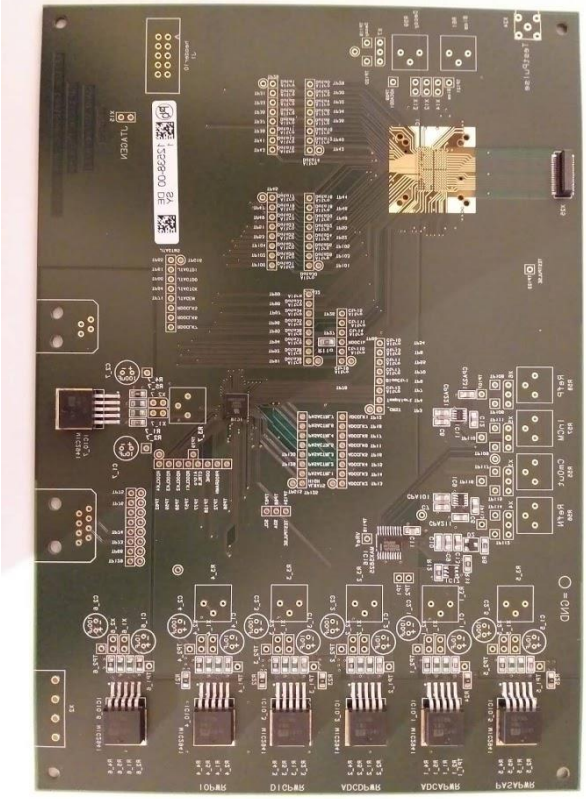

Figure 8: The new test board

3.2. DESIGN OF A NEW MULTI-CHIP-MODULE

The design of the MCM board has to be modified to make it compatible with the BGA footprint of the packaged chips and to accommodate the new CPLD. In addition, we are investigating if there are alternative space-saving connectors.

The re-design of the MCM-board is about to start but the completion is awaiting the first test results from the new test board, which can be obtained using the already tested chips

4. REFERENCES

[1] Aspell, P. et al., (2011) 'Description of the SAltro-16 chip for gas detector readout', http://cdsweb.cern.ch/record/1443515/files/LCD-2011-024.pdf

[2] http://rd51-public.web.cern.ch/RD51-Public/Activities/Documents/WG5SRS.pdf

ANNEX: GLOSSARY

Acronym	Definition
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
CPLD	Complex Programmable Logic Devise
ESS	European Spallation Source
FPGA	Field Programmable Gate Array
PGA	Pin Grid Array
QPF	Quad Flat Package
XFEL	X-ray Free Electron Laser