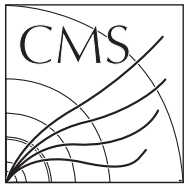
Available on CMS information server

CMS CR -2018/279



The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

15 October 2018 (v6, 11 February 2019)

Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities

Davide Ceresa, Alessandro Caratelli, Jarne Theo De Clercq, Dena Giovinazzo, Mykyta Haranko, Jan Kaplon, Kostas Kloukinas, Jan Murdzek, Simone Scarfì on behalf of the CMS Tracker Group.

Abstract

The first prototype of the full-size, full-functionality Macro Pixel ASIC has been produced in a 65 nm technology employing radiation tolerant techniques. It is a pixel readout ASIC designed for the Phase-2 upgrade of the CMS Outer Tracker detector. It features novel on-chip particle discrimination capabilities allowing for real-time event-driven readout of high transverse momentum particles at a 40 MHz rate. This data flow is complemented with a zero suppressed triggered readout data path for the readout of full events at a maximum rate of 1 MHz. This contribution presents the functional and performance evaluation results obtained from silicon prototypes.

Presented at *TWEPP2018 Topical Workshop on Electronics for Particle Physics*

PROCEEDINGS OF SCIENCE

Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities.

Davide Ceresa[*a†], **Alessandro Caratelli**[ab†], **Jarne Theo De Clercq**[c], **Dena Giovinazzo**[d], **Mykyta Haranko**[e], **Jan Kaplon**[a], **Kostas Kloukinas**[a], **Jan Murdzek**[a], **Simone Scarfì**[ab] **on behalf of the CMS Tracker Group.**

[a] *European Organization for Nuclear Research (CERN), Geneva, Switzerland.*
[b] *Microelectronic System Laboratory (LSM), École polytechnique fédérale de Lausanne (EPFL), Lausanne, Switzerland.*
[c] *Vrije Universiteit Brussel, Brussel, Belgium.*
[d] *UCSC, Santa Cruz, California, USA.*
[e] *Deutsches Elektronen-Synchrotron, Hamburg, Germany.*

E-mail: Davide.Ceresa@cern.ch, Alessandro.Caratelli@epfl.ch

The first prototype of the full-size, full-functionality Macro Pixel ASIC has been produced in a 65 nm technology employing radiation tolerant techniques. It is a pixel readout ASIC designed for the Phase-2 upgrade of the CMS Outer Tracker detector. It features novel on-chip particle discrimination capabilities allowing for real-time event-driven readout of high transverse momentum particles at a 40 MHz rate. This data flow is complemented with a zero suppressed triggered readout data path for the readout of full events at a maximum rate of 1 MHz. This contribution presents the functional and performance evaluation results obtained from silicon prototypes.

Topical Workshop on Electronics for Particle Physics
17 - 21 September 2018,
KU Leuven - Campus Carolus, Antwerpen, Belgium

*Speaker.
†Main authors

1. Introduction

The Macro Pixel ASIC, namely MPA, is a 65 nm CMOS technology pixel readout chip featuring on-chip real-time particle discrimination with trigger-less and zero suppressed readout. The design is dedicated to the hybrid Pixel-Strip (PS) module of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC). The trigger-less readout is based on transverse momentum (p_T) particle discrimination and it works in parallel with a triggered and zero suppressed readout with a programmable latency (up to 12.8 µs at 40 MHz event rate) which provides the entire event with a maximum trigger rate of 1 MHz.

The pixel matrix features macro-pixels of $100 \times 1446\,\mu m^2$ distributed in 118×16 channels. These dimensions fulfil the CMS Outer Tracker requirements [1]. The front-end, which consists of a pre-amplifier with Krummenacher feedback for detector leakage compensation, a shaper and a two stages discriminator with hysteresis, features a binary readout. The latter, followed by particle cluster reduction (clustering) and zero suppression, provides 3.8 Gbps to the particle discrimination logic. This digital logic block combines the front-end data with the external data coming from 8 parallel links for a total input bandwidth of 2.56 Gbps. The output of the particle discrimination logic is the high-p_T information that is continuously sent to the experiment back-end with 5 parallel links per chip for an output bandwidth of 1.6 Gbps. In parallel, a radiation tolerant Static RAM (SRAM) stores the full zero-suppressed event and provides it over a separated 320 Mbps serial link only when requested with an external trigger signal.

One of the main challenges for this design is the power consumption. The CMS Outer Tracker application requires a power density $< 90\,mW/cm^2$ for the entire chip (digital, analog and I/O). Consequently, the MPA is a Multi-Supply Voltage (MSV) design to strongly limit the digital power consumption without affecting the analog front-end performance. It contains three different power domains: digital, analog and I/O. The nominal digital power supply voltage is 1.00 V in order to decrease the power consumption, while the nominal analog and I/O power supply voltages are 1.2 V to avoid performance degradation. In addition, core logic presents a Multi-V_T design to locally reduce power consumption or improve performance. Furthermore, memory and clock gating are extensively used in the design. A full description of the chip design can be found in [2]. The purpose of this contribution is to present the functional and performance evaluation results obtained from the first full-size and full-functionality ASIC prototype.

2. Electrical characterization

The MPA was submitted for production and the first batch was available at the beginning of the 2018. A custom test set-up was developed to test and characterize the MPA. It includes a mezzanine board holding the chip, an interface board for voltage, current generation and monitoring, a custom-FPGA board developed at CERN, namely FC7 [3], and a command line interface program running on a Linux PC. The characterization was performed using the internal test capacitors (C_c, one per pixel) in a bare chip, without connection to a sensor. The quantity of charge injected is determined by the relationship $Q_i = C_c \cdot V$, where V is the voltage determined by the on-chip calibration DAC. A wire-bond pad allows the measurement of several bias points. For instance, the measurement of the calibration DAC voltage provides a Least Significant Bit (LSB)

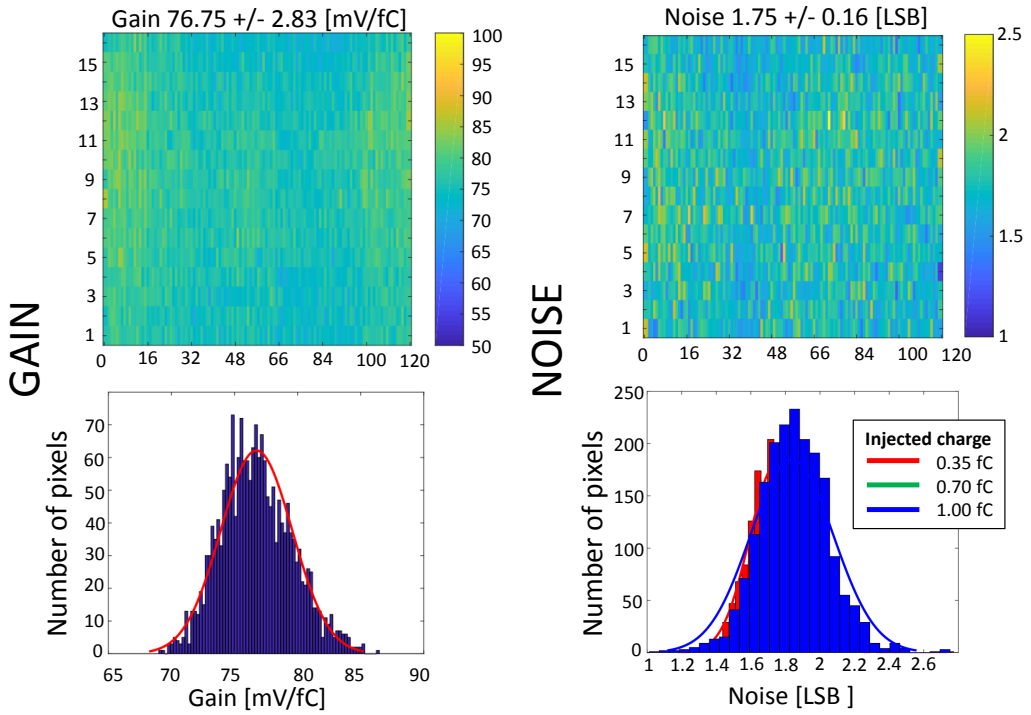


Figure 1: Single chip measurement of gain (left) and noise (right) distribution across pixel array.

value of 0.035 fC when an ideal value of 20 fF is assumed for C_c and an Integral Non-Linearity (INL) <0.5 LSB. Power consumption measurements confirm the simulation values, in particular the analog front-end shows a consumption of $\sim$28 µA per channel which results in a total power consumption of 67 mW. The digital logic, powered at 1.0 V consumes $\sim$91 mW, while the SLVS transmitters and receivers at the maximum bias current consume $\sim$26 mW. Summing these three contributions, a total power consumption without input activity of $\sim$184 mW is measured. As expected, input activity increases the digital logic power consumption: the increase, with the CMS Outer Tracker expected occupancy, is limited to <5 % and therefore the MPA fullfils the power requirement of <200 mW per chip.

2.1 Front-end characterization

The analog front-end of the MPA was already tested in a reduced size prototype, namely MPA-Light [4]. The only modification with respect to the previous version is the introduction of Enclosed Layout Transistor (ELT) in the input stage. This technique should reduce the increase of noise due to radiation (see section 2.2).

The measurements presented in the following paragraph are obtained on a single bare die. The front-end gain can be calculated from the differences among the average thresholds for different input charges. As shown in figure 1, the measured gain is 76.75 ± 2.83 mV/fC with a uniform distribution in the matrix. Gain variation impacts the overall mismatch and noise which need to be evaluated. A 5-bits threshold-equalization DAC per pixel allows to correct for the pixel-to-pixel threshold mismatch. The achieved noise free r.m.s threshold variation after equalization is 1.6 LSB ($\sim$171 e^-) as shown in figure 2. The Equivalent Noise Charge (ENC) distribution is shown in

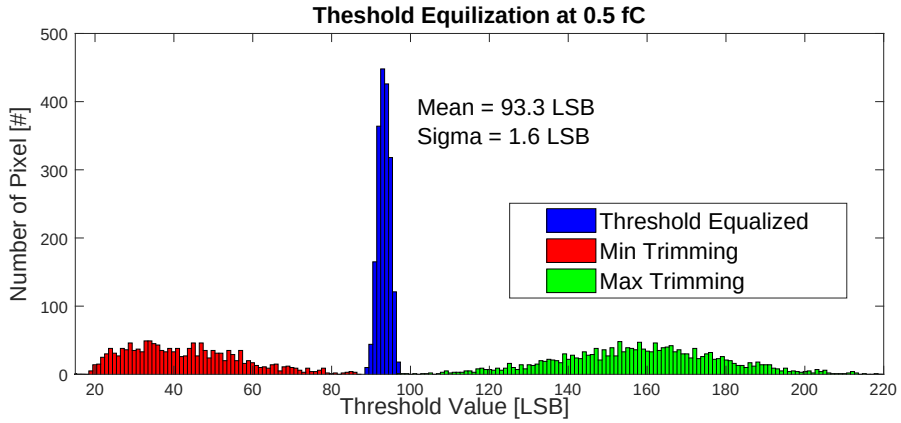


Figure 2: Red and green histograms show the threshold distribution for a not equalized MPA (with all the threshold-equalization DACs set to the minimum or to the maximum value); the blue histogram shows the same distribution in the calibrated matrix for a threshold of 0.5 fC: $\pm$ 1.6 Threshold DAC LSB $\sim$171 e^-.

figure 1 and provides an r.m.s value of $\sim$1.75 LSB ($\sim$188 e^-). The ENC does not depend on the charge injected and does not show any dependency on the location in the pixel array. The minimum detectable charge can be calculated by quadratically adding the measured electronic noise and the threshold variation after equalization. The quadratic sum of mismatch and noise is $\sim$2.4 LSB ($\sim$254 e^-). After threshold equalization, the 6σ minimum threshold could be set at $\sim$14.4 LSB ($\sim$1540 e^-) which is well below the nominal threshold of 0.5 fC ($\sim$3121 e^-).

The binary readout allows for timing characterization of the analog front-end. Charge injection time scans for different threshold values provide the shaper output shown in figure 3. The peaking time is 25 ± 1.1 ns as expected from simulation. An important parameter to ensure correct operation at 40 MHz is the front-end time walk. It is measured as the difference between charge injection time and detection by the edge detector in the front-end. In figure 3, a maximum time walk of $< 14 \pm 1.1$ ns over a charge range from 0.5 to 8 fC is measured with the threshold set at 0.5 fC.

Analog performances show also a good chip-to-chip uniformity, 90 % of the chips show a variation lower than than +/- 10 % from the average values obtained over 500 measured ASICs. In conclusion, the characterization of the front-end provides results very close to simulations and very similar to the MPA-Ligth prototype despite a 40 $\times$ increase in pixel array size.

2.2 Total Ionization Dose irradiation results

The MPA is expected to be exposed to a maximum Total Ionizing Dose (TID) of 56 Mrad. Considering more than a 2 $\times$ safety factor, the prototype was exposed to X-rays up to 150 Mrad with a dose rate of 1.5 Mrad/hour. During the entire procedure, the test system monitored power consumption, front-end performance and digital logic. As shown in figure 3, at 150 Mrad the analog current consumption variation was -8.5 %, while the IO consumption decreased with less than 3.0 %. The digital logic test consisted in pass/failure checks at different doses which did not show any failure during the entire irradiation, while its power consumption increased of less than 2.0 %. Minor degradations were observed on the analog blocks: all the DAC LSB variations were contained below -10 % at 150 Mrad. As shown in figure 3, the measured ENC increased in the

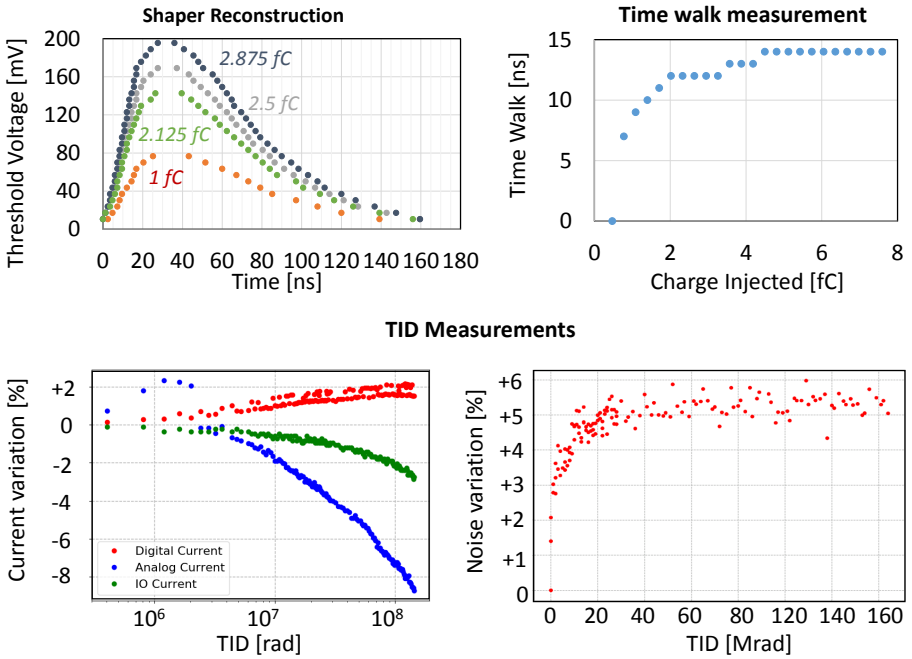


Figure 3: Top: Shaper output for different input charges (left) and Time walk (right) for nominal threshold (0.5 fC). Bottom: Current consumption variation with TID (left). Noise increase with TID (right).

first part of the irradiation and saturated after 20 Mrad for a total increase $<+6\,\%$. This result, compared with the +20 % of the MPA-Light, proves the effectiveness of the ELT at the input stage. In conclusion, the MPA did not show any problem with X-ray TID irradiation up to 150 Mrad.

3. Summary

The MPA chip has been designed using a commercial 65 nm CMOS technology with a macro pixel cell of $100 \times 1446\,\mu m^2$. The digital logic for quick recognition of high transverse momentum particles was included and performed as expected. Front-end characterization with test pulses matched simulations closely, with a pixel-to-pixel threshold spread of 171 e^- r.m.s. after equalization, an ENC of 188 e^- r.m.s., a peaking time of 24 ns and a time walk <15 ns. Irradiation with X-rays up to 150 Mrad did not show any problem. Power consumption is lower than 200 mW per chip and respects the very strict CMS Outer Tracker requirements.

References

[1] CMS Collaboration. *Technical proposal for the Phase-2 upgrade of the Compact Muon Solenoid*, CERN-LHCC-2015-010 / LHCC-P-008.

[2] D. Ceresa et al. *Macro Pixel ASIC (MPA): The readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC*, 2014 *JINST* 9 C11012

[3] M. Pesaresi et al. *FC7 AMC for generic DAQ control applications in CMS*, 2015 *JINST* 10 C03036

[4] D. Ceresa et al. *A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC*, 2016 *JINST* 11 C01054.