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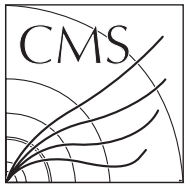

The Compact Muon Solenoid Experiment

Conference Report

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Characterization of the first prototype of the Silicon-Strip readout ASIC (SSA) for the CMS Outer-Tracker phase-2 upgrade

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Abstract

The silicon strip readout ASIC (SSA) for the CMS Outer Tracker PS module was prototyped in a $65\,nm$ CMOS technology and characterized utilizing a custom made test bench based on the FC7 μTCA FPGA card. The ASIC has been evaluated and characterised under different working temperatures and radiation levels up to $200\,Mrad$. Measurements show a front-end gain between 35 and $54\,mV/fC$ and an average noise of $< 330\,e^-$, meeting the specification of noise performance. The measured peaking time for an injected charge between $0.5\,fC$ and $8\,fC$ is $\approx 19\,ns$ allowing to detect consecutive particle events in combination with the zero dead-cycle binary readout. The embedded trimming circuit allows to obtain a measured threshold spread smaller than $55\,e^-$ between channels. The measured power consumption is $\approx\ 60\,mW$ and thus within the strict power budget of the PS modules. The performance characterization results and radiation tolerance test results of the first SSA silicon prototype are presented.

Presented at *TWEPP2018 Topical Workshop on Electronics for Particle Physics*

PROCEEDINGS OF SCIENCE

Characterization of the first prototype of the Silicon-Strip readout ASIC (SSA) for the CMS Outer-Tracker phase-2 upgrade

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The silicon strip readout ASIC (SSA) for the CMS Outer Tracker Pixel-Strip (PS) module was prototyped in a 65 nm CMOS technology and characterized utilizing a custom made test bench based on the FC7 µTCA FPGA card. The ASIC has been evaluated and characterised under different working temperatures and radiation levels up to 200 Mrad. Measurements show a front-end gain between 35 and 54 mV/fC and an average noise of $< 330\,e^-$, meeting the specification of noise performance. The measured peaking time for an injected charge between 0.5 fC and 8 fC is ≈ 19 ns allowing to detect consecutive particle events in combination with the zero dead-cycle binary readout. The embedded trimming circuit allows to obtain a measured threshold spread smaller than $55\,e^-$ between channels. The measured power consumption is ≈ 60 mW and thus within the strict power budget of the PS modules. The performance characterization results and radiation tolerance test results of the first SSA silicon prototype are presented.

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1. Introduction

For the High Luminosity CMS Outer Tracker upgrade [1], the PS module is required to handle higher data-rates and readout bandwidths together with enhanced functionality compared to the current tracker, while keeping the Level-1 (L1) trigger rate at an acceptable level (< 1 MHz) in the high pileup conditions of the HL-LHC. For this reason, the Outer Tracker detector modules will introduce the capability to perform on-detector fast recognition of interesting events by locally rejecting low transverse momentum particles and transmit for every event encoded information of high momentum particles to the L1 trigger decision electronics. To facilitate the on-detector particle momentum discrimination, the Outer Tracker Pixel-Strip (PS) modules adopt a double layer sensor topology which combines a pixel silicon sensor with a strip silicon sensor..

The SSA, whose architecture is described in [2], is the 120-channel, Silicon Strip readout ASIC of the Outer Tracker PS module. It generates, in real time, the hit cluster coordinates necessary for the correlation with the information coming from the pixel layer that is readout by the Macro-Pixel ASIC (MPA) [3]. It stores full events in an embedded radiation-tolerant memory for a latency period of 12.8 µs. Full events are transmitted up to a average trigger rate of 1 MHz. More details of the PS module readout architecture can be found in [4]. The SSA ASIC incorporating already all the required functionality and performance characteristics for operation in the final readout system, has been prototyped for the first time using a 65 nm CMOS technology. Radiation tolerant design techniques were employed to mitigate Single Event Effects as well as Total Ionizing Dose effects for operation in the radiation environment of the HL-LHC CMS Tracker.

A custom setup was developed to test and characterize the ASIC based on an FC7 µTCA FPGA card [5] followed by a custom made interface board for voltage level translation, supply control and monitoring purposes. The ASIC, that in the final application will be flip-chipped on the tracker front-end hybrids, is instead wire-bonded on a PCI-E mezzanine board to facilitate the ASIC characterization under radiation sources or ion beams. Custom FPGA firmware and software routines have been developed based on the µDTC CMS data acquisition (DAQ) framework.

2. Functional tests and parameters characterization

The front-end channel was characterized with the use of the calibration circuit. The ASIC implements a self-injection circuitry: each channel input is connected with 52 fF calibration capacitor to a common chopper circuit through a switch controlled by the channel configuration registers, allowing to inject a known charge into the front-end channel input. The amplitude of the voltage step is controlled by an 8-bit DAC supplying the current to a 4.6 KΩ resistor. A strobe signal, generated by the fast-command decoder, allows to trigger the charge injection. The pulse duration is controllable by configuration, a 6-bits delay line (DL) allows to select the injection timing. In the field application the SSA will synchronously transmit pre-elaborated and encoded information to the experiment back-end electronics. To allow for calibration and for characterization of the prototype the ASIC implements a 15-bits asynchronous ripple counter per-channel connected to the low-threshold discriminator output. More details on the implementation can be found in [2].

By scanning the threshold DAC, the charge injection time and the sampling clock phase, it is possible to study the front-end response. Figure 1 shows the reconstruction of the signal at the output of the shaper circuit for a single channel for different values of injected charge. The mea-

sured average peaking time is around 19.3 ns ± 1.6 ns, as expected from the simulation. The charge threshold values are controlled at chip level thanks to the DACs located in the SSA periphery. Due to the on-chip mismatch and variability, the actual threshold can differ between channels. Figure 2b shows the number of events counted for an injected charge of 1 fC and for different values of the threshold DAC (S-Curves). The effective threshold evaluated as the middle point of the curve shows a standard deviation of $< 600\,e^-$ for a non calibrated ASIC. This value proves to be within the range that the SSA front-end can compensate. Indeed, a 5-bits threshold-equalization DAC per strip allows to correct for the strip-to-strip threshold mismatch, even if no sensor is connected. Figure 2a shows the distribution of the effective threshold before and after the trimming procedure where a $\sigma < 55\,e^-$ can be achieved. By evaluating the threshold for different values of the injected

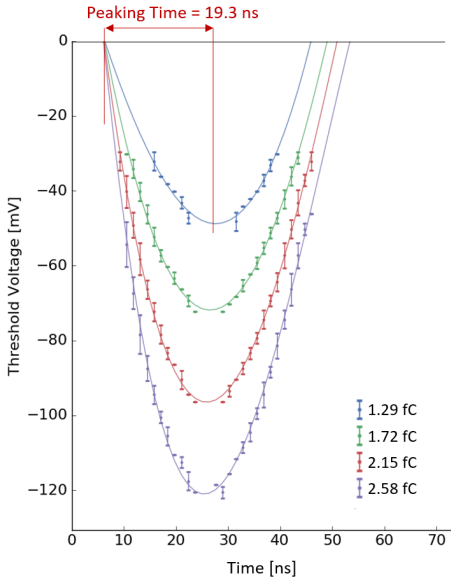

Figure 1: Reconstruction of the shaper circuit output-pulse for a single channel.

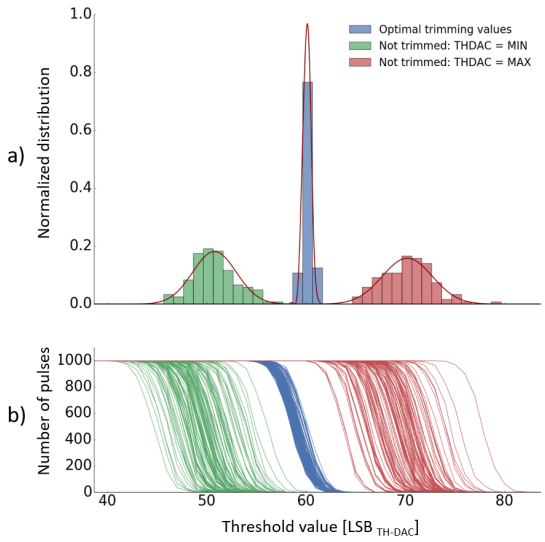

Figure 2: On-chip distribution of the effective channel threshold due to strip-to-strip threshold mismatch, before and after trimming procedure.

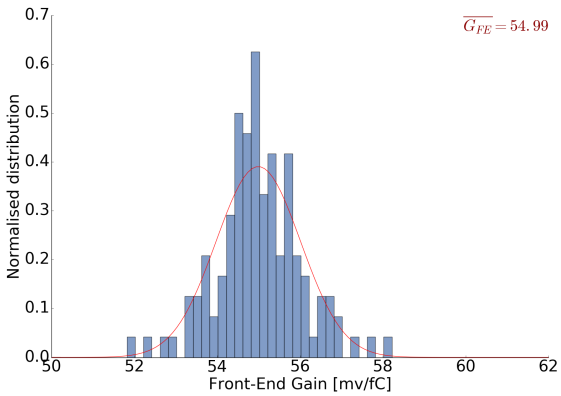

Figure 3: Analog Front-End Gain measured distribution across the SSA

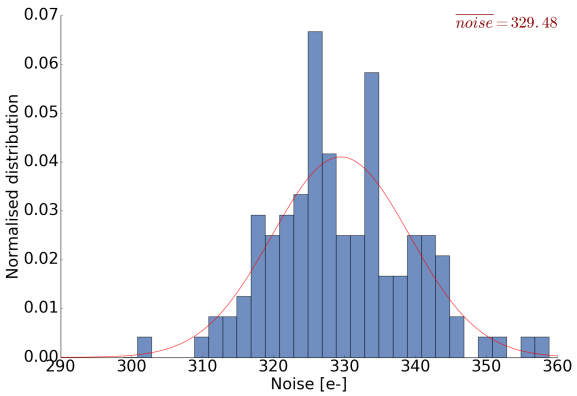

Figure 4: Distribution of the channel noise (ENC) measured across the SSA

charge it was possible to extract the analog Front-End gain (G_A) for each SSA channel. Figure 3 shows the on-chip distribution of the gain for a not-trimmed ASIC. A 5-bit trimming DAC per channel allows to reduce the standard deviation of the G_A to < 1 mV. The average G_A measured on the prototype is ≈ 54 mV/fC, in agreement with the simulation results.

The standard deviation of the inverse error function fitting the S-Curves close to the threshold value allows to evaluate the front-end noise. For a non irradiated SSA operating at 25 °C the average noise measured on the silicon prototype is $< 330 \pm 10\,e^-$ in agreement with the simulation assuming no capacitance at the input. Figure 4 shows the channel noise distribution across the ASIC. The minimum detectable charge evaluated as the quadratic sum of mismatch and noise is therefore equivalent to $< 355\,e^-$. In the target application with 5 pF sensor input capacitance, simulation results estimate an average of ENC of $\approx 900\,e^-$ fulfilling the application requirements.

3. Total Ionizing Dose characterization

The SSA employs radiation tolerant design techniques for Total Ionizing Dose (TID) and Single Event Upset (SEU) tolerance. The first SSA prototype was tested up to a total dose of 200 Mrad. The triggered readout and the continuous transmission of cluster centroids together with all the digital functionality integrated in the SSA did not show any failure during irradiation.

Figure 5 shows the effective threshold distribution across the ASIC before and after irradiation at 25°C. A shift in the measured mean value and an increased σ(up to $\approx 0.9\,LSB_{THDAC}$ of the threshold distribution is observed. This effect is related to the variation of the bias of the threshold DAC and of the charge injection. The dynamic range of the bias DACs and of the channel trimming DACs allows to compensate for this error. The red histogram in Figure 6 shows the threshold distribution of the irradiated ASIC after repeating the calibration procedure. As shown in Figure 6, the effect is almost negligible when the irradiation of the ASIC is performed at −30°C (temperature of the cooling system in the target application). As presented in in Figure 7, a ≈20% increase of the average channel noise was measured on the ASIC irradiated at room temperature. This effect is due to the convolution of the decrease of the channel gain, the reduction of the biasing currents of the analog front-end and of the increase of the flicker and thermal noise in the pre-amplifier input

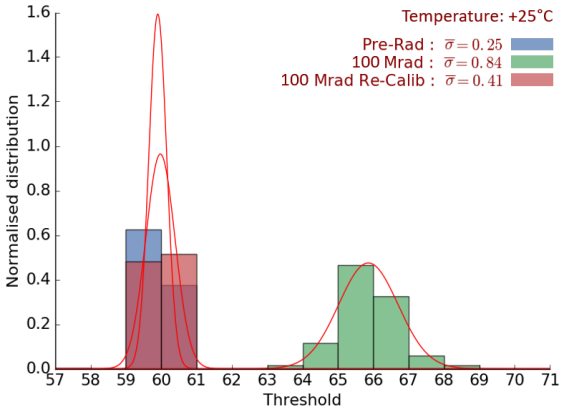

Figure 5: Distribution of the channel threshold value before and after irradiating at 25°C

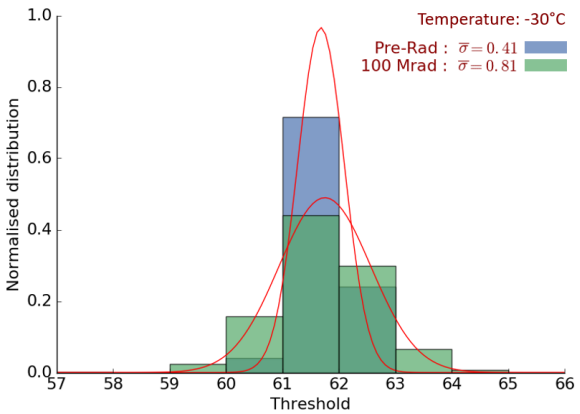

Figure 6: Distribution of the channel threshold value before and after irradiation at −30°C

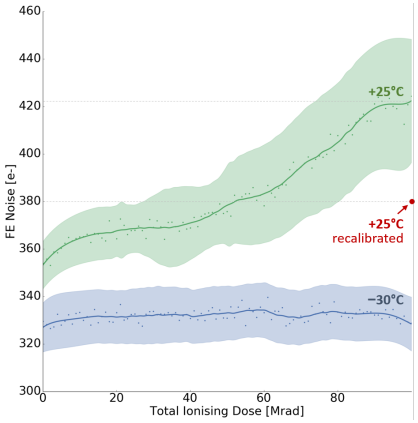

Figure 7: Front-End ENC respect to the total dose at $+25\,^{\circ}\mathrm{C}$ and at $-30\,^{\circ}\mathrm{C}$

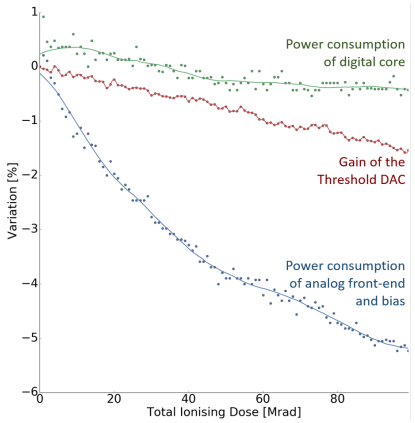

Figure 8: Variation of the analog and digital power consumption and of the Th-DAC Gain respect to TID

stage. By recalibrating the SSA bias block it is possible to evaluate the actual noise increase due to the front-end which results $<9\%$. A variation of $<1\%$ in the digital core power consumption and of up to $\approx 6\%$ for the analog front-end current was observed during irradiation. Figure 8 shows their percent variation up to 100 Mrad. The internal bang-gap reference voltage shows a very week dependency on the radiation dose.

4. Summary

The first full size, fully functional SSA ASIC was designed in a 65 nm CMOS technology. The characterization of the digital functionality and analog front-end performance of the silicon prototype shows results in agreement with the simulation. The shift of the parameters with a total ionizing dose up to 100 Mrad are within the range that can be compensated by the embedded calibration circuits.

References

[1] CMS Collaboration *et al.*, "The phase-2 upgrade of the CMS tracker," tech. rep., CERN-LHCC-2017-009, CERN, Geneva Switzerland,[CMS-TDR-17-001], 2017.

[2] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, Y. Leblebici, J. Murdzek, and S. Scarfi, "Short-Strip ASIC (SSA): A 65nm silicon-strip readout ASIC for the Pixel-Strip (PS) module of the CMS Outer Tracker detector upgrade at HL-LHC," *PoS*, vol. TWEPP-17, p. 031. 5 p, 2018.

[3] D. Ceresa, J. Kaplon, R. Francisco, A. Caratelli, K. Kloukinas, and A. Marchioro, "A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC," *Journal of Instrumentation*, vol. 11, no. 01, p. C01054, 2016.

[4] D. Ceresa, A. Caratelli, J. Kaplon, K. Kloukinas, and S. Scarfi, "Readout architecture for the Pixel-Strip module of the CMS Outer Tracker Phase-2 upgrade," *PoS*, vol. Vertex2016, p. 066, 2017.

[5] M. Pesaresi, M. B. Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis, "The FC7 AMC for generic DAQ & control applications in CMS," *Journal of Instrumentation*, vol. 10, no. 03, p. C03036, 2015.