Ultrascale+ for the new ATLAS calorimeter trigger board dedicated to jet identification

Bruno Bauss, Andrea Brogna, Volker Büscher, Reinhold Degele, Holger Herr, Christian Kahra, Stefan Rave, Elena Rocco, Ulrich Schäfer, Jan Schäffer, Julio Souza*, Duc Bao Ta, Marcel Weirich

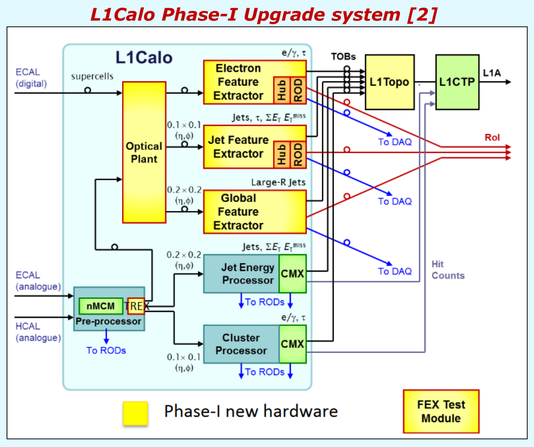
ATLAS Trigger And Data Acquisition Phase-I Upgrade

The ATLAS experiment [1], one of the multi-purpose detectors at the LHC, has planned a major detector upgrade for the Phase-I [2] period (from 2021 to 2026) to adapt data readout capabilities for increased beam intensity up to an instantaneous luminosity of 2.5 × 10^{34} $cm^{-2}s^{-1}$.

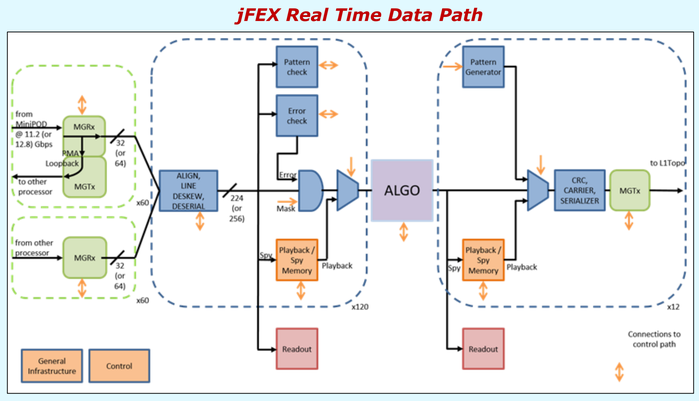
A significant part of this upgrade is related to the Level 1 Calorimeter Trigger (L1Calo), which uses data from the calorimeters to reconstruct different physics objects for the trigger selection. In order to exploit the fine granularity readout with a trigger rate at up to 100 kHz, a new system of Feature EXtractors will be used for trigger selection. There are three dedicated module types: electron FEX (eFEX), jet FEX (jFEX) and global FEX (gFEX).

During the commissioning phase of the new system, the legacy trigger is going to be kept, to be later retired.

L1Calo Phase-I Upgrade system [2]



jFEX Real Time Data Path



The Jet Feature Extractor (jFEX) has been conceived to identify small/large area jets, large area tau leptons, missing transverse energy and the total sum of the transverse energy. The use of the latest generation of the Xilinx Virtex Ultrascale+ FPGAs (Field Programmable Gate Array), is dictated by the physics requirements which include a significant processing power and an enormous input bandwidth, up to ~3Tb/s, within a latency budget of less than 390 ns.

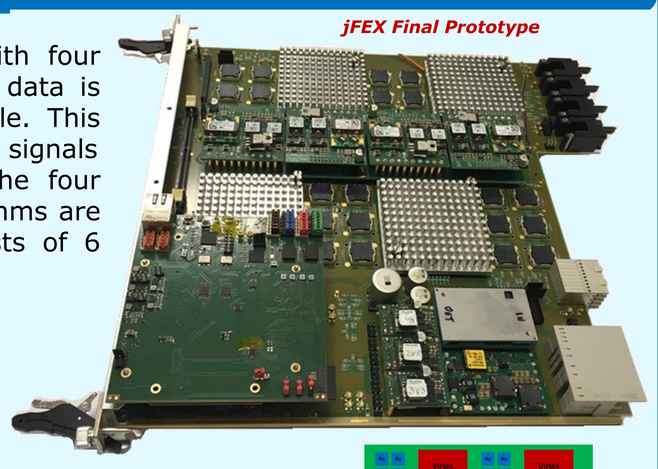
[1] ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST 3 (2008) S08003
[2] ATLAS TDAQ System Phase-I Upgrade Technical Design Report url: https://cds.cern.ch/record/1602235

Hardware Overview

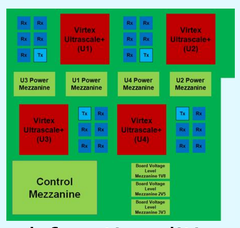
The jFEX is an ATCA board equipped with four Xilinx Virtex Ultrascale+ FPGAs. All input data is received via 240 optical fibres per module. This information is then converted into electrical signals via Avago miniPODs and directed into the four processor FPGAs, where the trigger algorithms are applied. In total, the jFEX system consists of 6 boards.
The main features of the board are:

- Modular design
  - 4 equal "blocks" FPGA & miniPODs
  - Independent power supplies per FPGA
- FPGA part number XCVU9P-2FLGA2577E
  - 240 optical inputs @ 11.2 Gbps
  - 48 optical outputs @ 12.8 Gbps
  - 24 MiniPODs (optical module): 20 Rx + 4 Tx
  - 186 IO lines per processor (8 banks)
- Data sharing between FPGAs
  - 2x29 Multi-gigabit transceivers per FPGA pair

jFEX Final Prototype



Simplified diagram of the jFEX board



In order to gain in flexibility for future board changes, the board control functionalities are located on a mezzanine card. This philosophy allows a smooth and reliable way of upgrading control functions and components without affecting the main board.
The main functionalities of the Control Mezzanine are:

jFEX Control Mezzanine

- Host jFEX control FPGA
  - Carrier card for the Avnet PicoZed
    - Equipped with Zynq XC7Z030
- IPBus master
- Hosts the MasterSPI configuration circuitry for processors and control FPGAs
- Clock cleaning and distribution to processor FPGAs with the Si5345
- Monitoring and slow control
- Trigger Timing Control (TTC) data reception and distribution to processor FPGAs

The design strategy based on mezzanines is also used on the power distribution for the voltage rails with current consumption higher than 3 A, which use switching regulators. Two different designs are used on the jFEX, both based on the TDK iJX series (iJA (I_{outmax}= 35 A) and iJB (I_{outmax}= 60 A)):

- The DC/DC converters for the FPGA voltage rails V_{CCINT} (0.85 V), $V_{MGTAVCC}$ (0.9 V) and $V_{MGTAVTT}$ (1.2 V) are populated on the so called FPGA PWR Mezzanine.
  - One mezzanine per FPGA, four per jFEX
- The Board PWR Mezzanine supplies the board level voltages 2.5 V and 3.3 V, so as the FPGA rail V_{CCINT_IO} (1.8 V).
  - Total of three per board

FPGA PWR Mezzanine

Board PWR Mezzanine

That approach allowed great flexibility during the prototype phase, as the DC/DC converters first tests and optimization could be performed without the main board. Additionally, the risks of damaging the hardware in case of faults (i.e. short circuits) on the PCB manufacturing or assembly process, was reduced.

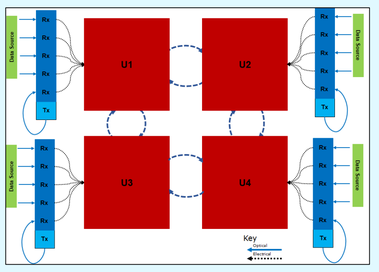
The FPGA current consumption requirements are based on Xilinx Power Estimator and on Vivado Power Estimator

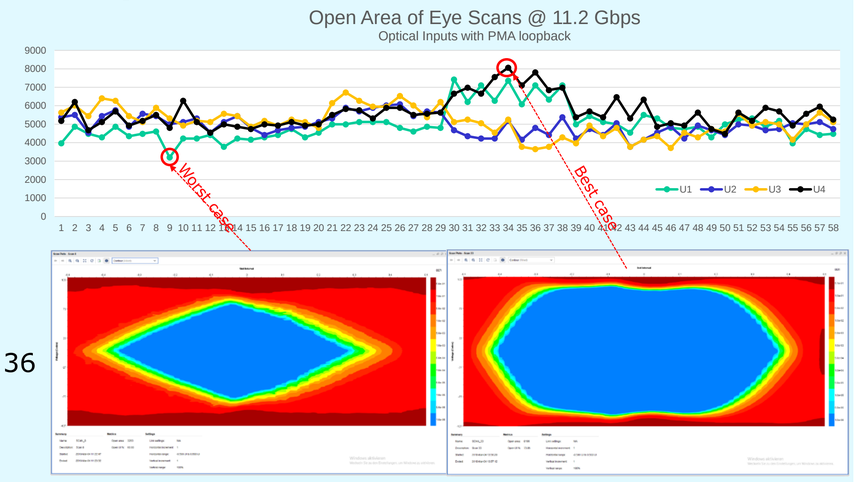
Hardware Characterization

The jFEX prototype was produced in November 2017 and extensively tested during the last 12 months. The tests were mainly focused on the power consumption, ripple measurement on the MGTs power pins, thermal dissipation, Multi-Gigabit Transceivers reference clock quality and validation of the optical inputs and parallel IOs.

Validation of all optical inputs

Setup used for testing all 240 input fibres simultaneously

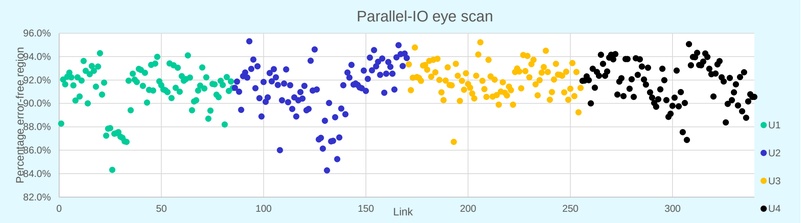




- Long term test: over 36 hours
  - BER < $1x10^{-15}$
- NO ERRORS!!!

Validation of parallel IOs

- 186 lines on each processor @ 1000 Mbps
  - One half of the lines used as transmitter, the other half as receiver
- 1000 Mbps chosen as line rate for measurement purpose (eye scan)



- Performing eye scan with IDELAY blocks (count mode) on receiver side for each line
  - Scan resolution 2.1 - 12 ps (512 taps)
  - Very good results: data eyes open 84-95 %

Power consumption and thermal dissipation

Current consumption of the jFEX with all Multi-Gigabit Transceivers enabled from PMBus

Supply	Voltage Rail	Current (A)	Temp. (°C)
Board Level Voltages	1V8	0.47	32.00
	2V5	14.55	0.00
	3V3	7.42	30.00
U1	$V_{CCINT\ (0.85V)}$	23.75	44.00
	$MGTYAV_{CC\ (0.9V)}$	10.95	46.00
	$MGTYAV_{TT\ (1.2V)}$	20.42	52.00
U2	$V_{CCINT\ (0.85V)}$	20.41	36.00
	$MGTYAV_{CC\ (0.9V)}$	10.75	39.00
	$MGTYAV_{TT\ (1.2V)}$	20.43	45.00
U3	$V_{CCINT\ (0.85V)}$	17.17	38.00
	$MGTYAV_{CC\ (0.9V)}$	10.45	43.00
	$MGTYAV_{TT\ (1.2V)}$	20.14	48.00
U4	$V_{CCINT\ (0.85V)}$	18.82	38.00
	$MGTYAV_{CC\ (0.9V)}$	10.73	39.00
	$MGTYAV_{TT\ (1.2V)}$	20.21	45.54
Total (W)			265.86

Current estimation calculated by Vivado

Current Estimation Vivado (A)	
$MGTYAV_{CC\ (0.9V)}$	10.326
$MGTYAV_{TT\ (1.2V)}$	22.111

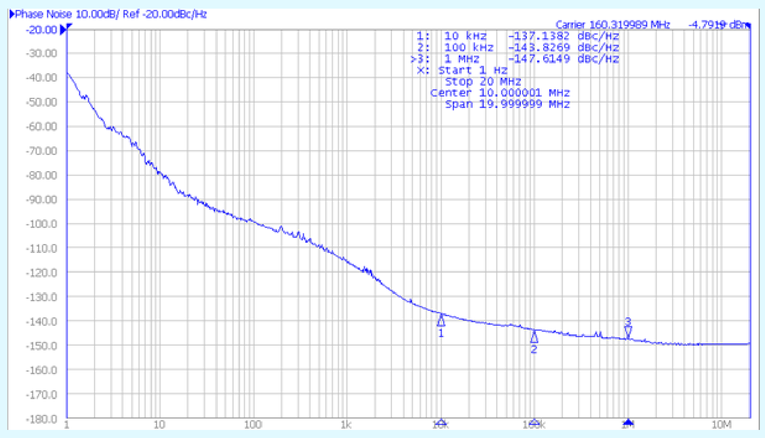
- Current consumption measured is consistent with Vivado estimations

Thermal picture of the jFEX final prototype in the crate. Confirmation of no thermal issues

XADC	
FPGA	Temp. (°C)
U1	85.2
U2	71.3
U3	56.3
U4	64.3

- FPGA internal temperatures are within the Xilinx specs

Clock Jitter Measurement



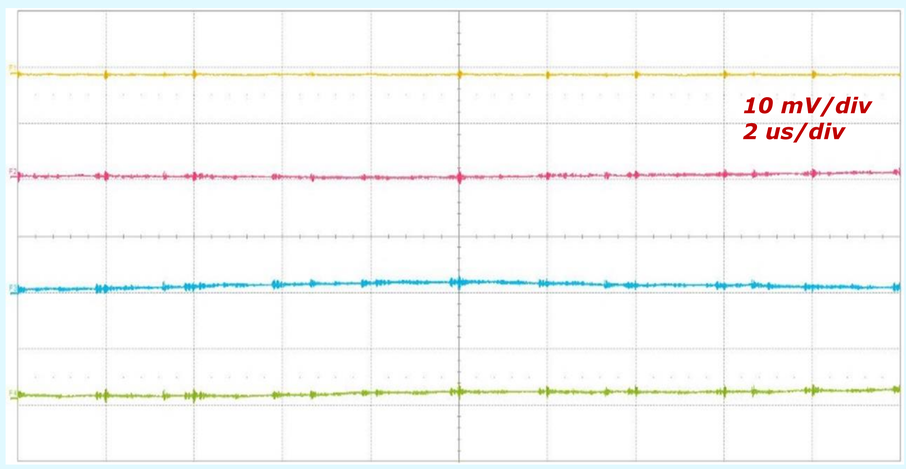
Phase noise measurement with Spectrum Analyzer

Offset Frequency	Xilinx Specs	jFEX Measurements
10 kHZ	-112 dBc/Hz	-137.14 dBc/Hz
100 kHz	-128 dBc/Hz	-143.83 dBc/Hz
1 MHz	-145 dBc/Hz	-147.615 dBc/Hz

- Phase Noise values for the MGT reference clock are within the Xilinx Specs!!!

Ripple Measurement for MGT $V_{MGTAVTT}$

Ripple measurement of the $V_{MGTAVTT}$ with a bandwidth <80 MHz



Values <10mV so within the Xilinx Specs

MGTYAVTT (1.2V)	
U1	2.136 mV
U2	6.999 mV
U3	7.606 mV
U4	8.394 mV

- Oscilloscope setup AC coupling with external 50 ohm termination
- Timescale 2 us/div
- MGT voltage rails specification (UG578): "The noise at the power pins should be less than 10 mVpp over the band from 10 kHz to 80 MHz"

Conclusion

The jFEX prototype board has been delivered in November 2017. The board has been extensively and successfully tested over the last 12 months

A pre-production module, with no hardware changes with respect to the prototype, is currently being manufactured and is expected to be delivered before the end of 2018.
The final jFEX modules are expected to be installed on the ATLAS detector before the end of 2019

2018 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC)
*Email:julio.souza@cern.ch – Address for correspondence:Institut für Physik, Universität Mainz, Staudingerweg 7, 55128 Mainz, Germany