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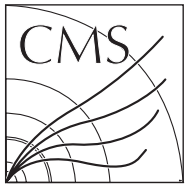

The Compact Muon Solenoid Experiment

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A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase-2 Upgrades

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Abstract

The foreseen Phase-2 upgrades at the LHC present very challenging requirements for the front-end readout electronics of the CMS Outer Tracker detector. High data rates in combination with the employment of a novel technique for rejecting locally low transverse momentum particles as well as the strict low power consumption constraints require the implementation of an optimized readout architecture and specific interconnect synchronization schemes for its components. This work focuses on the development and the verification of the Concentrator IC (CIC) ASIC, a 65 nm digital chip featuring high input and output data rates, in the context of the readout chains incorporating all front-end ASICs: namely the Macro Pixel ASIC (MPA), Short Strip ASIC (SSA) for the Pixel-Strip (PS) modules and the CMS Binary Chip (CBC) for Strip-Strip (2S) Modules. The CIC ASIC receives high data rate (320 MHz) digital streams from eight Front-end ASICs via a total of 48 differential lines and transmits them through seven differential lines operating at 320 MHz or 640 MHz, depending on the occupancy of the detector module. A complex system level simulation environment based on the System-Verilog hardware description language and on the Universal Verification Methodology (UVM) platform has been adapted and extended to help the CIC development and verification simulating the complete readout chains from the particle event to the output of the modules. The paper is composed of four sections: the first one describes the p_{T} module concept, the second presents the UVM environment for MPA/SSA ASICs adapted and extended to include the CIC, the third one shows the UVM environment for the 2S module (a CBC emulator has been developed) and the last section presents the PS module efficiency as a function of the stub occupancy for different CIC output frequencies.

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PROCEEDINGS OF SCIENCE

A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase-2 Upgrades

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The foreseen Phase-2 upgrades at the LHC present very challenging requirements for the front-end readout electronics of the CMS Outer Tracker detector. High data rates in combination with the employment of a novel technique for rejecting locally low transverse momentum particles as well as the strict low power consumption constraints require the implementation of an optimized readout architecture and specific interconnect synchronization schemes for its components. This work focuses on the development and the verification of the Concentrator IC (CIC) ASIC, a 65 nm digital chip featuring high input and output data rates, in the context of the readout chains incorporating all front-end ASICs: namely the Macro Pixel ASIC (MPA), Short Strip ASIC (SSA) for the Pixel-Strip (PS) modules and the CMS Binary Chip (CBC) for Strip-Strip (2S) Modules. The CIC ASIC receives high data rate (320 MHz) digital streams from eight Front-end ASICs via a total of 48 differential lines and transmits them through seven differential lines operating at 320 MHz or 640 MHz, depending on the occupancy of the detector module. A complex system level simulation environment based on the System-Verilog hardware description language and on the Universal Verification Methodology (UVM) platform has been adapted and extended to help the CIC development and verification simulating the complete readout chains from the particle event to the output of the modules. The paper is composed of four sections: the first one describes the p_{T} module concept, the second presents the UVM environment for MPA/SSA ASICs adapted and extended to include the CIC, the third one shows the UVM environment for the 2S module (a CBC emulator has been developed) and the last section presents the PS module efficiency as a function of the stub occupancy for different CIC output frequencies.

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1. CMS Outer Tracker readout chains description

For the CMS Outer Tracker Upgrade [1] two different p_{T} modules will be used: namely the PS module and the 2S module. Both modules are composed of two closely (few mm) spaced silicon sensors. The particle trajectories are bent by the high magnetic field (3.8 T). Correlating the information from the two layers allows to evaluate the incident particle transverse momentum (p_{T}). High-p_{T} particles, above a certain threshold, are more interesting for the scope of the research. The pairs of hits in the two sensors of a module, called stubs, are sent out synchronously at 40 MHz to be analyzed, and kept in a memory for 12.6 μs waiting for the Level-1 (L1) trigger decision. In Figure 1 a cross section of the PS module/2S module is shown. The readout of the two sensor layers is done by 16 SSAs [2] and 16 MPAs [3] in the PS module and by 16 CBCs [4] in the 2S module. To reduce the module output bandwidth a concentrator chip has been developed, namely the CIC. The CIC objective is to perform stub data averaging over space (8 FE-Chips) and time (8 BX). Each CIC receives data at 320 MHz from 8 Front-End (FE) chips (MPA or CBC):

- 40 lines (5 from each FE-Chip) for stub data sent out synchronously at each Bunch Crossing (BX) for the L1 trigger decision. For this reason raw data are kept in a memory for a maximum latency of 12.6 μs waiting for the L1 trigger signal;
- 8 lines (1 from each FE-Chip) for full sensor data only when a L1 trigger is received. The maximum L1 trigger frequency is 750 KHz.

The FE-Chips and CIC clock and fast commands are provided at the module level by the Low-power GigaBit Transceiver (LpGBT) ASIC [5] operating as a serializer at the module output and sending out data via the optical fiber. The CIC ASIC is mostly a digital chip, but it incorporates 12 phase aligners (analog blocks) in order to sample properly the incoming data streams. A custom System-Verilog model emulates the operation of the phase aligner. Each CIC can be configured for different output flavors. According to the supplied clock it can use a data output frequency of 320 or 640 MHz (this is valid both for stub data and L1 raw data). In addition, only for stub data, it can be configured via I^2C to use 5 or 6 lines in the output, and to transmit information related to the particle curvature in the CMS magnetic field, or instead to use the available bandwidth to provide a larger number of stub coordinates. This approach allows to optimize the system in terms

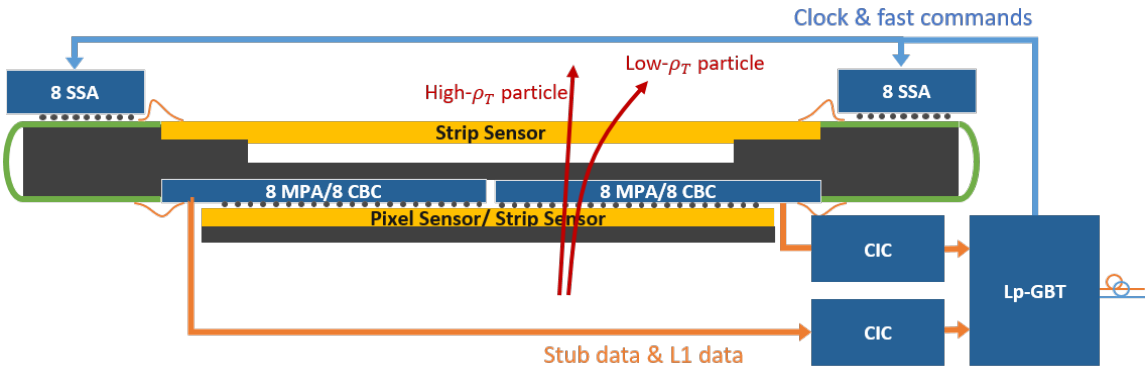

Figure 1: PS module/2S module cross section.

of power budget and bandwidth requirements with respect to the module position within the CMS Outer Tracker.

2. UVM framework for PS module readout chain

An existing UVM framework has been adapted and extended to add the CIC ASIC to the MPA/SSA simulation environment [6] in order to complete the PS module readout chain. In Figure 2 a functional block diagram of the UVM framework for the PS module chain is shown. The framework uses a modular approach. The Design Under Verification (DUV) is represented by the PS module ASICs composed of a configurable number of MPAs and SSAs (up to 16) plus 1 or 2 CICs. It is possible to run the simulation on the DUV RTL code to verify the implemented algorithm or on the DUV final netlist with back-annotated delays. The latter case has a more realistic timing and allows to verify the post-layout ASICs operation in all the process corners and to generate activity information for accurate power analysis taking into account all the parasitics. To verify the DUV an ideal behaviour of the readout chain is described (in System-Verilog language) in a block called Reference model. Both the DUV and the Reference model receive the same configuration from the Configuration block (I^2C master), fast commands (from the T1 generation block), and particle hit information signals. These can be either from the Monte Carlo generation block, based on real physics data-sets containing event samples for the entire CMS Outer Tracker, or from the Stub generation block, which creates randomized hits that emulate high transverse momentum particles, representing the main primitives expected to be identified in the CMS Outer Tracker. Moreover, a third block called Combinatorial generation has been developed to create randomized hits with a uniform distribution to emulate detector noise. It can be added on top of the stub generation or be used separately. In the UVM environment these are considered to be the simulation stimuli. Each block composing the environment is described as a UVM Verification

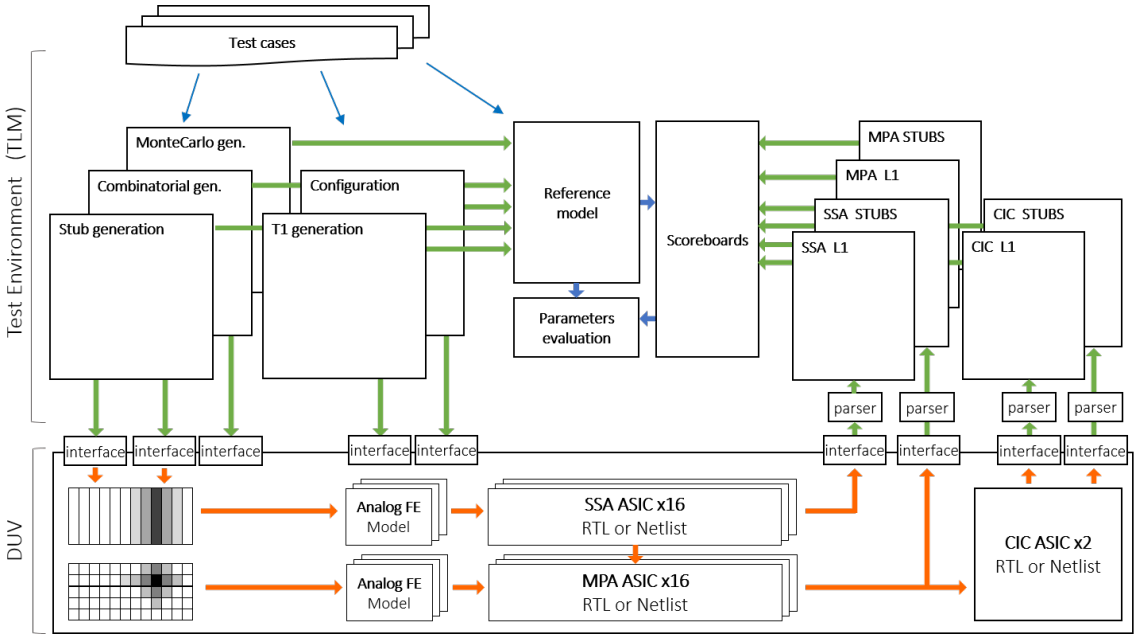

Figure 2: PS module (MPA, SSA, CIC) readout chain.

Component (UVC) and connected to the DUV via interfaces. UVM makes large use of Transaction Level Modeling (TLM). The data flow in and out of different components is done via special ports called TLM interfaces. At the output of the DUVs, signals are parsed via interfaces and converted to data packets to be compared at a higher level of abstraction with predicted output from the reference model. This comparison is carried out via another UVC called Scoreboard. There is a dedicated scoreboard for each ASIC. Thanks to this approach it is possible not only to find mismatches at run time between the DUV and the reference model, but also to know if these mismatches are related to an ASIC hardware limitation (for instance the ASIC reaching the bandwidth saturation or the transmitting FIFOs being full) or a bug in the RTL code. In the latter case the ASIC that is failing can be detected thanks to the display of output data from the reference model and the DUV. Moreover, a report for each ASIC is created at the end of the simulation summarizing the total number of data packets processed from the DUV. In this way the single ASIC efficiency and the total readout chain efficiency for the particle recognition can be computed. The verification environment allows to perform clock-cycle accurate behavioral simulations. While this framework is stable, the user can change the above mentioned stimuli by applying different test cases chosen from the developed test library. Several test cases have been developed to stress and verify all functionalities of all the ASICs in the system.

3. UVM framework for 2S module readout chain

The CIC ASIC functionality was also verified in the context of the 2S module using the same UVM environment. Due to the lack of a CBC model, it was necessary to develop a CBC emulator and CBC driver based on the CBC documentation and prototype characterization [4]. The 2S module UVM framework is based on the same concepts explained before, with some modifications concerning the hit generation constraints, because in this case two strip sensors have to be read out by the same CBC ASIC. The DUV in this framework is composed of the CIC only. Consequently, the reference model and the scoreboard have been developed for this specific case only for the CIC ASIC. Different Test cases have been developed to verify some important CIC features, like the L1 data CBC sparsification (cluster compression) that is performed at the CIC level, and the phase alignment and word alignment that have to be tested at system level because specific CBC training patterns are required while performing I^2C operations in the CIC. This environment has been developed to obtain the full verification coverage of the CIC model.

4. CIC performance evaluation

Applying two different test cases it is possible to simulate the CIC working at two different output frequencies. The scoreboard, thanks to the UVM environment, allows to perform efficiency studies on the complete readout chain. For instance, Figure 3 shows efficiency results from simulations of the PS module readout chain: it is noticeable from this plot that the MPA (blue line) has minimal losses, while a drop in CIC efficiency is expected at higher stub occupancy when the CIC output frequency is set to 320 MHz. This drop has been estimated to be around 40 % at the maximum expected stub occupancy. In the other test case doubling the CIC output bus frequency to 640 MHz, and consequently the bandwidth, these limitations are overcome and the readout chain works as expected with an efficiency close to 100 % (green line). The green area represents the

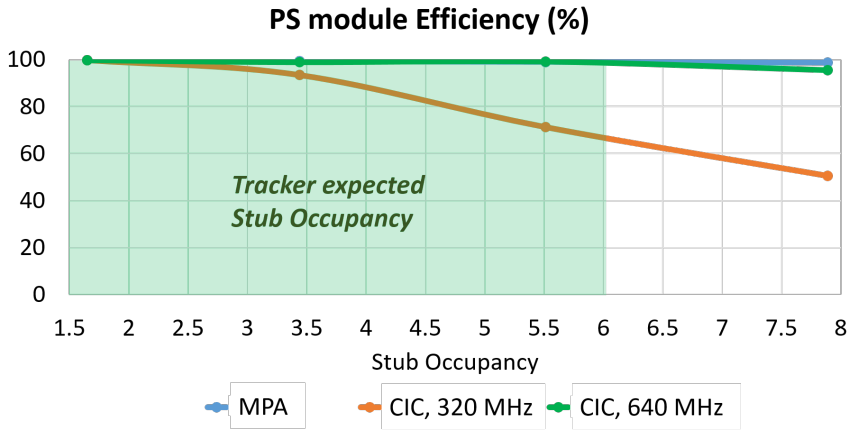

Figure 3: PS module efficiency at the MPA output and CIC output for two different output frequencies.

CMS Outer Tracker expected stub occupancy. Therefore, depending on the position of the PS module in the tracker, it will be needed to configure it properly to find a good trade-off between power budget and data bandwidth.

5. Conclusions

A system level simulation environment has been developed in order to simulate the entire PS module and 2S module readout chains to extract ASIC efficiencies for different test cases, perform Monte Carlo analysis, and to verify the final version of each ASIC in the complete readout chain. In the case of the 2S module, a behavioral model of the CBC ASIC was developed to enable the simulation of the readout chain and the verification of the CIC ASIC. The simulation environment was extensively used.

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