Utopia: A Nine Decade Femtoampere Sensitivity Current Digitizer and Its Application in Ionizing Radiation Monitoring

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***Abstract*— Radiation measurements and monitoring are very important for particle physics accelerators, hadron therapy institutes, and nuclear facilities. An Application Specific Integrated Circuit (ASIC) able to digitize current generated from ionization chambers was designed and characterized in order to be used as the front-end of the new radiation monitoring system at CERN. The design of the Utopia 2 ASIC was motivated by the need to measure input currents as low as 2 fA and over a wide dynamic range of 9 decades. This paper presents the challenges, the design procedure, the architecture, and the measurement results of the front-end that was fabricated in AMS 0.35-μm technology. The main limitation was related to the leakage currents that are injected into the input of the ASIC from various sources and are added to the signal of the detector. By active leakage current compensation, the ASIC can measure current down to 1 fA, and by introducing a multiple range architecture, the ASIC can digitize current up to 5 μA.**

***Index Terms*— Active leakage current compensation, current-to-frequency converter (CFC), femtoampere current sensing, femtoamperes (fA), leakage currents, radiation monitoring.**

I. Introduction

RADIATION monitoring is important and a legal obligation for particle physics accelerators. In that respect, the European Organization for Nuclear Research (CERN) has to comply with the relevant legislation for radiation protection and environmental monitoring. The public and personnel should be protected from any unjustified exposure to ionizing radiation. The radiation levels should be constantly monitored to guarantee that the required dose limits are not exceeded [1], [2]. The output signal of the existing radiation detectors used at CERN, which are mainly commercial ionization chambers [3], [4], is a current that is proportional to the energy deposited by the incident radiation [5], [6].

The readout circuit should be able to digitize currents that span over nine decades of dynamic range. The required specifications are strict due to the need to measure even the natural background radioactivity for the environmental monitoring, so the minimum current that the digitizer should sense can be as low as 2 fA. The measurement range starts from 50 nSv/h to 0.1 Sv/h. The Sv unit is equal to 1 Sv = 1 J/kg and represents the equivalent biological effect of the deposit of a joule of radiation energy in a kilogram of human tissue. When measuring with a specific chamber [7] whose conversion factor for neutrons is equal to $4 \cdot 10^{-8}$ A/Sv/h, the output current range starts from 2 fA up to 4 nA. Additionally, in extreme cases, due to the existence of pulsed radiation fields [8], the output current can reach the maximum value of 5 μA. The specifications for the readout electronics are shown in Table I [9]. The required measurement time is equal to 100 ms. However, at the lower end of the current spectrum, longer acquisition times can be tolerated due to the lower level of radiation. For 1 fA, an acquisition time of 100 s is acceptable. The ASIC will be used for radiation monitoring for radiation protection and not for beam loss monitoring, hence such a long measuring time is not an issue.

TABLE I
Required Specifications

Measurement Range	2 fA to 5 μA
Resolution	1 fA
Accuracy	1 fA + 5% of the reading
Measurement Time	T_w= 100 ms for $I_{in} \geq$ 1 pA 100 s $\leq T_w \leq$ 100 ms for 1 fA $\leq I_{in} \leq$ 1 pA
Temperature	-15°C to 55°C
Power Consumption	$<$ 10 mW

The scope of this paper is the design and characterization of an application specific integrated circuit (ASIC) that can digitize input currents from 1 fA up to a few μA. The design of the front-end ASIC for radiation monitoring is challenging due to the wide dynamic range requirements, the accuracy constraints, and the lowest measurable current that can be as low as 1 fA. This paper presents the design procedure, the guidelines that were followed, and the measurement results of the Ultralow Picoammeter 2 (Utopia 2) ASIC.

II. State of the Art and Demonstrator ASIC

There are many examples of CMOS ASICs that are used in hadron therapy institutes, particle accelerators, or beam loss

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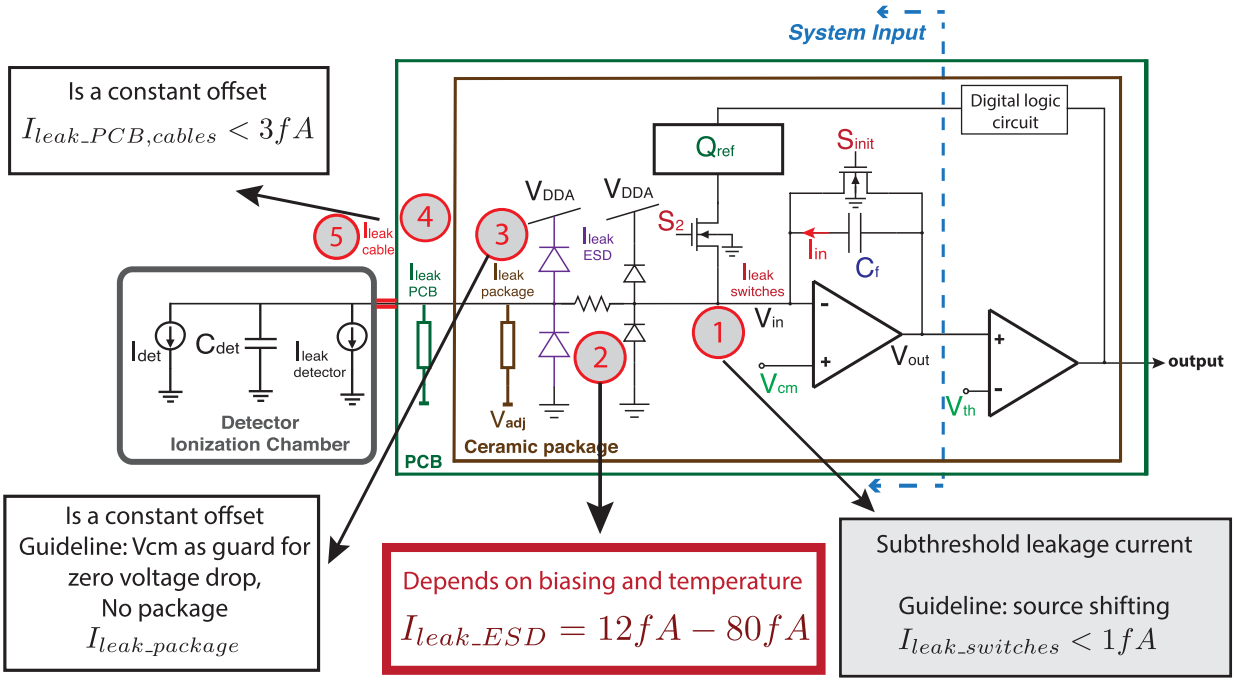

Fig. 1. Leakage currents at the input of the demonstrator Utopia 1 ASIC.

monitoring systems [10]–[13]. These works mostly aim at extending the measuring current dynamic range to the upper end in order to cope with higher radiation doses [14], [15]. On the other hand, the minimum current that they can measure is dominated by the sum of the leakage currents. The main limitation in measuring current down to the femtoampere range is the various leakage currents and their variation due to temperature.

A. Technology Selection

The various leakage current mechanisms for a transistor are, namely, the reverse bias p-n junction leakage, the subthreshold leakage, the oxide tunneling leakage, the gate-induced drain leakage (GIDL), and the channel punchthrough current [16]–[18]. The technologies that were initially considered for the ASIC development were 0.35-μm, 0.18-μm, and 0.13-μm. These technologies were compared in terms of subthreshold leakage current and substrate leakage of a single device [19]. Radiation hardness was not required by the specifications for this development, since the system should be used for radiation protection and is not supposed to be used in harsh radiation environments. Finally, the AMS 0.35-μm technology was selected among the others because of its lowest leakage current behavior. A demonstrator ASIC named Utopia 1 was built in AMS 0.35-μm, to experimentally verify the selected technology and evaluate the contribution of each leakage current source present at the input of the measuring system [20], [21].

B. Guidelines for Femtoampere Current Measurements

The demonstrator's architecture was based on a current-to-frequency converter (CFC) exploiting a charge balancing technique [22], [23]. The recycling integrator is the best way to evaluate the total integrated dose over time and it provides good linearity over a wide dynamic range with no charge loss. Based on a simple CFC architecture, four channels were built with slight variants in their inputs and compared with a reference channel, in order to quantify the contribution of the leakage currents [24], [25].

The schematic of the front-end input and the results of the characterization of the Utopia 1 ASIC in terms of leakage current are shown in Fig. 1. The current I_{in} that is integrated in the input capacitor C_f includes the detector signal I_{det} and the sum of the leakage currents. The potential sources of leakage current that contribute to the net leakage current include: 1) the leakage current of the input switches; 2) the leakage current of the Electrostatic Discharge (ESD) protection diodes; 3) the leakage current of the package; 4) the leakage current of the printed circuit board (PCB); and 5) finally the leakage of the cables and the connectors. The different voltage adjacent to the measuring input pin can lead to a voltage drop that creates a leakage current that is added to the package leakage current noted as (3) [26].

The characterization of the Utopia 1 ASIC provided a list of guidelines that can be used in systems that perform femtoampere current measurements. These guidelines are summarized in Fig. 2 and were used for the design of the Utopia 2 ASIC.

The leakage current of the switches in AMS 0.35-μm technology when $V_{GS} = 0$ is dominated by the subthreshold leakage current [17], [27]. According to the EKV model, the subthreshold leakage current in the OFF-state is given by (1) [28], [29]

$$I_D = I_{\text{spec}} \exp \frac{-(V_{T0} + \text{nV}_{\text{SB}})}{nU_T} \cdot \left[1 - \exp \frac{-V_{\text{DS}}}{U_T}\right] \quad (1)$$

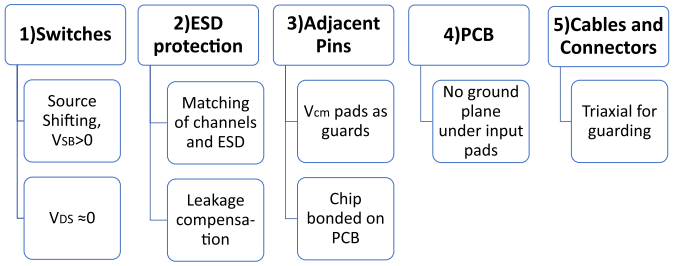

Fig. 2. Guidelines used in a femtoampere sensitivity ASIC design.

where I_{spec} is the specific current of the transistor, V_{T0} is the threshold voltage, n is the slope factor, U_T is the thermal voltage, and V_S, V_D, and V_B are the source, the drain, and the bulk voltages. The specific current is given by (2), where β is the transfer parameter that depends on the W/L ratio of the channel, μ is the equivalent mobility of electrons in the channel, and C_{ox} is the gate oxide capacitance per unit area

$$I_{\text{spec}} = 2n\mu C_{\text{ox}} \frac{W}{L} U_T^2 = 2n\beta U_T^2. \tag{2}$$

For a single transistor connected to the input, the subthreshold leakage current due to ion implantation in AMS 0.35-μm technology can be as large as 10 pA [27]. Equation (1) shows that the leakage current of the switches can be decreased by both/either increasing V_{SB} voltage (that is explained as the source voltage shifting technique in [27] and [30]–[32]) or by keeping V_{DS} voltage as close as possible to 0 V. Measurements of the Utopia 1 ASIC demonstrated that after source shifting, the $I_{\text{leak\_switches}}$ decreased below 1 fA [25], [33].

The leakage current of a p-n junction depends on the junction geometry area and perimeter and the doping concentration. When using the standard foundry cells that include the ESD diodes, their leakage current is affected by temperature and by biasing. The measured leakage current of the ESD protection diodes proved to vary from 12 to 80 fA according to the environmental temperature. This is the reason why an active leakage current compensating architecture is proposed for the Utopia 2 design [26]. The compensating method will be explained in detail in Section III that presents the architecture of the Utopia 2 ASIC.

Regarding the extrinsic leakage current sources, the leakage current of the package, and the leakage of the adjacent pins can be regarded as a constant offset. The chip can be directly bonded on the PCB without any ground plane under the input sensitive nodes to eliminate leakage coming from the package. Additionally, the pads adjacent to the input pads can be driven internally to the voltage of the non-inverting input of the integrator so that there will not be any voltage drop across the inputs. The same guard signal principle can be extended all the way up to the detector by using triaxial cables and connectors.

The leakage of the PCB was measured with the demonstrator to be below 3 fA and can be compensated. The PCB should be placed inside a metallic shield box to limit the interference from the external sources and the chip should be properly shielded due to the light sensitive ESD protection diodes. Finally, the analog and the digital padrings should be separated. It should be noted that dirt on the PCB traces can act as a conductive medium that increases the stray leakage currents, so proper cleaning is a prerequisite for such sensitive measurements.

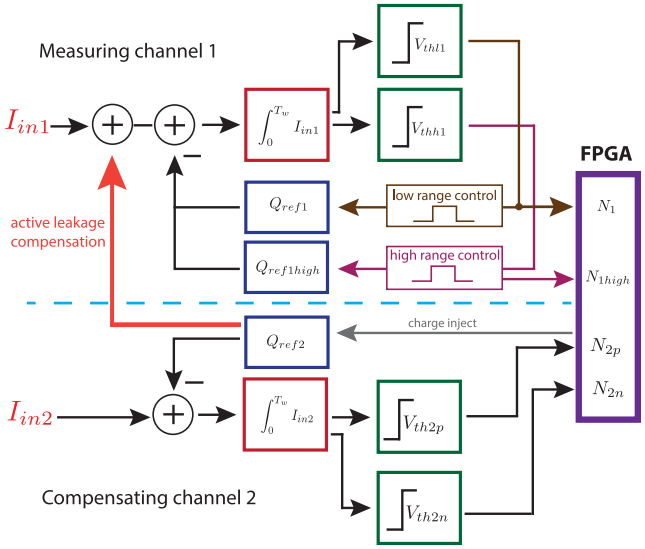

Fig. 3. Utopia 2 ASIC block diagram.

III. Architecture of the Utopia 2 ASIC

The CFC operating principle was already evaluated with the demonstrator. The input current I_{in1} is integrated on a feedback capacitor C_{f1} and the generated output voltage ramp is compared with a determined voltage threshold V_{thl1} using a comparator. When that threshold is crossed, a monostable triggers the injection of a fixed amount of charge, Q_{ref1}, which balances the charge that is integrated in the feedback capacitor. As long as the integrator's output remains above the threshold, the monostable of the low range alternates between charging and discharging phases and controls the discharging circuit operation. The average current can be calculated by counting the number of charge injections in a defined time window T_w [33].

The measuring channel and the compensating channel are shown in Fig. 3. The basic building blocks of the integrators, the comparators, and the reference charge circuits along with the low- and high-range digital controls can be identified in this block diagram.

A. Femtoampere Range

The dominant source of leakage current in the input of the front-end proved to be the ESD protection. To compensate the variation of the leakage current of the p-n junctions due to temperature and humidity changes, an active leakage current compensation scheme has been implemented. A second channel replicates the input structures of the measuring channel 1, measures only the net leakage current, and subtracts it automatically from the measuring channel input. The ESD protection devices and the input switches should be designed matched. Channel 2 operates like channel 1 but it integrates

only the net input leakage current I_{in2}. The reference charge circuit of channel 2 can inject negative or positive charge that is equal to Q_{ref2} according to the polarity of the measured leakage current. Channel 2 measures only the leakage current and this is the reason why the charge Q_{ref2} is scaled to $Q_{\text{ref1}}/10$ to measure faster and provide finer granularity. The detector current after the active compensation is given by (3)

$$I_{\text{det}} = \frac{N_1 Q_{\text{ref1}} + \rho(N_{2p} - N_{2n}) Q_{\text{ref2}}}{T_w} \tag{3}$$

where N_1 is the number of charge injection cycles of the low reference charge Q_{ref1} and N_{2p} and N_{2n} are the number of times that the second channel's integrator output crosses the positive current or the negative current thresholds, respectively. T_w is the selected measuring time window and ρ is the calibrated ratio of the leakage currents $I_{\text{leak\_in1}}/I_{\text{leak\_in2}}$ of the two channels. In most cases, the leakage current is expected to be either positive or negative, so either N_{2n} or N_{2p} will be zero. The ratio ρ has to be extracted during the leakage current calibration procedure because due to mismatches and non-idealities, it can slightly differ from $\rho = 1$.

When the input current is below 1 pA, the measuring time window that was set at $T_w = 100$ ms has to be increased. Similarly, consecutive T_w can be added and the charge that is accumulated in the C_f will finally provide a non-zero count. The increase in the measuring time is related to the nature of the CFC architecture. By increasing the measurement time, the resolution of the system increases.

B. Microampere Range

The maximum current that has to be measured is given by (4) and is equal to $I_{\text{max}} = 5\ \mu$A

$$I_{\text{max}} = \frac{Q_{\text{ref}}}{t_{\text{cycle}}} \tag{4}$$

where Q_{ref} is the reference charge and $t_{\text{cycle}} = t_{\text{charge}} + t_{\text{discharge}}$ is the period of operation of the two phases of the discharging circuit that are managed by a monostable and some non-overlapping clocks.

In order to be able to cover the dynamic range of nine decades and measure up to 5 μA, the reference charge Q_{ref} has to be adjusted since the t_{charge} and $t_{\text{discharge}}$ pulses should be long enough to allow the formation and delivery of a precise Q_{ref} at the input of the integrator.

A second discharging circuit that can balance charge equal to Q_{ref1high} is added and is connected in parallel to the low-range discharging circuit that can inject charge equal to Q_{ref1}. The total reference charge that is injected to the input is equal to the sum of the reference charge of the two ranges Q_{ref1} and Q_{ref1high}. The high-range discharging circuit is automatically activated after the crossing of a higher threshold V_{thh1} set by another comparator. Finally, the maximum current of 5 μA can be measured when $t_{\text{cycle}} = 100$ ns and $Q_{\text{ref1}} + Q_{\text{ref1high}} = 500$ fC. The second range is activated for input current that is above 1 μA. The high-range control circuit that is connected to the Q_{ref1high} discharging circuit is shown in Fig. 4. The signal that activates the high-range discharging circuit when the high-range comparator

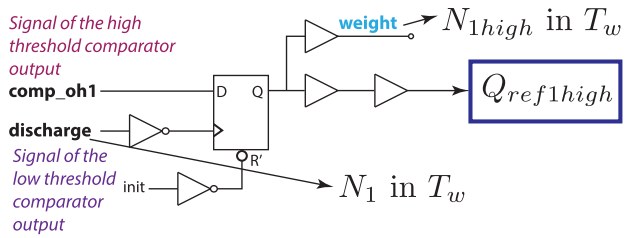

Fig. 4. High range control circuit.

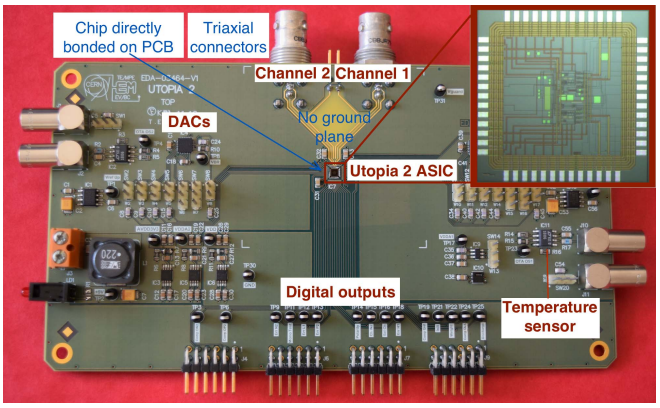

Fig. 5. Utopia 2 PCB and Utopia 2 ASIC.

"comp_oh1" is triggered due to the high input current is clocked according to the *"discharge"* signal that is the output of the low-range comparator. The *"weight"* that is the output of the second range is sent to the FPGA along with the *"discharge"* signal. This is how the total charge Q_{total} using the two ranges is injected in parallel. The Q_{ref1high} charge has to be properly calibrated as it will be explained later in order to avoid non-linearity in the conversion.

After the addition of the second range, the detector current can be calculated using (5), where N_{1high} is the number of charge injection cycles with both discharging circuits activated

$$I'_{\text{det}} = \frac{N_1 Q_{\text{ref1}} + N_{\text{1high}} Q_{\text{ref1high}} + \rho(N_{2p} - N_{2n}) Q_{\text{ref2}}}{T_w}. \tag{5}$$

IV. Circuit Design

The ASIC was designed in AMS 0.35-μm technology with a die size of 2.75 mm × 2.75 mm. The chip is pad limited and the block size is equal to 780 μm × 800 μm. The power consumption of the chip is equal to 8.25 mW. The PCB and the microscopic picture of the ASIC are shown in Fig. 5. All the presented guidelines that were defined during the Utopia 1 testing were also used in the Utopia 2 ASIC and measuring system. The ASIC was directly bonded on the PCB and triaxial connectors were used. The input pads with a voltage equal to V_{in} were surrounded by pads connected to the common mode voltage V_{cm} in order to limit any leakage due to different adjacent pins voltage.

A. Microelectronic Design

The reference charges Q_{ref1}, Q_{ref1high}, and Q_{ref2} that are very important for the conversion are implemented using stray

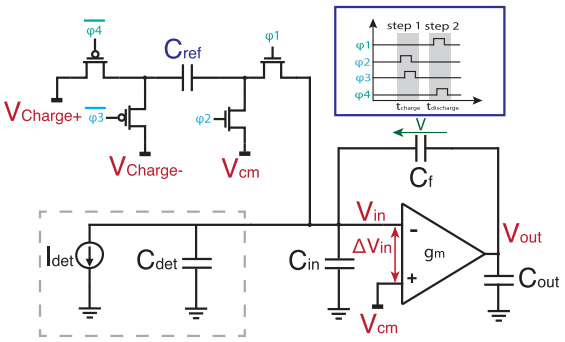

Fig. 6. Integrator with switched capacitor circuit and timing for charge subtraction.

insensitive switched capacitor circuits [34]. Fig. 6 shows the integrator with the switched capacitor circuit and the signals φ_1, φ_2, φ_3, and φ_4 generated from non-overlapping clocks that control the switches and are responsible for the charge injection [35]. The width of these signals is managed by a monostable and is related to the t_{cycle}.

In general, the reference charge Q_{ref} depends on the capacitor C_{ref} and the voltages $V_{\text{charge}+}$, $V_{\text{charge}-}$, V_{cm}, and V_{in}, and it is given by (6)

$$Q_{\text{ref}} = C_{\text{ref}}(V_{\text{ref}} - \Delta V_{\text{in}}) \tag{6}$$

where $V_{\text{ref}} = V_{\text{charge}+} - V_{\text{charge}-}$ and the difference ΔV_{in} is not equal to zero due to static and dynamic offsets. During the design phase, the target value for the dc offset was below 1% in order to have an impact of less than 1% on the Q_{ref}. The operational transconductance amplifier (OTA) was designed as a folded cascode OTA and was optimized in order to have a dc offset voltage $V_{\text{os}} < 5$ mV. Additionally, regarding the dynamic offset the OTA was optimized in terms of transconductance, so $g_m = 3$ mS [26]. Although the charge balancing principle is not affected by offsets, the design was optimized for low offset in order to minimize the possible drift due to temperature and aging between the two consecutive calibrations and improve the accuracy of the system. To minimize the effect of the charge injection and clock feedthrough of the switches of the switched capacitor circuits, minimum size nMOS switches were selected and connected to the input of the OTA. Finally, the solution regarding the non-ideal values of the capacitors is the calibration of the reference charges.

The summary of the Utopia 2 characteristics is presented in Table II and the selected design values in Table III [33].

B. Noise Considerations

The noise can be roughly expressed as the noise of the switching operation that includes the OTA noise and the noise of the switches of channel 1, the noise of the leakage current compensating channel 2, and the parallel noise that is injected into the input of both channels.

The sampled RMS noise voltage across a switched capacitor is equal to $\sqrt{kT/\text{Cref}}$ [36] and this has been also verified for Utopia 2 ASIC with simulations [33]. The sampled RMS noise charge for N counts is given by $Q_{n,\text{sc}} = \sqrt{2qU_T\text{NC}_{\text{ref}}}$, where $U_T = kT/q = 26$ mV. Using (7), the input-referred RMS noise current due to the switched capacitor operation across the C_{ref} in channel 1 can be derived from (8)

$$NC_{\text{ref}} = \frac{I_{\text{in}}T_w}{V_{\text{ref}}} \tag{7}$$

$$I_{n,\text{sc}} = \sqrt{2q\frac{U_T}{V_{\text{ref}}}\frac{I_{\text{in}}}{T_w}}. \tag{8}$$

Similarly, the noise due to the switched capacitor C_{ref2} in the compensating channel 2 is given by (9). The Q_{ref2} is used both for the operation of channel 2 and for the leakage current compensation in channel 1

$$I_{n,\text{comp}} = \sqrt{4q\frac{U_T}{V_{\text{ref}}}\frac{I_{\text{leak}}}{T_w}}. \tag{9}$$

The parallel noise can be considered to be dominated by the shot noise of the reversed-biased ESD protection diodes, the PSD of which is equal to $2qI_{\text{leak}}$ (A^2/Hz). Integrated over the time window T_w, the input-referred RMS noise value due to the contribution of the ESD diodes is equal to (10)

$$I_{n,\text{ESD}} = \sqrt{\frac{4qI_{\text{leak}}}{T_w}}. \tag{10}$$

Consequently, the total input-referred noise in the measuring channel 1 is given by (11) and finally the S/N by (12)

$$I_n = \sqrt{\frac{2q}{T_w}\left[\frac{U_T}{V_{\text{ref}}}(I_{\text{in}} + 2I_{\text{leak}}) + 2I_{\text{leak}}\right]} \tag{11}$$

$$S/N = \frac{I_{\text{in}}}{\sqrt{\frac{2q}{T_w}\left[\frac{U_T}{V_{\text{ref}}}(I_{\text{in}} + 2I_{\text{leak}}) + 2I_{\text{leak}}\right]}}. \tag{12}$$

TABLE II
SUMMARY OF UTOPIA 2 ASIC CHARACTERISTICS

Technology	AMS 0.35 μm
Power Supply	3.3 V
Power Consumption	8.25 mW
Die Size	2.75 mm x 2.75 mm
Number of Channels	2
Gain A_0 of OTA	76.4 dB
g_m of OTA	3 mS
GBW of OTA	430 MHz
Phase Margin ϕ	50 deg
V_{os} of OTA (3σ)	< 5 mV
Dynamic Range	1 fA to 5 μA
t_{cycle}	100 ns

TABLE III
DESIGN VALUES OF UTOPIA 2 ASIC

Channel 1	Channel 2
Q_{ref1}= 100 fC $Q_{ref1high}$= 400 fC	Q_{ref2}= 10 fC
C_{ref1}= 100 fF $C_{ref1high}$= 400 fF	C_{ref2}= 10 fF
C_{f1}= 1 pF	C_{f2}= 100 fF
V_{thl1}= 2.1 V	V_{thp2}= 1.9 V
V_{thh1}= 2.3 V	V_{thn2}= 2.1 V
V_{cm}= 1.5 V, $V_{charge+}$= 2.5 V, $V_{charge-}$= 1.5 V	

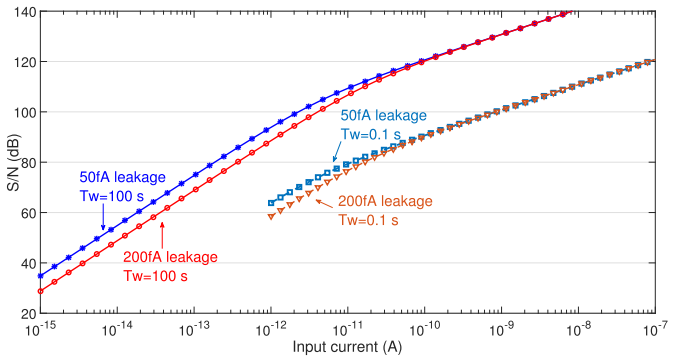

Fig. 7. Utopia S/N as a function of input current at 20 °C and at 40 °C for two different time windows, $T_{w1} = 100$ s and $T_{w2} = 0.1$ s.

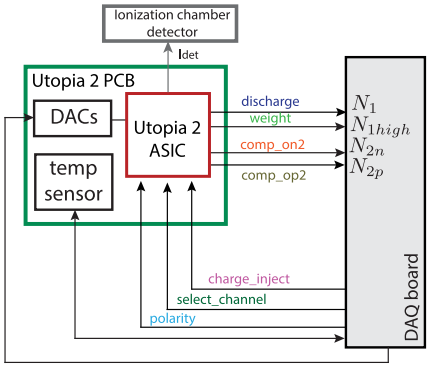

Fig. 8. Block diagram of Utopia 2 measuring system.

The S/N is plotted in Fig. 7 versus the injected current for two different leakage current values that correspond to different temperatures when the T_w is equal to 100 s and when it is equal to 100 ms. The effect of the leakage current that degrades the S/N can be observed. Additionally, the longer time window that corresponds to averaging shows that the S/N profile improves.

The low-frequency $1/f$ noise of the OTA and equally the noise of the external voltage reference V_{ref} are not included in this analysis but they will ultimately limit the S/N at high count rates.

V. Data Acquisition System and Active Leakage Current Compensation

The block diagram of the measuring system is depicted in Fig. 8. It includes the PCB that is hosting the ASIC with a humidity and temperature sensor that is used during the ratio ρ calibration and the DACs that set the switched capacitor voltage references $V_{\text{charge}+}$, $V_{\text{charge}-}$, and V_{cm}. The data acquisition board that was used is the ARTY Evaluation board that includes an Artix-7 field programmable gate array (FPGA) from Xilinx [37]. The DAQ system provides the counters that count the number of charge injections in a measuring time window T_w. The *"discharge"* signal is used to count the number of charge injections N_1 of the low range Q_{ref1} and the *"weight"* signal is used to count the number of times $N_{1\text{high}}$ that both the discharging circuits are activated. For channel 2, by monitoring the *"comp_op2"* and the *"comp_on2"* signals, the number of times N_{2p} or N_{2n} that the output of the second channel's integrator crosses the discriminators' thresholds is estimated. For the active leakage current compensation operation, according to the comparators of the second channel status, the FPGA generates the *"polarity,"* the *"select_channel,"* and the *"charge_inject"* signals. The *"polarity"* signal depends on the comparator that is triggered according to the leakage current polarity. The reference charge Q_{ref2}, controlled by the *"charge_inject"* signal, can be injected either to channel 2 or to channel 1 according to the value of the *"select_channel"* signal.

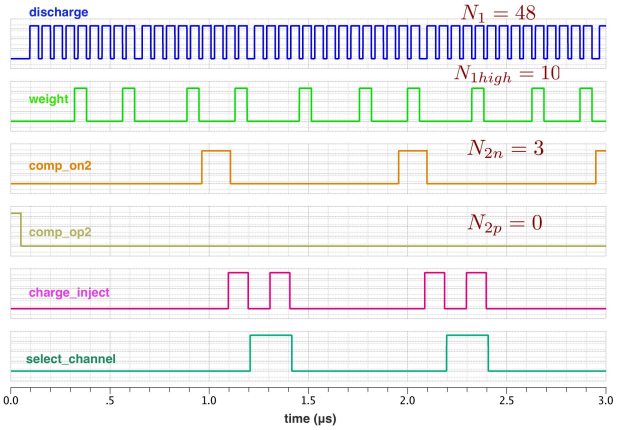

Fig. 9. Digital signals of Utopia 2 ASIC.

For the sake of clarity, the digital signals in a $T_w = 3$ μs and the respective counts are simulated as shown in Fig. 9.

VI. Measurement Results

A. Calibration

Before performing any measurement, the chips have to be calibrated. The flowchart in Fig. 10 shows the procedure that has to be followed for the calibration of the reference charges. Channel 2 is used as a reference charge source and a known current is injected by controlling the *"charge_inject"* signal from the FPGA. In calibration mode, the low-range switched capacitor circuit can be disabled using the signal *"enable low controls"*. This is how the Q_{ref1high} charge can be calibrated separately. Finally, after the injection of a well-known current into channel 1, the values of all the references charges Q_{ref1}, Q_{ref1high}, and Q_{ref2} are calculated and stored for each chip.

The ratio ρ between the leakage currents of channel 1 and channel 2 has to be estimated at nominal temperature or in the highest operating temperature of 55 °C. These measurements can be performed inside a climatic chamber where the temperature and humidity can be controlled. The two channels operate and integrate their own leakage. The ρ is stored for each chip in the FPGA that is responsible for the active leakage current compensation.

B. Measurements With Current Sources

Laboratory current sources were connected to the measuring system to characterize its dynamic range performance. Fig. 11 shows in logarithmic scale the measured current versus

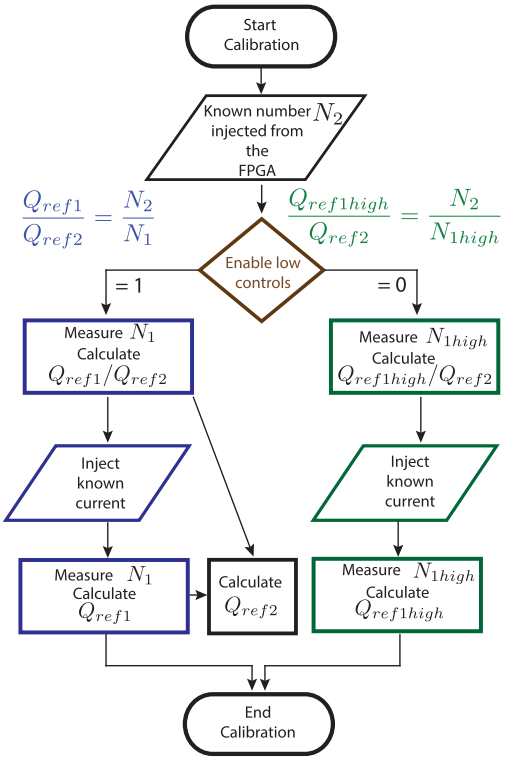

Fig. 10. Flowchart of the reference charges calibration.

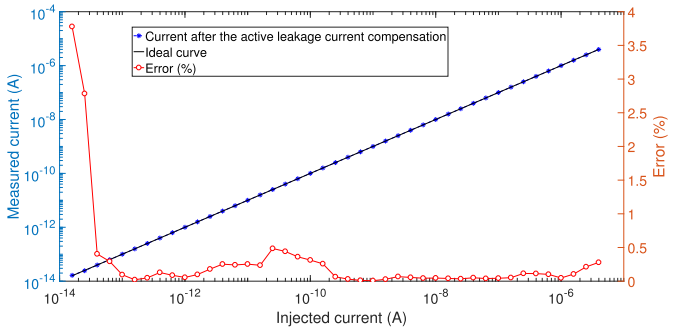

Fig. 11. Dynamic range measurement from 20 fA to 5 μA at 25 °C using a laboratory current source.

the injected current from a Keithley 6430 current source. It also presents the percentage error in the right linear axis for each injected current.

Precise femtoampere measurements down to 1 fA are very challenging. The Swiss Federal Institute of Metrology (METAS) has a certified system that is able to generate current as low as 1 fA. The current source that is available in METAS is based on the differentiation of a linear voltage into a dc current using calibrated reference capacitors [38]. The Utopia 2 ASIC was characterized at METAS, where current in the femtoampere range was injected. The results of the measurements down to 1 fA are presented in Fig. 12. To perform these ultra-low current measurements, the measurement time window was increased to $T_w = 100$ s.

C. Measurements With the Detector

The functionality of the front-end was verified qualitatively by performing radiation measurements with one of the

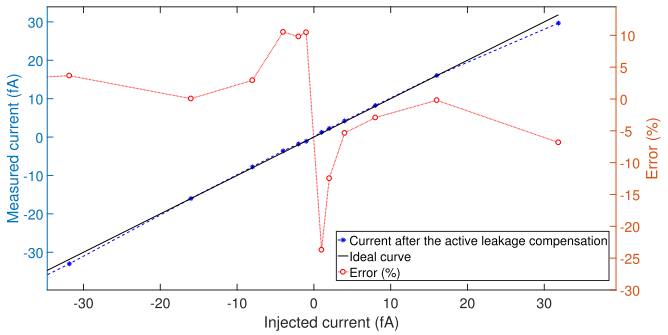

Fig. 12. Femtoampere current measurement at METAS.

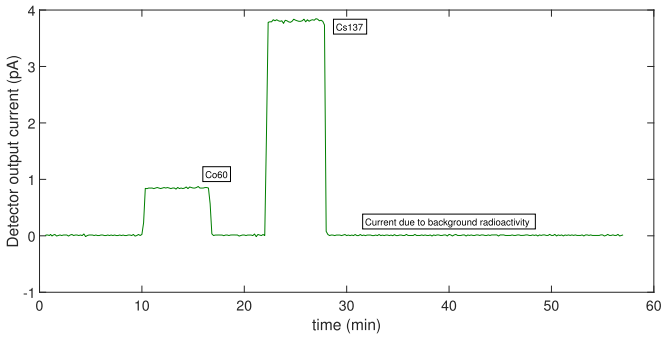

Fig. 13. Output current I_{det} when ^{60}Co and ^{137}Cs sources were placed close to the detector.

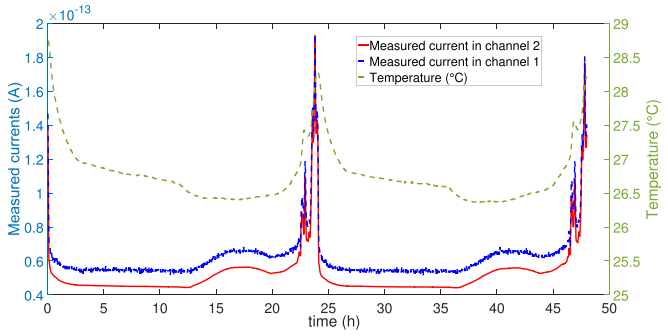

Fig. 14. Measured current due to the background radioactivity and temperature when the front-end was connected to the detector.

commercial radiation detectors used at CERN [7] and ^{60}Co and ^{137}Cs radiation sources. The sources were placed close to the detector for some minutes, and the measured current was equal to $I_{\text{det}} = 850$ fA and $I_{\text{det}} = 3.8$ pA, as shown in Fig. 13.

The importance of the active leakage current compensation can be demonstrated when measuring the current due to the background radiation. In that case, the detector's output current can be as low as tenths of femtoamperes. However, due to the possible temperature variations, the leakage current can be as high as hundreds of femtoamperes. Fig. 14 presents the measured current of channel 1 that includes the detector current and the net leakage current and the leakage current measured at channel 2. During this experiment that was performed for 48 h, the temperature was monitored. The measured currents

TABLE IV
COMPARISON AMONG ASICS USED FOR RADIATION MONITORING [33]

Characteristics	TERA06 [10]	TERA09 [14], [15]	QFW I ASIC [12]	BLM ASIC [13]	UTOPIA 1 [24]	UTOPIA 2 (This work)
Year	2004	2016	2004	2012	2015	2016
Technology	AMS 0.8 μm	AMS 0.35 μm	AMS 0.35 μm	IBM 0.25 μm	AMS 0.35 μm	AMS 0.35 μm
Die Size	6mm x 7mm	4.68mm x 5.8mm	3.28mm x 3.38mm	2.4mm x 3.775mm	2.6mm x 2.6mm	2.75mm x 2.75mm
Dynamic Range	5 decades	6 decades	1.60 pA to 180 μA	1 pA to 1.05 mA	-12 fA to -5 μA	-1 fA to -5 μA
Leakage Current	194 fA	2 pA	1.65 pA	-188 fA	-12 fA to -80 fA	<-1 fA
Linearity Error	$\pm$ 1%	$\pm$ 2%	$\pm$ 1.5%	$\pm$ 5%	$\pm$ 2.5%	$\pm$ 1% (100 fA to 5 μA)

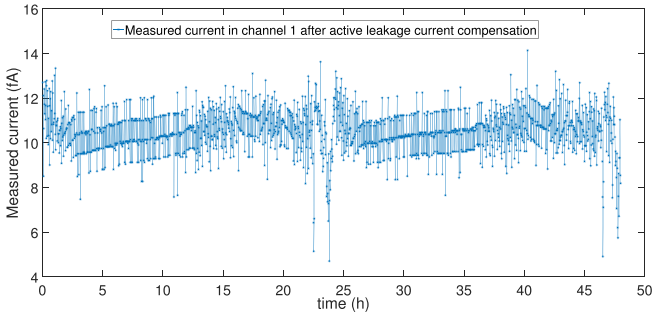

Fig. 15. Output current of the detector due to the background radioactivity after the active leakage current compensation.

increased when the temperature was increasing. Finally, Fig. 15 shows the measured detector current after the active leakage current compensation. This corresponds to 92 nSv/h that is compatible with the background radiation measured by a reference instrument at the time of the experiment.

VII. CONCLUSION

This paper presented the design procedure, the architecture, and the measurements of a novel ASIC named Utopia 2 that is used as the readout circuit and digitizer for ionization chambers for radiation monitoring. The Utopia 2 ASIC is based on current integration and charge balancing and demonstrates some key features like active leakage current compensation and automatic range changing. These functionalities allow the measurement of current over a wide dynamic range of nine decades. After integration over 100 s, the ASIC can digitize current as low as 1 fA. To achieve such performance, circuit techniques like source shifting were used during the microelectronic design and some guidelines were followed in system level design. Finally, the dominant source of leakage current that was related to the ESD protection diodes was eliminated using a two-channel compensating architecture. A comparison among other ASICs that are used for radiation monitoring is shown in Table IV. The Utopia 2 ASIC extends the current state of the art for sub-picoampere current measurements.

In a more advanced CMOS process, the leakage currents of a single device are expected to increase. Moreover, the scaling of the channel length leads to the increase of short channel effects. The subthreshold leakage current increases with technology scaling since the threshold voltage is reduced. The substrate leakage current that includes the p-n junction leakage and the GIDL also increases [19]. The downscaling of the oxide thickness leads to gate tunneling currents especially when $T_{ox} < 2$ nm [18], [39].

However, the guidelines that were set during this development and the active compensation can be used to mitigate the net leakage increase. The same operating principle, architecture, and guidelines can be also used in other applications when femtoampere measuring performance is required. Such applications include the digitization of biosensor signals, device characterization, and leakage current measurements.

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