

# FATALIC: A novel CMOS front-end readout ASIC for the ATLAS Tile Calorimeter

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**ABSTRACT:** The present article introduces a novel ASIC architecture, designed in the context of the ATLAS Tile Calorimeter upgrade program for the High-Luminosity phase of the Large Hadron Collider at CERN. The architecture is based on radiation-tolerant 130 nm Complementary Metal-Oxide-Semiconductor technology, embedding both analog and digital processing of detector signals. A detailed description of the ASIC is given in terms of motivation, design characteristics, simulated and measured performance. Experimental studies, based on 24 prototype chips under real particle beam conditions are also presented in order to demonstrate the potential of the architecture as a reliable front-end readout electronic solution.

**KEYWORDS:** Front-end electronics for detector readout, Calorimeter methods

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## 1 Introduction

The Large Hadron Collider (LHC) [1] at CERN is scheduled to undergo a decisive upgrade [2], which will extend its physics potential well beyond the initial design goal [3, 4]. The first phase (Phase-I) of the upgrade will take place during the long technical shutdown of the LHC, in 2019-2020, to improve the injector and the collider collimation system. In the second phase (Phase-II), scheduled for 2024-2026, the LHC will be further enhanced with new technologies, including 11-12 T triplet magnets and compact crab cavities with ultra-precise phase control. The final High Luminosity LHC (HL-LHC) is expected to begin operation in 2026, delivering proton-proton ( $pp$ ) collisions with a maximum instantaneous luminosity of  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  (7.5 times higher than the initial design). In terms of total integrated luminosity, a goal of 3000-4000  $\text{fb}^{-1}$  is defined.

In order to perform in the high intensity radiation environment of the HL-LHC, where up to 200 inelastic  $pp$  collisions (pile-up events) per 25 ns bunch crossing are expected, the ATLAS detector [5] is scheduled for upgrade of its sub-detector systems as well as the Trigger and Data AcQuisition (TDAQ) strategies [6]. In this context, the Phase-II upgrade program foresees the replacement of the readout electronics of the Tile Calorimeter (TileCal) [7, 8], the central hadronic calorimeter of ATLAS, with new architectures that will be able to deliver reliable measurements during the HL-LHC operation. Among the different designs proposed and evaluated for the Front-End (FE) readout electronics, the Laboratoire de Physique de Clermont-Ferrand (LPC) presented the solution of an ASIC that embeds both the analog processing and digitisation of the detector signal, the Front-end ATLAS tile Integrated Circuit (FATALIC). The following sections intend to provide a detailed description of the FATALIC motivation and design, and present simulation and experimental measurements to demonstrate its potential as a FE readout system.

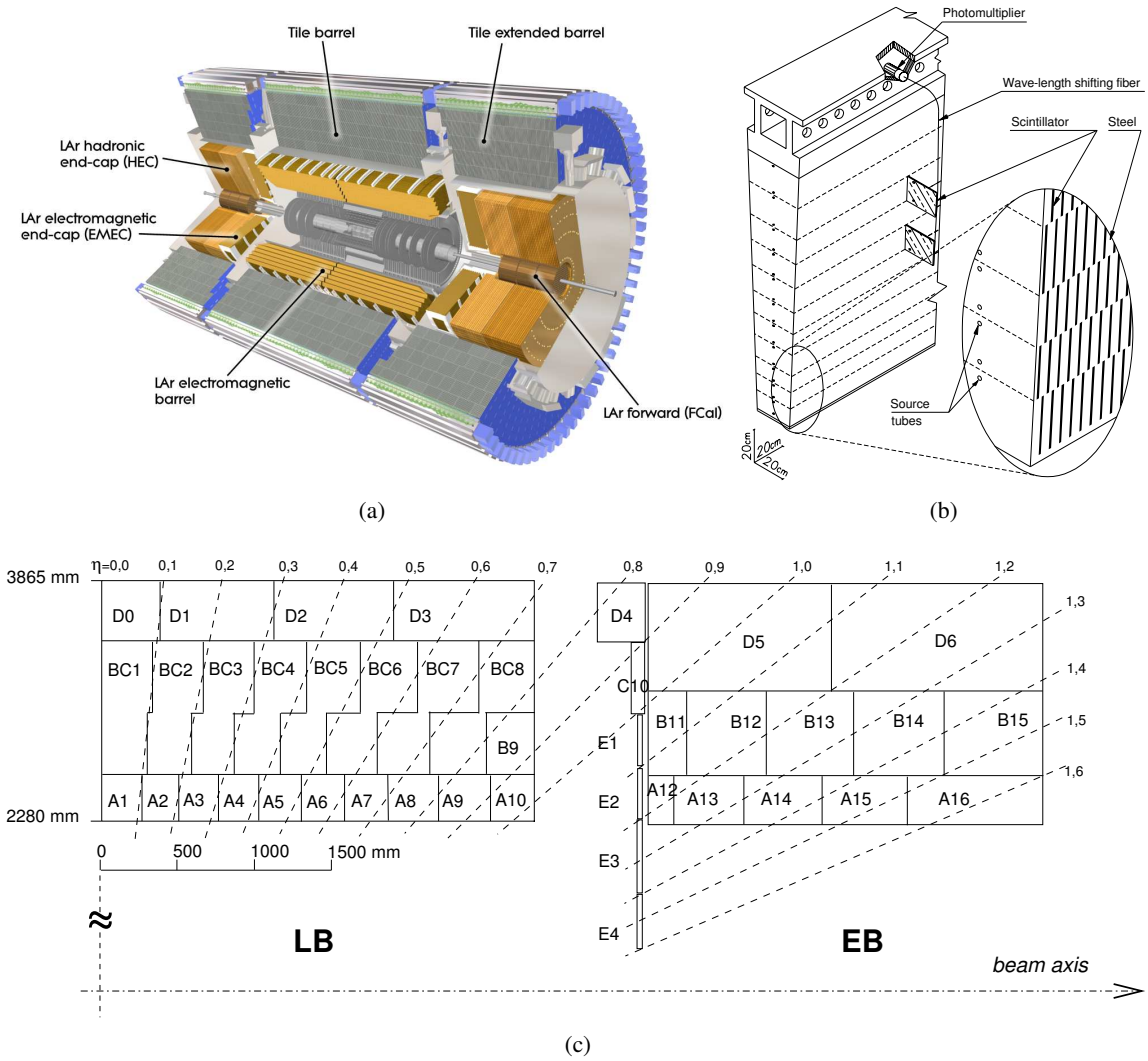
## 2 The ATLAS Tile Calorimeter

TileCal is a sampling calorimeter, constructed of steel plates as absorber and scintillating tiles as active medium, and it is important for the measurement of jet- and missing-energy, jet substructure, electron isolation and triggering (including muon information). The position of TileCal in the ATLAS calorimeter complex can be seen in figure 1a. It is divided into four cylinders, two of which form the central Long-Barrel (LB) while the other two constitute Extended-Barrel (EB) partitions, covering the pseudorapidity<sup>1</sup> range  $|\eta| < 1.7$ . Each Tile cylinder is made of 64 wedge modules (figure 1b) in the azimuthal coordinate. The Photo-Multiplier Tubes (PMTs) with the associated FE readout electronics and high voltage distribution cards are inserted at the outer radius of each module, hosted by a train of two 1.4 m long “drawers” which form a “super-drawer” (one super-drawer can host up to 48 PMTs).

The scintillation light is collected from the two opposite sides of the tiles by wavelength-shifting (WLS) fibres, which are bundled, to define readout cells, and coupled to a pair of PMTs. The current pulse induced at the PMT anodes, with a typical width of 10 ns, is therefore proportional to the

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<sup>1</sup>ATLAS uses a right-handed coordinate system, centered at the nominal interaction point. The  $x$ -axis points towards the center of the LHC ring, the  $y$ -axis points upwards and the  $z$ -axis points along the beampipe. Cylindrical coordinates  $(r, \phi)$  are used in the transverse plane,  $\phi$  being the azimuthal angle around the  $z$ -axis. The pseudorapidity is defined in terms of the polar angle  $\theta$  as  $\eta = -\ln(\tan \frac{\theta}{2})$ .



**Figure 1:** (a) The calorimeter system of ATLAS. (b) Schematic of a wedge module. (c) Tile cell mapping.

energy deposited in the respective cell and is fed to the FE electronics to be amplified, shaped and digitised at the 40 MHz LHC clock rate. This arrangement of the readout employs a total of 9852 PMTs and segments TileCal into three radial layers (figure 1c), classified as "A", "BC" and "D", with depth 1.5, 4.1, and 1.8 interaction lengths, respectively, at  $\eta = 0$ . Each A-BC-D cell grouping in the same  $\eta$ -direction forms a projective tower currently used for the fast trigger. Additional scintillators (E cells) are installed in the region between the LB and the EB, mainly to measure energy escaping the electromagnetic calorimeter, while at higher  $|\eta|$ , Minimum Bias Trigger Scintillators (MBTS) are used to monitor minimum-bias event rates. The E and MBTS scintillators have been used to monitor the luminosity during van der Meer scans<sup>2</sup> [9] and are also useful in electron identification.

<sup>2</sup>Van der Meer scans enable the measurement of the absolute luminosity of a particle collider by sweeping the

To ensure stable measurements, TileCal incorporates three calibration systems. A Charge Injection System (CIS) [10] is used to monitor the response of the FE electronics to known injected charge, but also to derive the conversion factors between the electronic responses and the input charge. Next, the Cesium (Cs) system [11, 12] uses a radioactive  $^{137}\text{Cs}$   $\gamma$ -source, hydraulically circulated through a system of tubes that traverses every row of scintillating tiles. The illumination of the tiles with 0.662 MeV  $\gamma$  produces a uniform, low current signal at the PMT anodes that allows inter-calibration of the detection chains (scintillators, WLS fibres, PMTs, FE electronics). After initial adjustment of the PMT gains, the Cs system is used to measure the small variations among the read-out responses, which are used to derive the necessary calibration coefficients with respect to a unique reference value. Lastly, the laser system [13] injects light pulses to the PMTs for frequent monitoring of the gains between Cs scans.

### 3 Upgrade of the Tile readout

In the current Tile readout scheme, the 256 super-drawers are interfaced to back-end Read-Out Drivers (RODs) through 256 optical links (plus another 256 links for redundancy) with a bandwidth of 800 Mbps per link. Each super-drawer stores the digitised samples from the read-out Tile cells in pipeline memories, while analog trigger signals, corresponding to each Tile tower, are transmitted to the off-detector trigger pre-processor. These trigger signals are formed by summation of the PMT outputs, in dedicated analog boards, with rough adjustment in time but without calibration to account for gain variations. Upon trigger acceptance, the data of each super-drawer are forwarded to the RODs.

For the HL-LHC, the TDAQ strategy [8] foresees a fully digital calorimeter trigger with higher granularity and precision. Each super-drawer is replaced by four independent mini-drawers, with half the length of the current drawers to allow easier access to the electronics and improve the reliability of the cooling circuits. At the 40 MHz rate, each mini-drawer transmits the entire set of digitised data to an off-detector PreProcessor (PPr) [14] over two 9.6 Gbps optical links (the full readout scheme employs 2048 optical links plus another 2048 links for redundancy). The PPr stores the data in pipeline memories and, in parallel, transmits calibrated trigger primitives (energy measured in grouped or individual Tile cells) to the trigger system. Upon receipt of a trigger acceptance signal, the reconstructed energy, the time and a quality factor for each Tile cell are forwarded to the data network for event aggregation and storage.

In the new Tile readout system, the present reliable but outdated Tile FE electronics will be replaced by a new architecture that will be able to endure the harsh radiation conditions anticipated at the HL-LHC (up to 50 krad Total Ionising Dose, as presented in Section 7.4) and handle the expected dynamic range of the input signal. The lowest expected signal from physics events is defined by the minimum ionisation Landau peak of muons traversing an A cell (smallest Tile cell) at normal incidence, with a most probable value of 350 MeV [15]. Considering the typical electromagnetic (EM) scale constant of 1.05 pC/GeV and the  $e/\mu$  response ratio of 0.91, the respective charge delivered by a single PMT is approximately 200 fC. On the other hand, the largest expected signal is that of energetic jets, depositing up to 1.3 TeV in EM scale (1.5 TeV in hadronic

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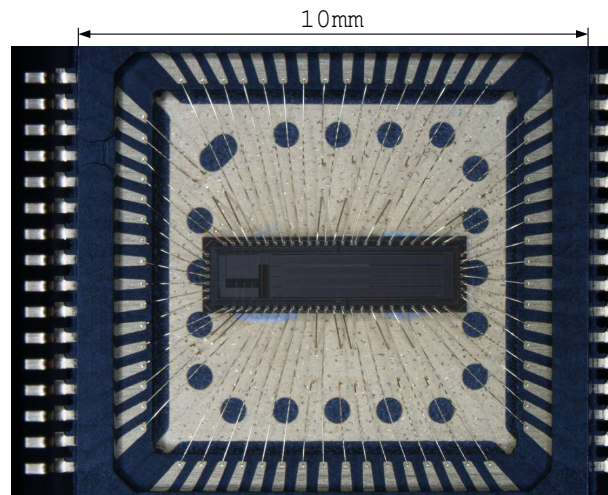
beams transversely across each other. Being responsible for luminosity measurements in ATLAS, TileCal must be able to measure very low Minimum Bias event rates.

scale) in a single Tile cell. To cover this range, the maximum charge requirement for one readout channel is set to 800 pC. There is however interest in extending the range up to 1.2 nC to be able to measure higher energy jets, expected in rare and possibly new physics events. In addition to the processing of physics signals, each FE electronic card must include a separate channel for large time-constant integration of low amplitude currents. This channel is needed for calibration scans using the Cs system (50 nA – 100 nA) but also for the monitoring of minimum-bias event rates and the instantaneous luminosity (20 pA – 10  $\mu$ A).

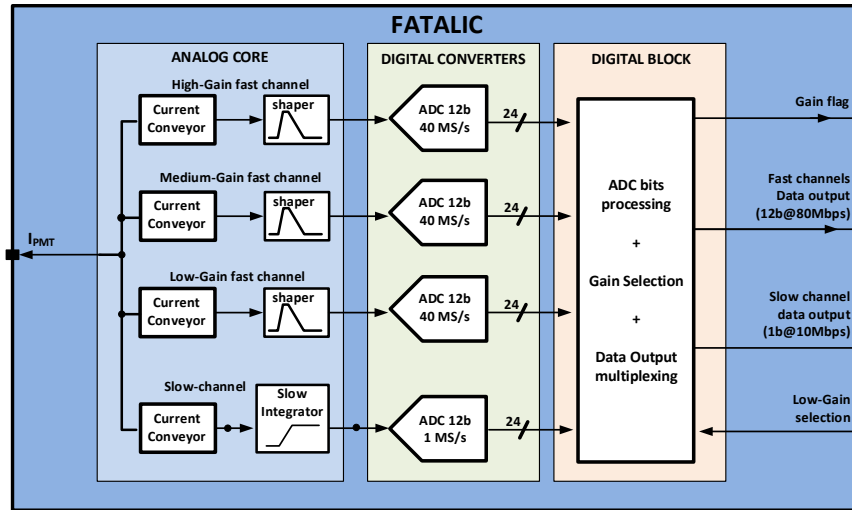
#### 4 The FATALIC Architecture

FATALIC is an ASIC, based on 130 nm GlobalFoundries (GF) Complementary Metal-Oxide-Semiconductor (CMOS) technology, designed to replace the current, discrete FE readout electronics of the TileCal. The proposal of an ASIC, embedding both analog signal processing and digitisation, is motivated by its significant advantages in terms of simplicity, radiation tolerance, power consumption and production cost for a large number of chips. On the other hand, since the operating low voltage (1.6 V) is dictated by the technology, FATALIC must rely on a current-driven, rather than a voltage-driven architecture to handle the large input dynamic range. Hence, an input stage employing current conveyors is implemented to adjust the impedance and distribute the signal to the different channels. Figure 2 shows a FATALIC chip, wire-bonded inside a 64-pin LQFP package.

The specifications of FATALIC are listed in table 1, while a block diagram summarising the architecture is given in figure 3. In order to handle the large input range (up to 1.2 nC), FATALIC provides three fast channels to process the PMT signal at the 40 MHz LHC clock rate, with relative amplification  $\times 1$  (low gain),  $\times 8$  (medium gain) and  $\times 64$  (high gain). This three-gain scheme is chosen, instead of using two gains, in order to improve the energy resolution (at the Tile cell level) across the input range, as shown by the related study in Section 8.3. In parallel, the signal is routed to an additional, slow channel for integration over a large (100  $\mu$ s) time constant.



**Figure 2:** FATALIC chip, wire-bonded inside an LQFP 64-pin package.



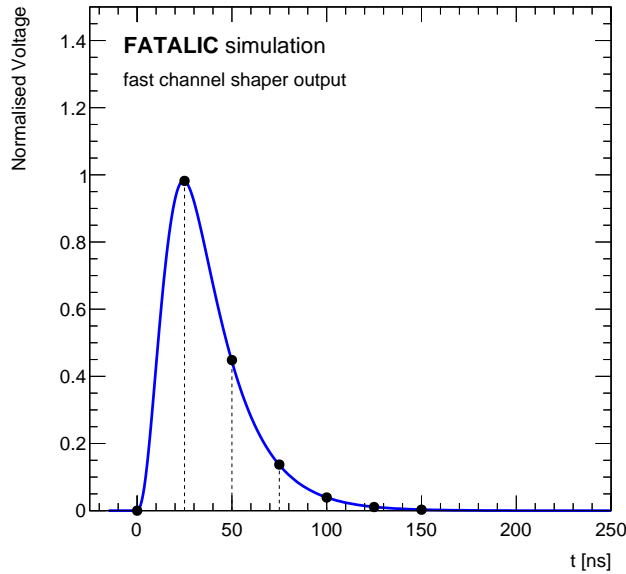
**Figure 3:** Block diagram of FATALIC.

Technology	130 nm CMOS GF
Number of channels per ASIC	1
Polarity	negative
Fast channel dynamic range in charge	25 fC - 1.2 nC
Fast channel dynamic range in current peak	1.25 $\mu$ A - 60 mA
Rise time of the current peak	4 ns
Fall time of the current peak	36 ns
Fast channel noise (rms)	<12.5 fC
Slow channel dynamic range in average current	0.5 nA - 1 $\mu$ A
Slow channel Noise (rms)	0.25 nA
Power consumption	~200 mW
Power supply	1.6 V
Output	12-bit words

**Table 1:** Specifications of FATALIC.

#### 4.1 Fast channels

In the fast channels the signal is read by three current conveyors with different input impedances, which define the respective gain ratios. Current integration and current-to-voltage conversion follow at the transimpedance-shaping stage by three identical shapers, composed by a differential amplifier with RC feedback loop. A 25 ns time constant is used to produce an asymmetric output pulse with 25 ns peaking time, as shown in figure 4. The digitisation is carried out in the ASIC, by 12-bit 40 MS/s Analog-to-Digital Converters (ADCs), to avoid degradation of the signal during transmission to an external converter. This establishes an effective 18-bit dynamic range and defines the range of each channel: 25 fC-20 pC (high gain), 200 fC-164 pC (medium gain) and 1.6 pC-1.3 nC (low gain).



**Figure 4:** Typical analog output pulse (simulation) from the fast channel shapers. At the 40 MHz clock rate, the 2<sup>nd</sup> sample coincides with the pulse peak.

## 4.2 Slow channel

The slow channel is designed to integrate low amplitude currents in the range from 0.5 nA to 1  $\mu$ A with minimum contamination from  $1/f$  noise, induced by the input stage. A current conveyor with low input impedance is therefore used to drive approximately 87% of the PMT signal to the slow channel, while current integration and current-to-voltage conversion are carried out by a differential amplifier with large time-constant (100  $\mu$ s) RC feedback. The integrated signal is then sampled by a 12-bit 833 kS/s ADC. Finally, to minimise the contamination from white noise in the measurement of such low amplitude currents, the data are obtained after averaging over a time interval of 10 ms, as described in Section 6.

## 4.3 Outputs

The 12-bit fast channel samples are read-out from 12 respective output pins. In order to comply with the bandwidth of the uplink to the back-end electronics (see Section 6), FATALIC is restricted to provide the data of only two of the three channels; the 12-bit data of the medium-gain channel are always delivered upon the rising edge of the 40 MHz clock, while the data of either the low- or the high-gain channel (alternative gain) are delivered upon the falling edge. The selection of the alternative gain is made by the embedded digital block, depending on the saturation of the most sensitive channel (dynamic gain switch), and is declared by an output flag. The dynamic gain switch can however be forced to provide only low gain readout by a dedicated input bit. On the other hand, slow channel data are delivered serially, at 10 Mbps (833 kHz for the 12 bits), through a single readout pin.

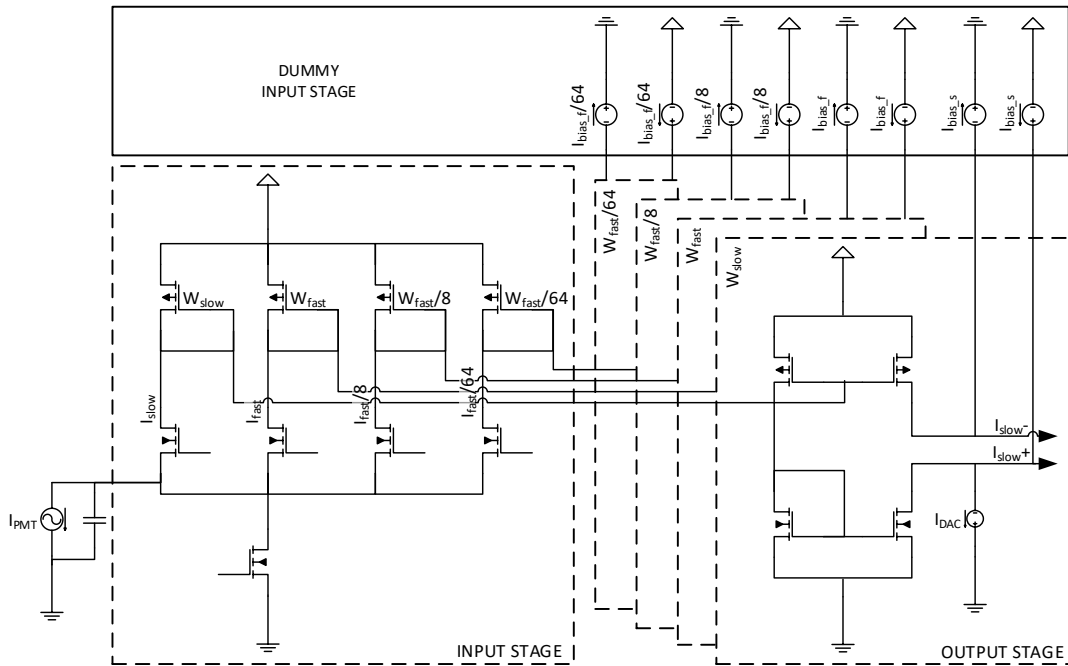


## 5 Development of the integrated circuit

### 5.1 Current conveyor system

The current conveyor system, schematically depicted in figure 5, consists of one input stage and four output stages, which provide differential signal to each of the FATALIC channels. At the input stage, a current mirror sets the biasing current to the nominal value of 0.5 mA. The PMT signal is read at the source of four common-gate NMOS<sup>3</sup> with the same length (L) but with different widths:  $W_{fast}/1$  (high gain),  $W_{fast}/8$  (medium gain),  $W_{fast}/64$  (low gain) and  $W_{slow} = 8 W_{fast}$  (slow channel). A PMOS<sup>4</sup> current mirror is then used to replicate the current from the drain of each NMOS onto the respective output stage, while a replica of the input stage (dummy) is implemented to return just the biasing current to be subtracted from the final output.

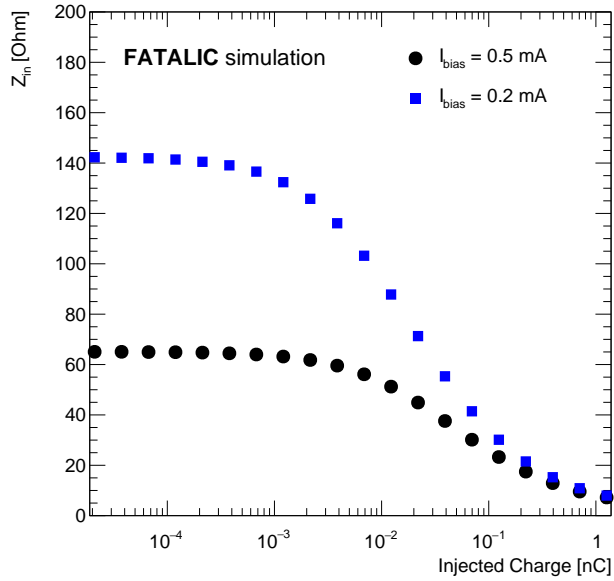
In terms of noise, the performance of such current-conveyor is modest compared to a charge preamplifier, but well adequate, given the large dynamic range of input stage. The input impedance is kept below  $70 \Omega$  for the entire input range, as presented in figure 6. Finally, to account for the open-loop configuration of the input stage, which induces large dispersion among the pedestal values, a tuning system with a Digital-to-Analog Converter (DAC) is also added to the above design.



**Figure 5:** The current conveyor system, consisting of the input stage, the four output stages and a replica (dummy) of the input stage in order to subtract the biasing current from the differential output.

<sup>3</sup>Negative channel Metal Oxide Semiconductor

<sup>4</sup>Positive channel Metal Oxide Semiconductor



**Figure 6:** Input impedance as a function of the input charge for the nominal biasing current,  $I_{bias} = 0.5$  mA, and for a test value of  $I_{bias} = 0.2$  mA.

## 5.2 Signal shaping

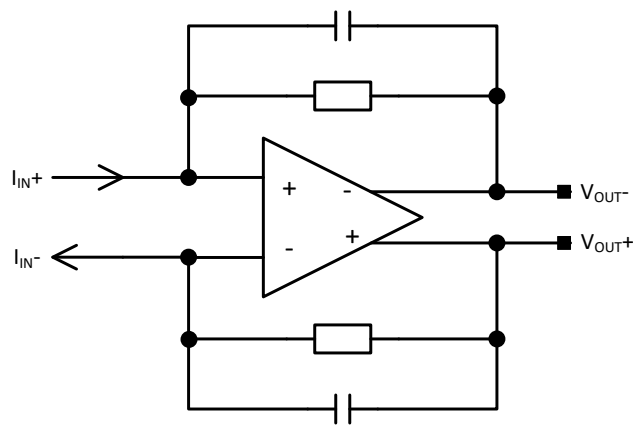
The shaper (figure 7a) is a differential amplifier with RC feedback loop, with a time constant of 25 ns ( $R = 5$  k $\Omega$ ,  $C = 5$  pF) in the fast channels and 100  $\mu$ s ( $R = 500$  k $\Omega$ ,  $C = 200$  pF) in the slow channel. The amplifier is based on a folded-cascode boosted architecture, depicted in figure 7b, with two differential input pairs, one NMOS and one PMOS, and Common Mode FeedBack (CMFB) to control the output common mode. Its open-loop characteristics are listed in table 2.

Open-loop gain	84 dB
-3db bandwidth	38 kHz
Unity-gain bandwidth	650 MHz
Slew rate	220 V/ $\mu$ s
Phase margin	85°
Supply voltage	1.6 V
Consumption	2.3 mA

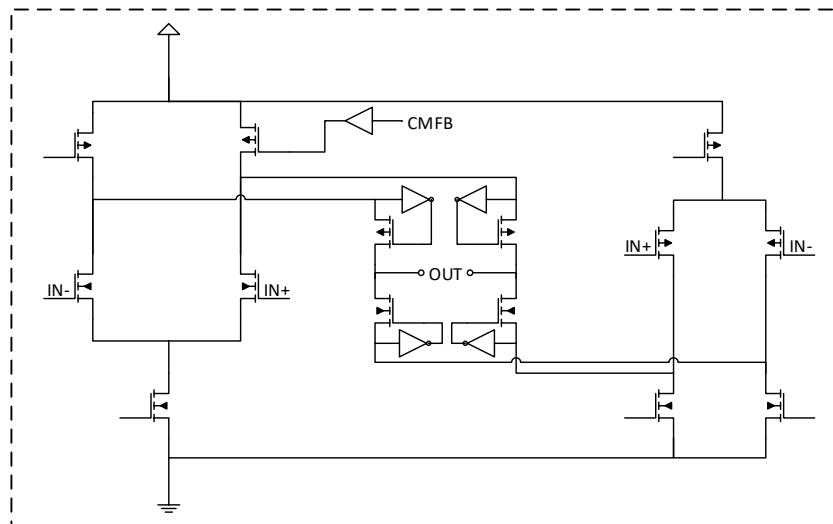
**Table 2:** Open-loop characteristics of the shaper with the ADC input capacitive load of 1.6 pF.

## 5.3 Signal digitisation

The shaper output is sampled by three 12-bit 40 MS/s ADCs in the fast channels and one 12-bit 833 kS/s ADC in the slow channel. The ADC design by LPC is based on the pipeline architecture



(a)



(b)

**Figure 7:** (a) Schematic of the shaper, consisting of a differential amplifier with RC feedback loop. (b) Architecture of the differential amplifier.

with 1.5-bit-per-stage resolution. Among the various efficient ADC architectures developed and improved over the last ten years, the pipelined ADC has been adapted for high resolution, speed and dynamic range with relatively low power consumption and low component count. In CMOS technologies, resolutions in the range of 10-14 bits with a sampling frequency up to 100 MS/s are typically achieved with power consumption lower than 100 mW.

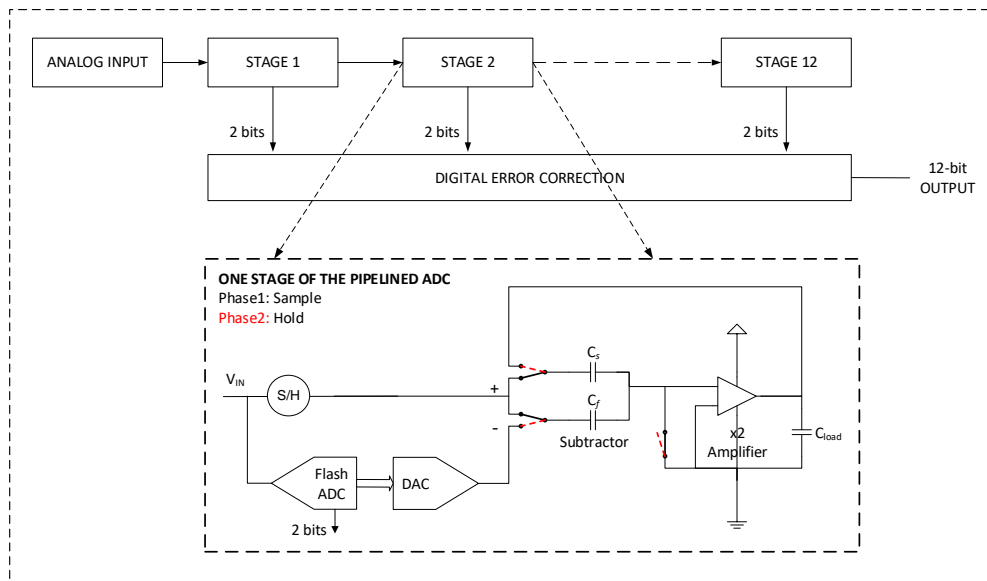
Figure 8 presents the block diagram of the pipelined ADC, with two output bits per stage, displaying the architecture of one of the stages. Each stage receives a differential input voltage, in the range  $\pm 500$  mV, which is read by a sample-and-hold (S/H) and a 2-bit flash ADC. The flash ADC compares the input to two threshold voltages ( $\pm 125$  mV) and outputs a 2-bit word, while a DAC and a residue amplifier provide the input to the next stage, as presented in table 3. Although a

2-bit word is delivered, the effective resolution is 1.5-bit since the combination 11 is avoided. This bit redundancy limits the degradation of the Integral Non-Linearity<sup>5</sup> (INL) due to variations of the residue amplifier gain or the comparator offsets (the INL is unaffected by variations of the offset voltage for up to  $\pm 12.5\%$  of the full-scale input voltage). The complete architecture includes 12 cascading stages and is followed by the digital correction block (see Section 5.4), which delivers the final digital code. The estimated power consumption of the ADC is 48 mW.

$V_{in}^i$	$[b_2 b_1]$	DAC	$V_{in}^{i+1}$		
$V_{ref}/4$	-	$V_{ref}$	[10]	$V_{ref}/2$	$2V_{in}^i - V_{ref}$
$-V_{ref}/4$	-	$V_{ref}/4$	[01]	0	$2V_{in}^i$
$-V_{ref}$	-	$-V_{ref}/4$	[00]	$-V_{ref}/2$	$2V_{in}^i + V_{ref}$

**Table 3:** Each stage  $i$  of the pipeline converts the input voltage  $V_{in}^i$ , in the dynamic range  $\pm V_{ref}$ , into a 2-bit word  $[b_2 b_1]$  and feeds the amplified residual  $V_{in}^{i+1} = 2(V_{in}^i - DAC)$  to the next stage.

**The comparator.** The architecture of the comparator is presented in figure 9. The transconductance input stage is fully differential, comparing the differential input signal to the differential threshold voltage, while isolating the input from kick-back noise, induced by the switching of the subsequent latched stage. The latched stage performs the comparison when the switch-transistors are OFF and a reset when they are ON. The state of the comparator, when it is latched, is memorised



**Figure 8:** Block diagram of the 12-bit pipelined ADC with two output bits per stage.

<sup>5</sup>The INL is defined as the deviation, in Least-Significant-Bits (LSBs), of the output code from the ideal transfer-function.

thanks to the bistable third stage. Lastly, two NOT gates perform the final digital shaping of the output signal. The main characteristics of the comparator are given in table 4.

**The DAC.** The DAC employs a set of switches, controlled by the comparators, to select the differential reference voltage to be applied on the feedback capacitor of the residue amplifier. Given the  $\pm 500$  mV input dynamic range, the reference voltages are set to  $\pm 250$  mV.

Clocking frequency	40 MHz
Sensitivity	$50 \mu\text{V}$
Power supply	1.6 V
Power consumption	2.1 mW

**Table 4:** Characteristics of the comparator.

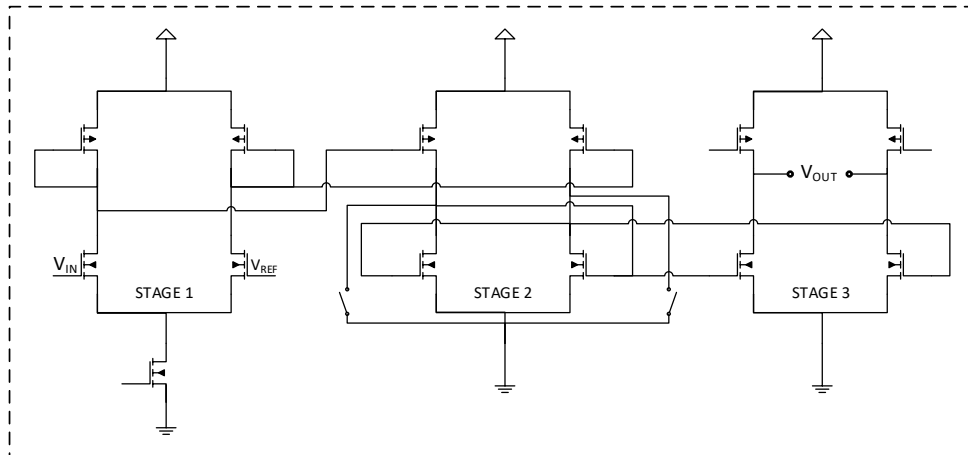
**The gain-2 residue amplifier.** The residue amplifier, displayed in figure 8, is a differential amplifier with capacitive feedback. Capacitive, rather than resistive feedback is used for better component matching, which is crucial for the accuracy of the amplification and, therefore, the linearity of the ADC. A capacitance of 800 fF is sufficient to minimise both the thermal noise ( $kT/C$ ) and the component mismatch ( $\sim 1/\sqrt{C}$ ). On the other hand, the design requires a small die surface and low supply current for dynamic performance. To match both the sampling ( $C_S$ ) and feedback ( $C_F$ ) capacitance to 800 fF, with an accuracy better than 0.1%, an array of four 1600 fF MIM capacitor unit cells is drawn in common-centroid layout, while dummy switches are added to counterbalance parasitic capacitors introduced by the reset switches. Lastly, the timing sequence, controlling the sample, hold/amplification and reset phases of each stage, has been carefully defined to prevent charge disruption.

#### 5.4 Digital block

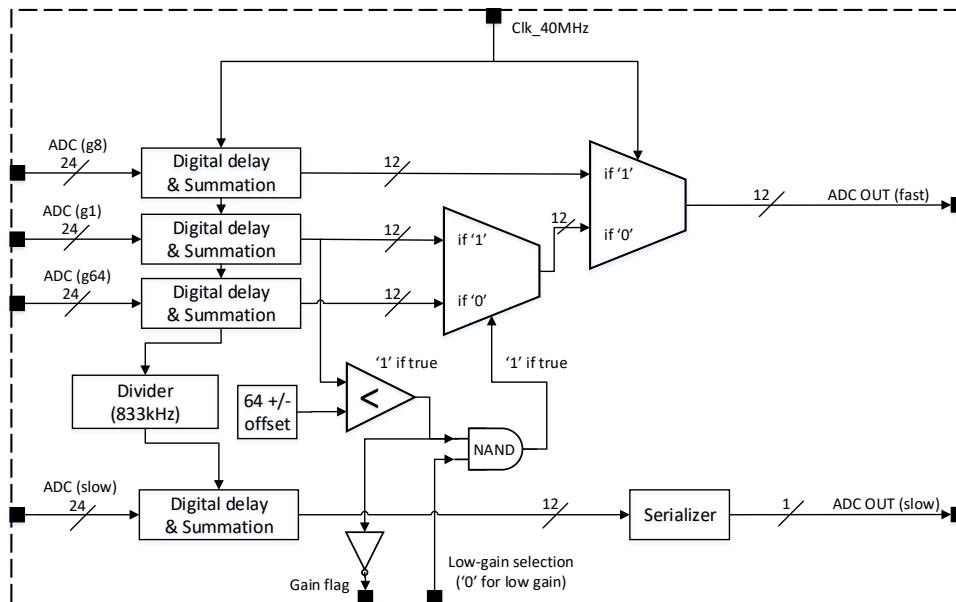
Each ADC delivers twelve 2-bit words at the 40 MHz clock rate. The result of the complete conversion is therefore a 24-bit word with 12 redundant bits. The digital block (figure 10) synchronises the outputs using shift registers to compensate for the delay due to the position of each stage in the pipeline. The total latency of this process is equal to eight clock cycles (200 ns) and it is fixed for every power cycle. Digital summation (with carry-save) of the most-significant bit of each stage with the least-significant bit of the previous stage is then performed to the final 12-bit code every 25 ns for the fast channels and 1.2  $\mu\text{s}$  for the slow channel. The second function of the digital block is to select the alternative gain output between the high-gain and the low-gain channel data (see Section 4.3). This selection is made according to the output of the low-gain channel; if it is equal or higher (lower) than 600 ADC counts, then the low-gain (high-gain) channel data are delivered.

#### 5.5 Floorplan

The floorplan of FATALIC (figure 11) is optimised for minimum surface, while preserving signal integrity. Two main regions are distinguished; the region hosting the input stage and the shapers (analog block), and the region hosting the ADCs and the digital block. The two regions are isolated



**Figure 9:** Architecture of the comparator (single-ended representation for simplicity).

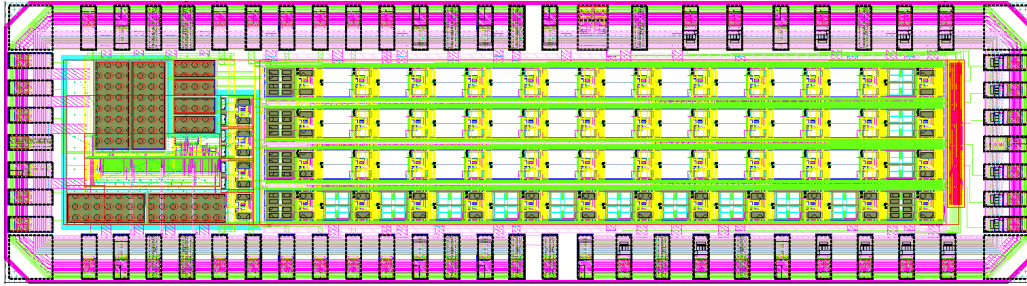


**Figure 10:** Architecture of the digital block.

by a high impedance (BFMOAT) layer to reduce the coupling. The analog power and reference voltage rails are also decoupled by embedded large capacitors. The total surface of the chip measures  $7.5 \text{ mm}^2$ , while the core area is limited to  $2.3 \text{ mm}^2$ .

## 5.6 Design verification

All standard verification checks have been performed for the design of FATALIC. The analog part was tested with Monte Carlo simulations, using the Virtuoso Analog Design Environment by



**Figure 11:** The floorplan of FATALIC. Two main regions are distinguished; the region hosting the analog blocks (left) and the region hosting the ADCs and the digital block.

Cadence. The yield with process and mismatch is evaluated to 90%, while the offset of the input stage, which is an open loop configuration, is tunable to maintain a high yield and was assessed with mismatch simulations. Corners simulations did not highlight sensitivity of the ASIC to the temperature or the power supply. For the digital part of the ASIC, simulations were performed with SOC Encounter, while for the full ASIC, mixed-mode simulations were performed with the Virtuoso Analog Mixed-Signal (AMS) Designer. Finally, the good performance of the ASIC is confirmed with all of the 24 prototype chips that were produced.

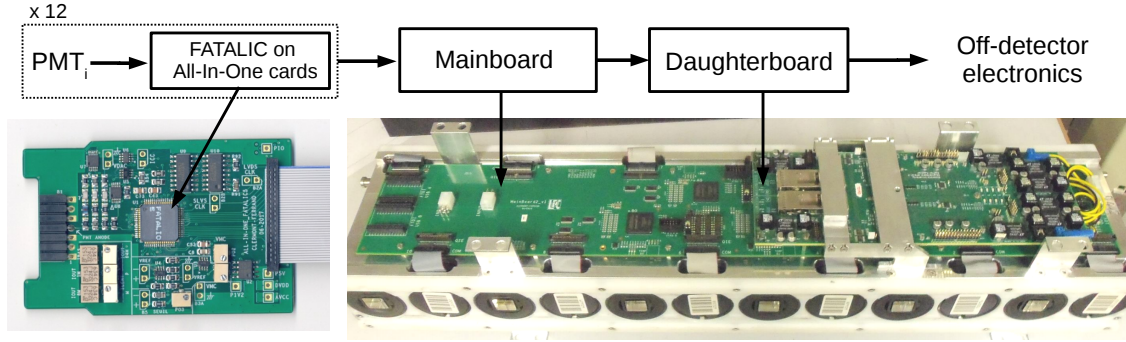
## 6 Associated cards

Figure 12 displays a fully equipped mini-drawer, hosting 12 PMTs, 12 “All-in-One” cards, each of which contains one FATALIC chip and the dedicated CIS, and the Mainboard, which controls the All-in-One cards and transmits the data to the Daughterboard. Both the All-in-One cards and the Mainboard have been designed by LPC for the purposes of FATALIC. The Daughterboard, also shown in figure 12, is the on-detector interface to the back-end electronics. It is divided into two independent sides, each of which establishes a 9.6 Gb/s uplink to deliver the data of six readout channels to the off-detector PPr, while a 4.8 Gb/s downlink is used to transmit the LHC clock as well as control and configuration commands.

### 6.1 All-in-one card

The All-in-One card contains FATALIC and the CIS. It is based on a 6-layer Printed Circuit Board (PCB) with dimensions 7.0 cm × 4.7 cm. On one side, a 7-pin connector attaches the card to the high-voltage divider, at the basis of the PMT, while on the opposite side a 40-conductor ribbon cable establishes communication with the Mainboard. Finally, nine on-board potentiometers adjust the low voltage supply and the pedestal for each channel.

A schematic diagram of the CIS is given in figure 13. The charge injection is driven by a 12-bit DAC with maximum output 4.095 Volts. The DAC charges one of the three available capacitors, 5.6 pF, 39 pF or 330 pF, for the scanning of the high-, medium- or low-gain dynamic range, respectively. The connected capacitance is defined through analog switches, controlled by two timing signals from the Mainboard. The same timing signals control the charge/discharge



**Figure 12:** Schematic view of the readout chain. Left: the All-In-One card supporting FATALIC. Right: a fully equipped mini-drawer housing 12 PMTs along with the associated readout electronic cards.

(through appropriately adjusted resistances) cycles reproducing the PMT pulse shape. Finally, the DAC is also connected to a Howland DC current source to allow calibration of the slow channel.

## 6.2 Mainboard

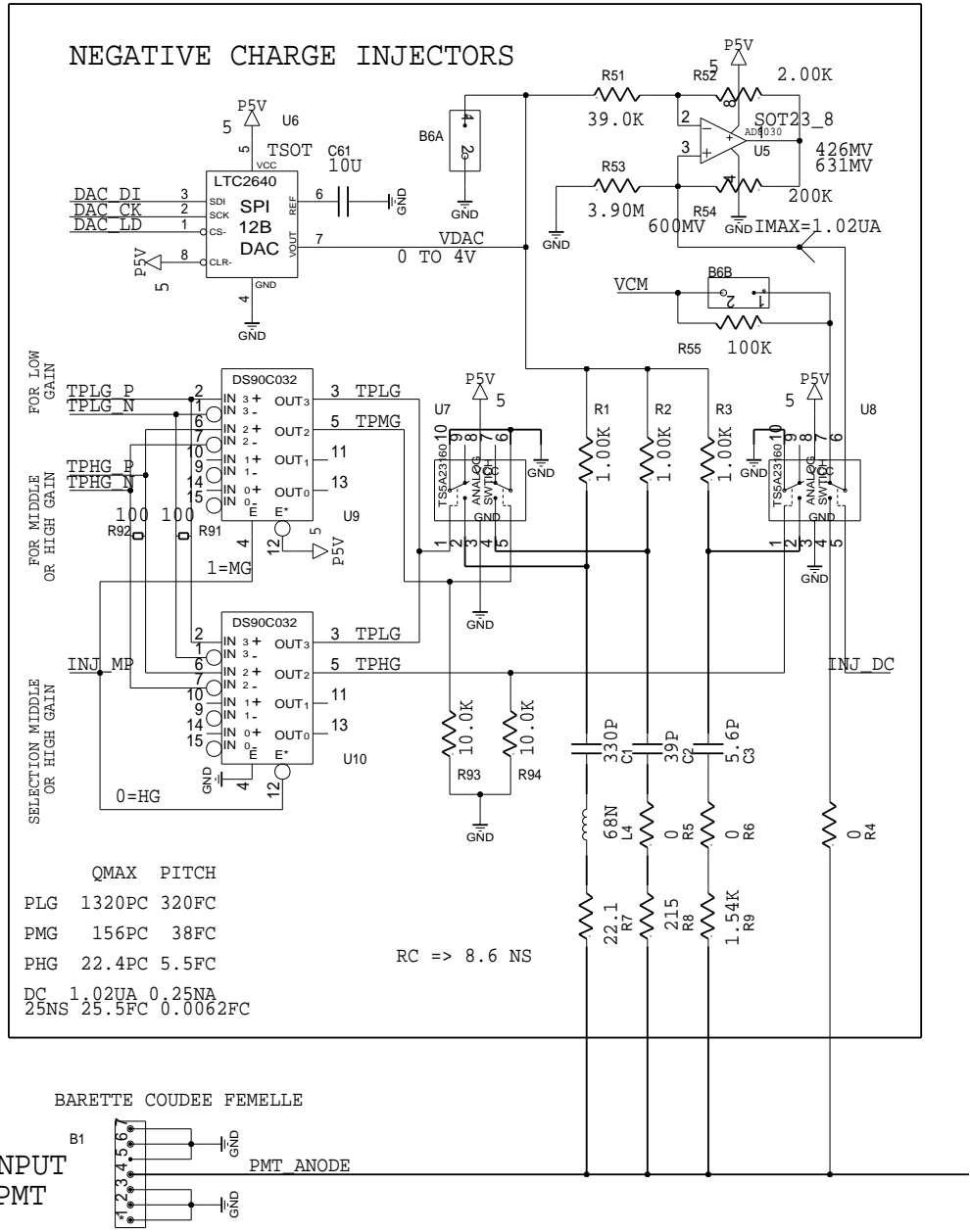
The twelve All-in-One cards of one mini-drawer are controlled by the 28 cm × 10 cm Mainboard, which serialises the data for transmission to the Daughterboard and distributes clocks and commands from the Daughterboard to the FE electronics. It also distributes the 10 V low-voltage supply, by means of point-of-load regulators, to power both the All-in-One cards and the Daughterboard. The connection to the Daughterboard is established with a 400-pin FPGA Mezzanine Connector (FMC).

The Mainboard is divided into two sections, each of which receives a separate 10 V supply and carries two Altera Cyclone4 FPGAs. Each FPGA controls three All-in-One cards and communicates with the Daughterboard through a Serial Peripheral Interface (SPI) port. The data of each of the two output fast channels are transmitted to the Daughterboard in Low-Voltage Differential Signaling (LVDS) with a “2-Lane Output, 16-bit Serialisation” at 320 Mbps. The necessary synchronisation clocks (160 MHz and 40 MHz) are also generated by the FPGA, in common for the three cards. On the other hand, slow channel data are digitally summed in the FPGA over a time interval of 10 ms and delivered to the Daughterboard through a standard Inter-Integrated Circuit (I<sup>2</sup>C) bus.

## 7 Simulation and performance

The following paragraphs describe the performance of FATALIC in terms of noise, linearity and radiation tolerance, based on simulation and experimental measurements with 24 prototype chips. For the simulation of the ASIC, the Cadence Virtuoso Analog Mixed-Signal Design Environment is used. Regarding the experimental measurements, it must be noted that the All-in-One cards, used to accommodate FATALIC for the purposes of these studies, are not adequate to support the slow channel of FATALIC. Specifically, due to the particularly large gain of the slow channel, the resistance range of the respective on-board potentiometer is not sufficient for the adjustment of the pedestal within the input dynamic range. As a workaround, it was decided to reduce the biasing





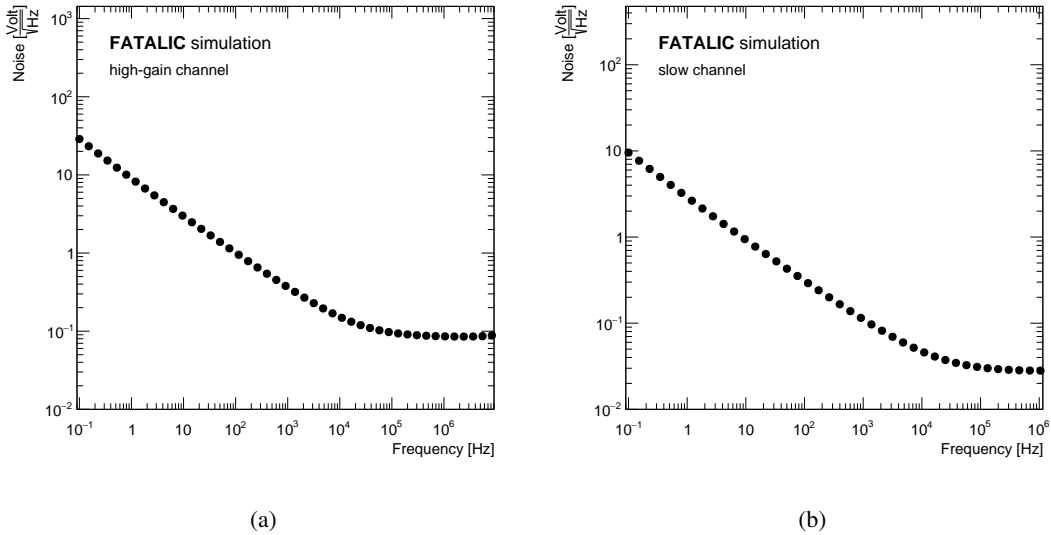
**Figure 13:** Schematic diagram of the CIS.

current in the input stage, from the nominal value of 0.5 mA to 0.2 mA. This however affected the performance of the fast channels, causing dynamic amplification of the signal depending on the amplitude, with significant impact on the linearity. This effect would normally be eliminated by equipping the All-in-One cards with potentiometers of larger resistance range or by implementing slow control functionalities in FATALIC.

### 7.1 Noise measurements

The dominant noise introduced in the fast channels is white noise from the input stage, expected from simulation to be approximately 8 fC in the high-gain channel. On the other hand, the dominant noise in the slow channel is  $1/f$  noise from the input stage, estimated at the level of 7 nA. This substantially exceeds the specification of 0.25 nA (see table 1) initially defined for FATALIC because the lowest region of the noise frequency spectrum was not properly included in the simulations used to define the design. The spectral density of the noise for the fast and slow channels is given in figure 14.

Experimental measurements of the noise were taken with the All-in-One cards connected to PMTs under high voltage, without signal. Figure 15a, 15b present the mean and standard deviation of the pedestal distribution in the fast channels, obtained by gaussian fit. The noise, estimated from the standard deviation, averages to  $(2.49 \pm 0.36)$  ADC counts in the high-gain (dominated by white noise from the input stage),  $(1.30 \pm 0.15)$  ADC counts in the medium-gain and  $(1.23 \pm 0.10)$  ADC counts in the low-gain channel (dominated by noise from the ADC). Using the fC/ADC conversion factors of Section 7.2, the above numbers can also be translated into units of input charge, namely  $(6.1 \pm 0.9)$  fC,  $(26.5 \pm 3.1)$  fC and  $(260.0 \pm 21.1)$  fC, respectively. The small difference between the measured noise in the high gain channel and the simulation could be explained by the reduction of the biasing current, described above. Finally, the results for the case of the slow channel are



**Figure 14:** Simulation of the noise spectral density in the (a) fast channels (high gain) and (b) slow channel.

presented in figure 15c, 15d. In this case the average noise is found  $(26.2 \pm 0.7)$  counts which, considering the design ratio of 0.25 nA/count, corresponds to  $(6.6 \pm 0.8)$  nA, in good agreement to the simulation.

## 7.2 Linearity measurements

Figure 16a, 16b and 16c present the linearity, obtained by simulation, of the analog pulse peak amplitude (in millivolt) with the input charge. The non-linearity, defined as the deviation from a linear fit over the maximum channel response (1 V), is estimated to be below 0.3% in the input range up to 850 pC, while at higher charge values it increases, reaching approximately 0.6% at 1.2 nC. In the case of the slow channel, the deviation from linearity is expected to be less than 0.2% over the entire input dynamic range, as shown in figure 16d.

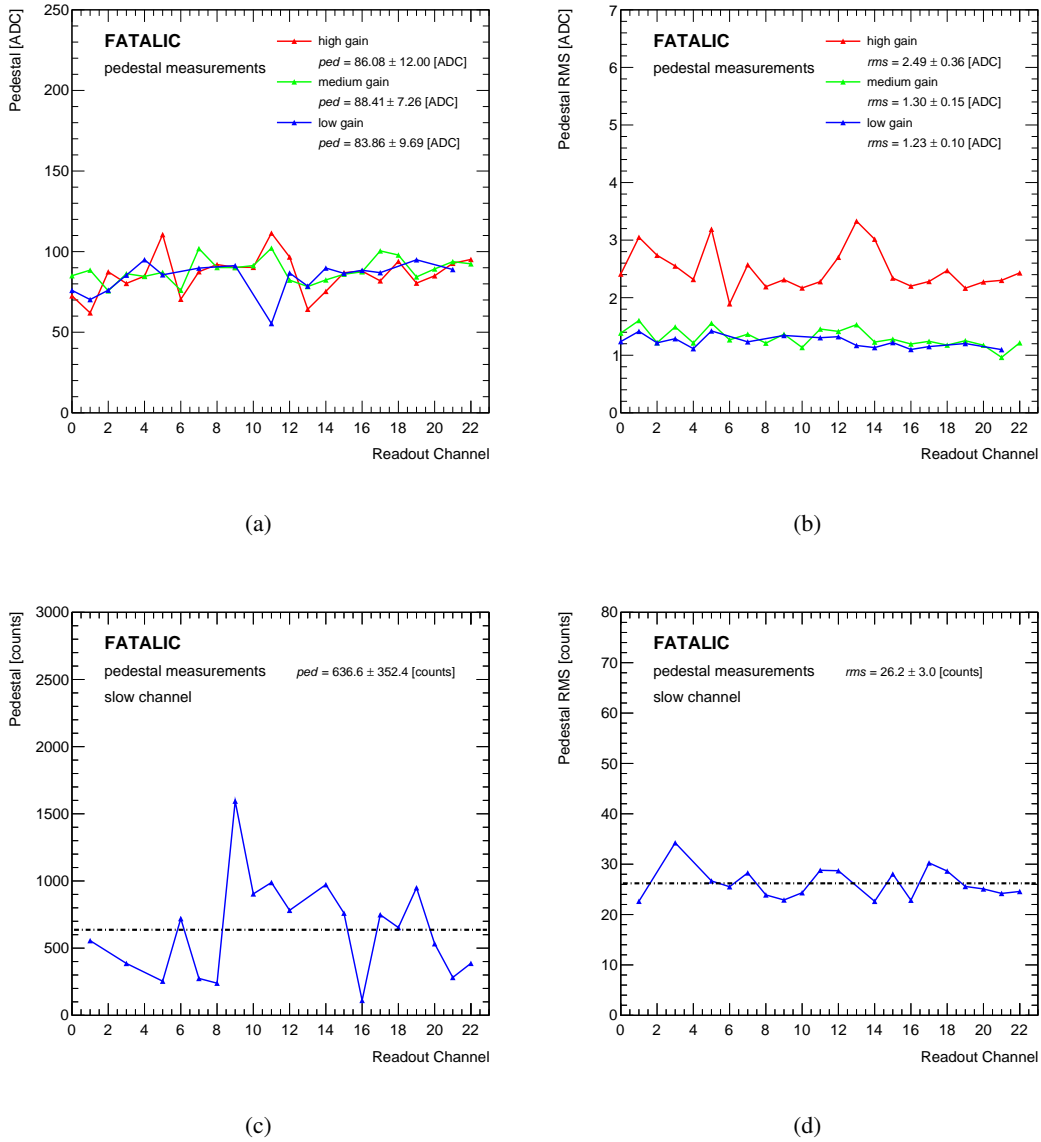
Experimental studies of the linearity are carried out using the on-board CIS. Since the linearity of the CIS has not been verified, the response in this case is obtained from the sum of the selected digitised samples, which is less sensitive to the shape of the injected pulse. Figure 17a, 17b and 17c present an example of the measured response as a function of the injected charge, for one chip. In the high-gain channel, the maximum deviation from linearity (average from all the tested prototype chips, relative to the maximum response) is measured to be  $(0.3 \pm 0.1)\%$  above 2 pC, increasing to  $(1.3 \pm 0.2)\%$  for lower charge values. In the medium-gain channel, the deviation is  $(1.4 \pm 0.6)\%$ , while in the low-gain channel it is  $(0.4 \pm 0.1)\%$  below 800 pC, reaching  $(3.5 \pm 0.7)\%$  at 1.2 nC. Finally, the fC/ADC conversion factors, summarised in figure 17d, are extracted from the slope of the linear interpolation and average to  $(2.46 \pm 0.03)$  fC/ADC for the high-gain,  $(20.4 \pm 0.7)$  fC/ADC for the medium-gain and  $(211.3 \pm 6.4)$  fC/ADC for the low-gain channel.

Two effects have been confirmed to contribute significantly to the observed difference between the measured linearity and the expectation, both regarding the present All-in-One card. The first one is the workaround, described above, of reducing the biasing current in the input stage from its nominal value in order to enable the operation of the slow channel. The second contribution comes from imperfections in the CIS, which have significant impact on the injected pulse shape (while in simulation FATALIC is always injected with the same PMT pulse shape). Both of these imperfections would be corrected in a subsequent version of the All-in-One card.

## 7.3 Performance of the analog and digital block

Dedicated studies have been carried out in order to assess the performance of the analog and digital block of FATALIC separately. For these studies, one chip of a previous version of FATALIC was used, which provided a dedicated output of the analog block and also contained an additional ADC, independent of the analog block. In order to measure the INL error, a differential slow ramping signal is delivered at the input of the ADC, which is clocked at the nominal frequency of 40 MHz, and the observed output is compared to the ideal transfer function across the entire dynamic range. Similarly, the Differential Non-Linearity (DNL) error is estimated from the difference between the actual step width and the ideal step of 1 LSB. The results are shown in figure 18. The INL error is found to be within  $\pm 3$  LSB, while the DNL error is less than  $\pm 1$  LSB.

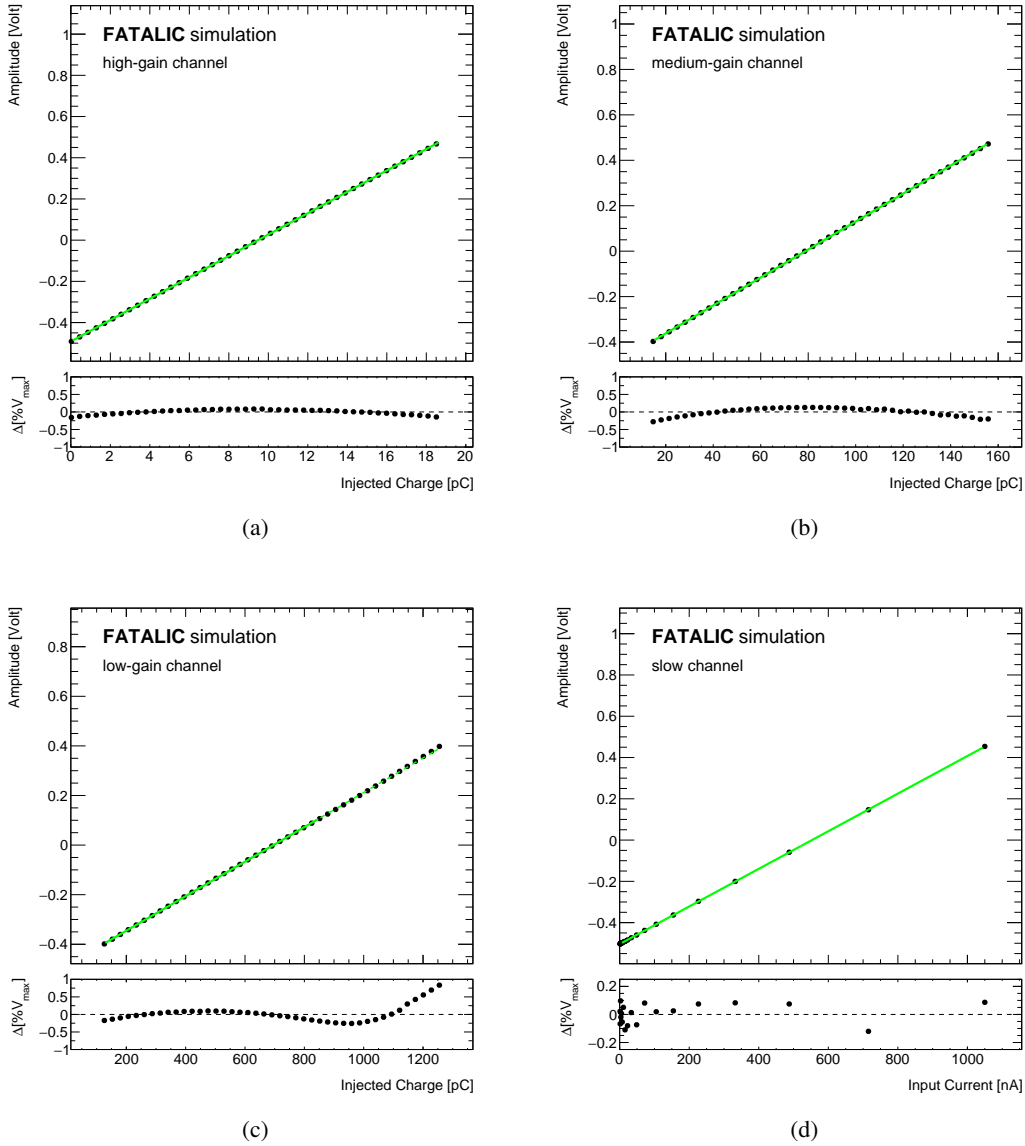
Furthermore, the intrinsic noise of the ADC was obtained from the standard deviation of the output, for an input signal corresponding to the middle of the dynamic range, i.e. 2047 ADC counts,



**Figure 15:** Pedestal measurements with 24 prototype FATALIC chips. (a) Mean and (b) standard deviation of the pedestal in the high-, medium- and low-gain channels. (c) Mean and (d) standard deviation of the pedestal in the slow channels.

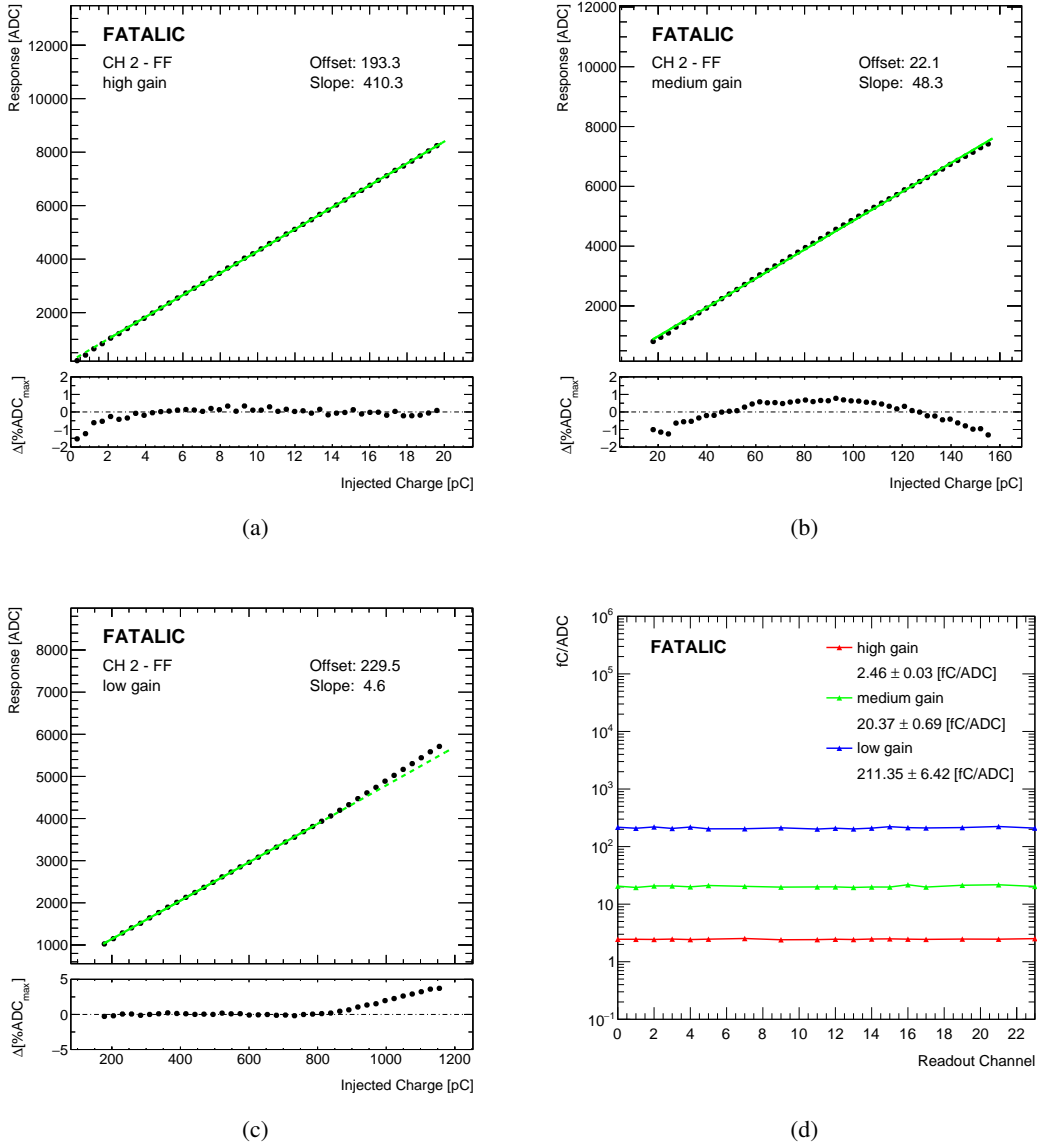
and was found to be 0.85 LSB. This measurement can also be used to estimate the noise of the analog block, by quadratically subtracting it from the noise level of the full ASIC, realistically assuming that they are not correlated. Using the noise measurements, derived with the 24 prototype chips (see Section 7.1), the estimated noise of the analog block is 2.34 LSB (significantly dominant) for the high-gain, 1.23 LSB for the medium-gain and 0.89 LSB channel for the low-gain channel.

Figure 19 compares the observed analog pulse shape, obtained by illumination of the connected PMT with a Light-Emitting Diode (LED), to the simulated pulse with which it shows good



**Figure 16:** Simulation results, showing the deviation from linearity in the (a) high-gain, (b) medium-gain, (c) low-gain and (d) slow channel.

agreement. The integral of the analog pulse as a function of the injected charge (using the CIS) is also presented in figure 19 for the three gain channels. The maximum deviation from linearity is found to be 0.4% in the high-gain, 1.9% in the medium-gain and 1.3% in the high-gain channel, up to approximately 700 pC. In this case as well, the observed linearity is significantly affected by imperfections of the CIS. The linearity for higher input charges is not comparable to that of the present version of FATALIC due to intermediate revisions in the input stage. Finally, although the dedicated output could be used to directly measure the noise of the analog block, this measurement would be significantly correlated to the noise of the scope. Therefore, the indirect estimation

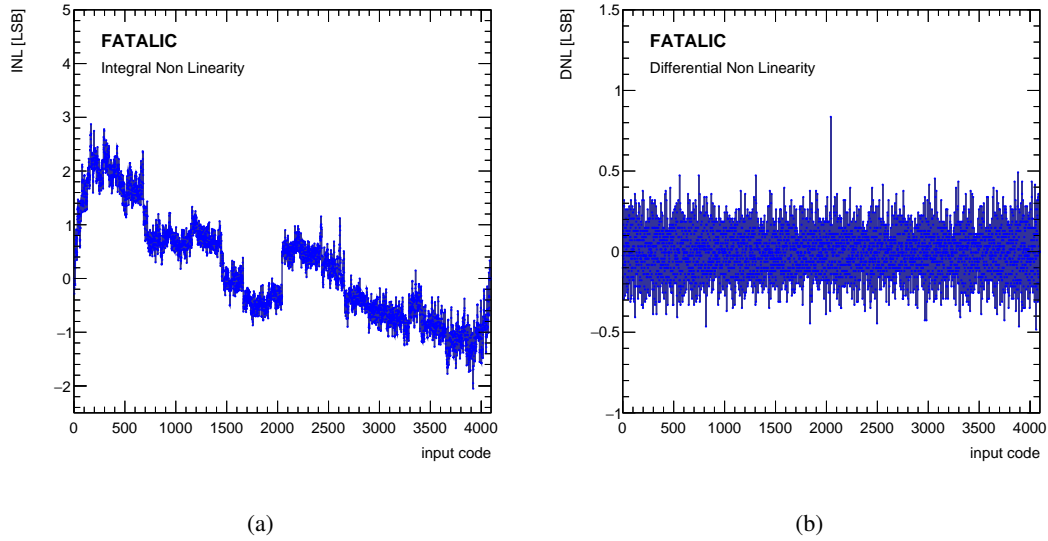


**Figure 17:** Linearity measurements using the CIS. Example showing the response as a function of the injected charge for one FATALIC chip in the (a) high, (b) medium and (c) low gain channel. (d) Summary of the measured fC/ADC conversion factors from all tested chips.

presented above is preferred.

## 7.4 Radiation tolerance

The 130 nm GF CMOS technology is recommended by ATLAS due to its high radiation tolerance in terms of Total Ionising Dose (TID). It is suitable for the development of radiation-hard chips up to at least 100 Mrad with a peak of leakage current at  $\sim 1$  Mrad. Therefore, since the expected radiation level at the HL-LHC, based on both Monte Carlo and in-situ measurements, is 50 krad

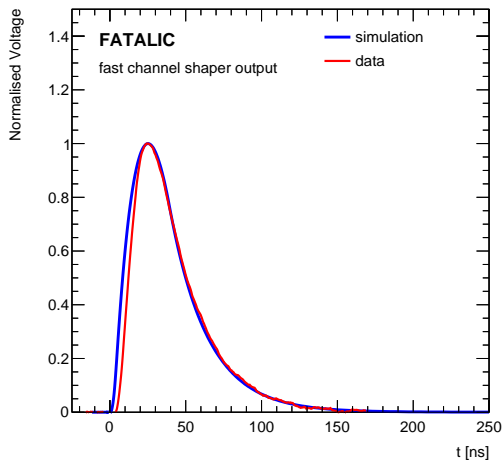


**Figure 18:** (a) INL and (b) DNL error of the pipelined ADCs.

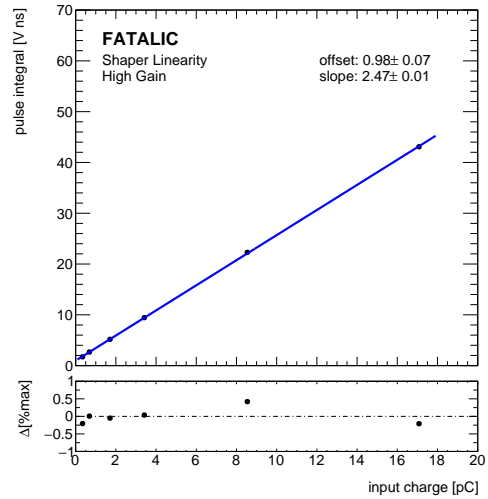
(including conservative safety factors), well below the 1 Mrad peak, no further assessment for TID or Non Ionising Energy Loss (NIEL) is deemed necessary for FATALIC. Single Event Effects (SEE) would need to be tested though for hadron fluxes up to  $8.06 \times 10^{11}$  particles/cm<sup>2</sup> (typically with 200 MeV protons), including safety factors. Finally, the associated All-in-One card and Mainboard contain Commercial Off-The-Shelf (COTS) components, which have been tested with a different FE electronic option to be tolerant for the radiation level expected at the HL-LHC. Since FATALIC was not the selected option for the TileCal upgrade, no further tests are currently planned. Table 5 lists the anticipated radiation levels for the ASIC and COTS.

Radiation	Simulation & Experiment	Safety Factors			Total ASIC (COTS)
		Simulation	Batch variation ASIC (COTS)	Low Dose Rate Effect	
NIEL [1 MeV eq. neutron/cm <sup>2</sup> ]	$2.69 \times 10^{12}$	2	1(4)	1	$5.38 \times 10^{12}$ ( $2.15 \times 10^{13}$ )
TID [Gray]	67.3	1.5	1(4)	5	505 (2019)
SEE [>20 MeV hadron/cm <sup>2</sup> ]	$4.03 \times 10^{11}$	2	1(4)	1	$8.06 \times 10^{11}$ ( $3.22 \times 10^{12}$ )

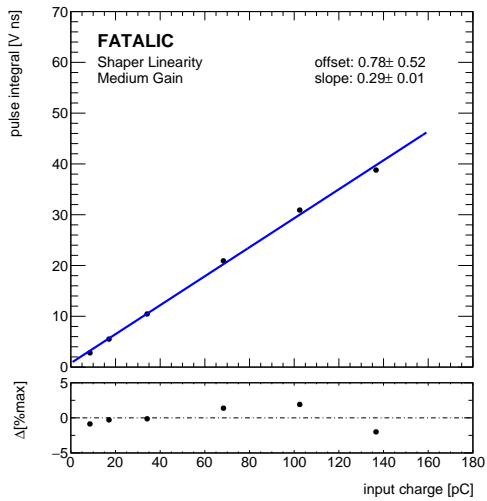
**Table 5:** Radiation levels in the worst location of the FE electronics for an integrated luminosity of 4000 fb<sup>-1</sup>.



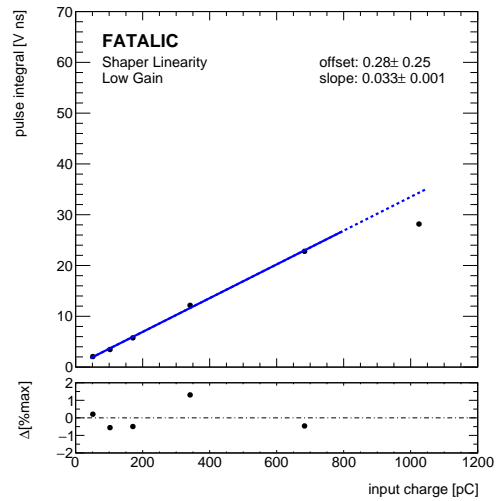
(a)



(b)



(c)



(d)

**Figure 19:** Comparison of the observed analog shaper pulse to simulation (a) and linearity of the analog block in the high-gain (a), medium-gain (b) and low-gain (c) channels.



## 8 Energy reconstruction

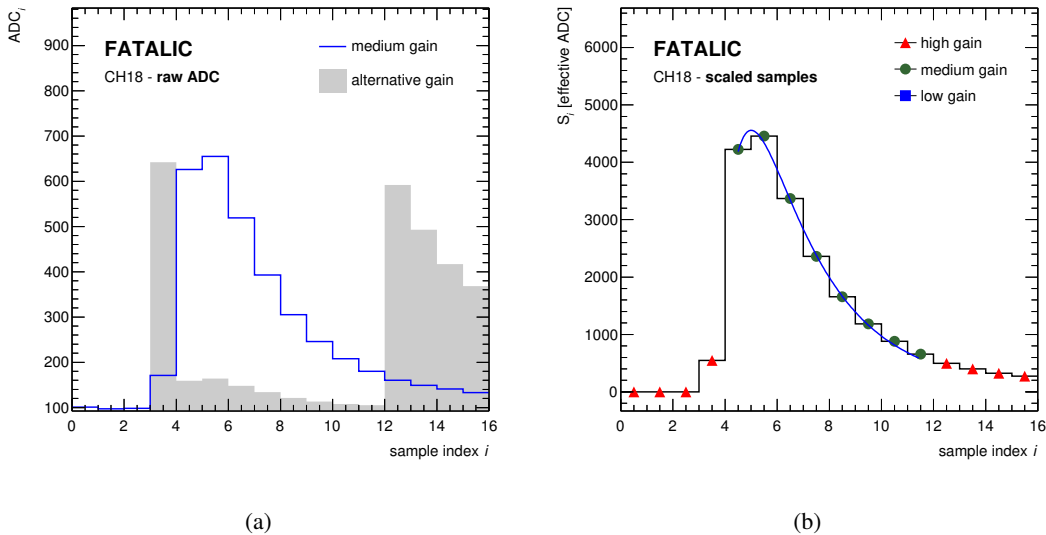
As described in Section 4, the fast channel shapers deliver an asymmetric pulse, the amplitude  $A$  of which has to be reconstructed from the set of digitised samples (typically using seven samples), collected after trigger decision. At the 40 MHz sampling rate, the second sample is expected to coincide with the pulse peak. Small time-shifts  $\tau$ , of the order of a few nanoseconds, are however possible. Both  $A$  and  $\tau$  are reconstructed by Optimal Filtering [16], a weighted sum of the digitised samples with minimum sensitivity to both correlated (e.g. pile-up) and uncorrelated noise.

### 8.1 Selection of digitised samples

The dynamic gain switch of FATALIC is exploited in order to ensure the best possible resolution for the acquisition of each digitised sample  $S_i$ . If the high-gain channel does not saturate, the ADC measurement is acquired from the alternative gain output. Otherwise, the switch turns to low gain, in which case the medium gain output is preferred. If, however, the medium-gain channel also saturates, then the alternative, low-gain measurement is used. It is noted that, once the high-gain channel saturates, the switch remains to low gain for the next seven samples (low-gain block). This is imposed through the Mainboard FPGAs to allow the high-gain channel to recover from the saturation state. Once the ADC value has been acquired, the pedestal  $p_i$  of the selected channel is subtracted and the sample is normalised to the high-gain scale. Figure 20 demonstrates a characteristic case in which digitised samples from different channels are selected.

### 8.2 Simulation of experimental effects

Simulation studies have been carried out in order to test the impact of experimental effects on the energy resolution. The latter is defined as the standard deviation of the  $(E_{\text{reco}} - E_{\text{true}})/E_{\text{true}}$



**Figure 20:** (a) ADC measurements from a 100 GeV electron beam event. (b) Selected samples, normalised to the high-gain scale, are used to reconstruct the analog pulse by Optimal Filtering.

distribution, where  $E$  refers to the deposited energy read by one of the two PMTs in a single Tile cell and the label “true” (“reco”) refers to the input (reconstructed) energy. In these studies, the Optimal Filter is calibrated with respect to the measured output pulse shape of one prototype chip. To simulate the charge-injection, this reference pulse is given random amplitudes and is subsequently sampled and digitised according to the procedure described in Section 8.1. Random noise is then added to each digitised sample, based on measurements with the same chip; 1.5 ADC counts for the low- and medium-gain channels (corresponding to 8.4 fC and 32 fC, respectively), and 3.5 ADC counts for the high-gain channel (256 fC). As shown in figure 21, the expected resolution is lower than 2% in the input range above 2 pC, while for lower values it increases up to  $\sim 7\%$ .

**Electronic noise and gain saturation.** The reference scenario described above is first compared to the ideal case where no electronic noise and/or no low-gain block is applied. The results are presented in figure 21a. The impact of noise on the intrinsic 18-bit resolution is about one order of magnitude, whereas the cost of the low gain block is less than 1% over the entire input range.

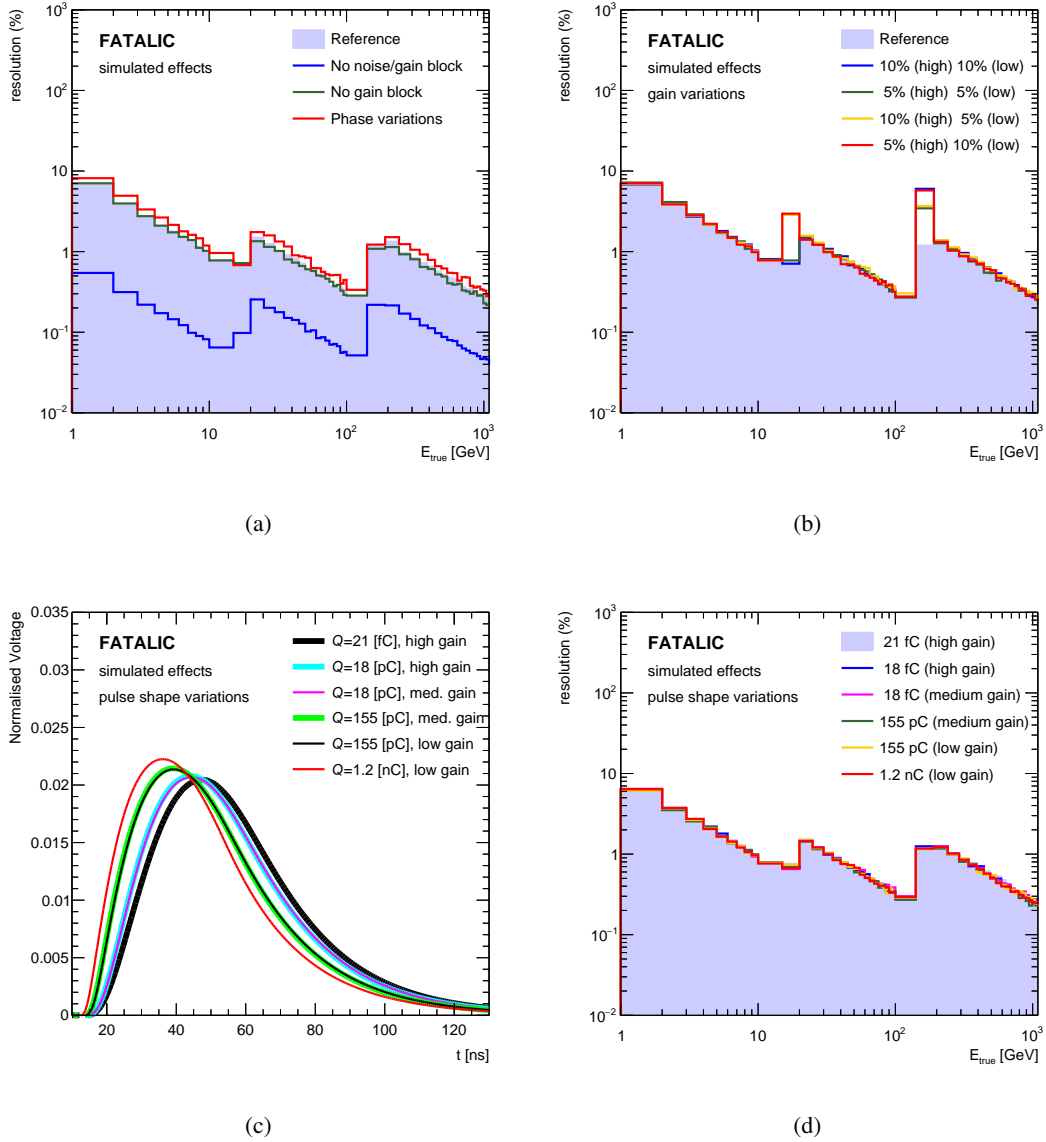
**Phase variations.** The arrival time of the pulse, with respect to the digitising clock, may vary by a few nanoseconds. To simulate this effect, the generated pulses are shifted by a random phase  $\tau \in [-8, 8]$  ns. The results (figure 21a) show that such time-shifts are accounted for by Optimal Filtering, affecting the resolution by  $\sim 1\%$ .

**Gain variations.** The impact of gain variations is tested by shifting the gain of each channel by 5% or 10%. Such variations do not affect the resolution (figure 21b) but rather introduce a shift to the reconstructed energy, which can be recovered by calibration using the CIS.

**Pulse shape variations.** Imperfections of the electronics have been found to distort the output pulse shape depending on the input charge. Figure 21c compares pulses, obtained from the simulation of the ASIC for different injected charges. These variations of the pulse shape have less than 0.5% impact on the resolution (figure 21d). However, they introduce a shift to the reconstructed energy (of less than 1%), which can be accounted for by applying a scale factor to the gain as a function of the input charge.

**Pile-up.** Inelastic  $pp$  interactions, taking place in the same (in-time pile-up) and adjacent (out-of-time pile-up) bunch crossings, introduce parasitic pulses, which contaminate the signal from the actual hard scattering. In the years 2015-2017 the average number of inelastic interactions per bunch-crossing was measured to be  $\langle \mu \rangle = 32$ , while in the HL-LHC, the nominal expected rate is  $\langle \mu \rangle = 140$  and it is foreseen to increase as much as  $\langle \mu \rangle \approx 200$ .

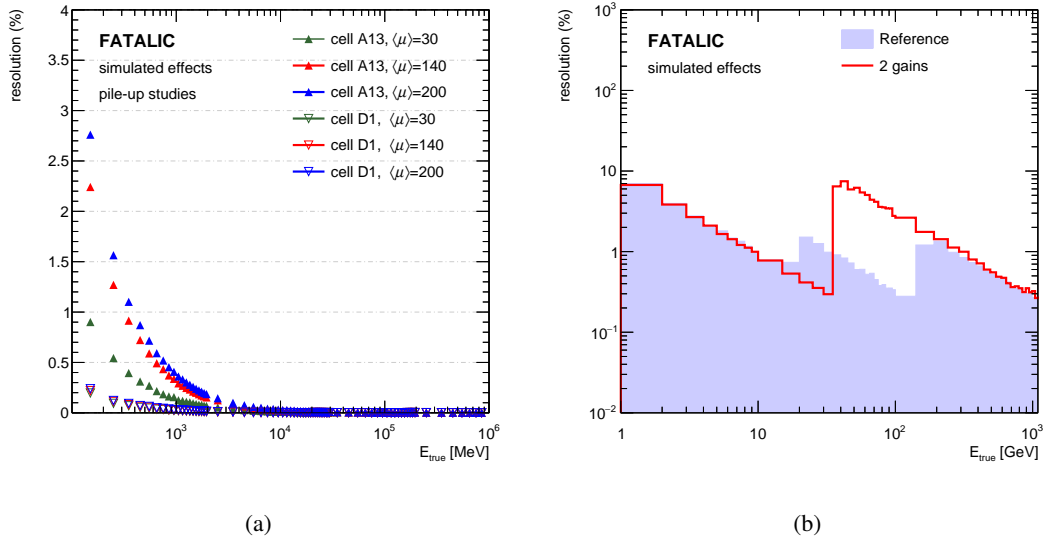
To test the performance of FATALIC in the presence of pile-up background, the description of the FATALIC readout is implemented into the official simulation software of ATLAS. Random in-time and out-of-time pile-up pulses are added to each generated signal pulse, according to the energy distribution of minimum-bias events in a given Tile cell. These distributions are available from physics simulation with different values of  $\langle \mu \rangle$ . The estimated impact on the resolution is presented in figure 22a as a function of the true deposited energy for Tile cell A13 (the most exposed to radiation from  $pp$  collisions) and cell D1 (the least exposed). It is note though that the impact can be reduced by calibrating the Optimal Filter against the correlation matrix of the pile-up background [16].



**Figure 21:** (a,b) Energy resolution as a function of the true energy in different scenarios probing the impact of various experimental effects. (c) Variation of the fast channel shaper output with the input charge and (d) its impact on the energy resolution.

### 8.3 Two-gain scenario

In order to quantify the benefit of having three gains, the scenario of using two gains with a gain ratio of 32 is explored, based on the simulation described above. Considering digitisation with 12-bit ADCs, the effective output range in this case is 17-bits. The noise is assumed to be 1.8 ADC counts for both channels. As seen in figure 22b the resolution drops by  $\sim 8\%$  in the intermediate range (40 MeV-180 MeV) which, in the case of FATALIC, is recovered by the medium-gain channel.



**Figure 22:** (a) Energy resolution as a function of the true energy for  $\langle\mu\rangle = 30, 140$  and 200, in Tile cells D1 and A13. (b) Energy resolution achieved with FATALIC, as a function of the true energy, compared to the scenario of using only two fast channels with a gain ratio of 32.

## 9 Performance with particle beams

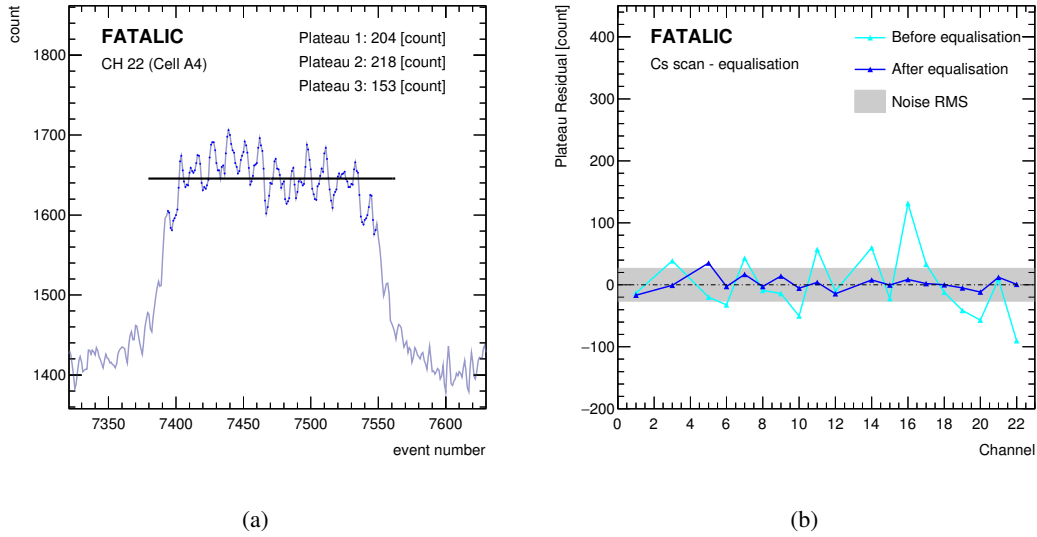
The 24 prototype FATALIC were tested in the reconstruction of real energy deposits of hadrons, electrons and muons, provided by the H8 secondary particle beam of CERN. Two mini-drawers, equipped with 12 FATALIC FE electronics each, were inserted into a demonstrator Tile module, providing full readout of Tile cells A1-5, BC1-5, D1 and partial readout of Tile cells A6 and D0. First, the detection chains were calibrated by running Cs scans, using the slow channel. The fast channels performance was then probed with particle beams of different energies and compositions.

### 9.1 Inter-calibration of readout channels

As the Cs source traverses a Tile cell, the response of the respective PMTs exhibits a characteristic plateau (figure 23a), which reflects the sequential excitation of the tiles, with local maxima (minima), generated when the source traverses scintillator tiles (steel plates). Since the energy deposited by the source is uniform, variations of the measured responses can be used to inter-calibrate the detection chains. This is performed by equalising each plateau  $p_i$  to the overall mean  $\langle p \rangle$ . Since the dependence of the PMT gain on the applied high voltage is  $\sim V^\beta$ , where  $\beta \simeq 7$  for the particular PMTs, the high voltage is corrected to  $V_i' = V_i \cdot (\langle p \rangle / p_i)^{-1/\beta}$ . Figure 23b demonstrates the plateaus before and after equalisation. As shown, residual variations are successfully reduced to the noise level and can be used to derive correction factors for each channel's response.

### 9.2 Measurement of particle deposits

The following paragraphs present the results of data analysis, using electron, muon and hadron beams, targeting the center of each A-cell at 20° incidence. The deposited energy is reconstructed

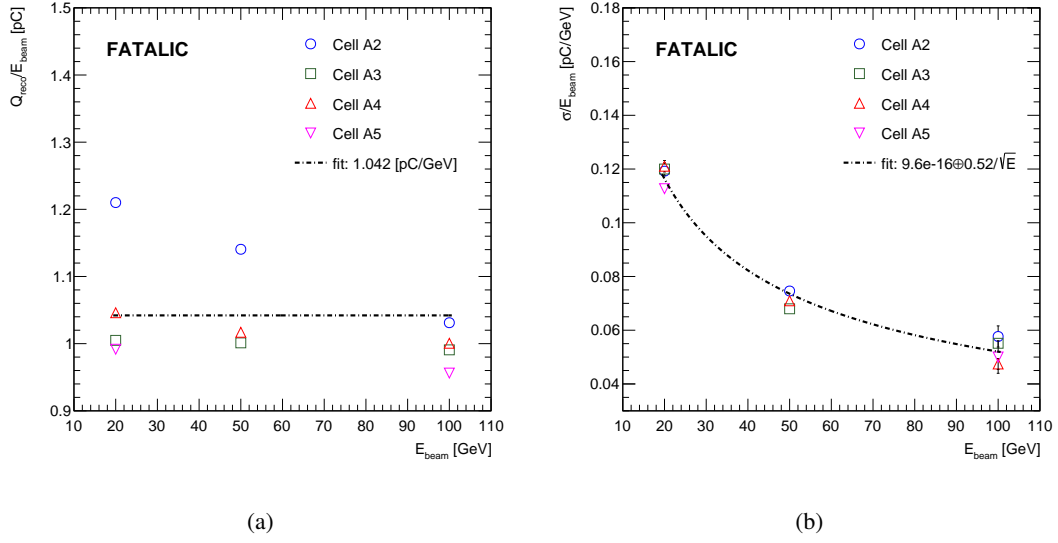


**Figure 23:** (a) Characteristic plateau, showing the response of one PMT to the Cs source signal. (b) Plateau variations before and after adjustment of the high voltage of each PMT.

using Optimal Filtering, as described in Section 8, and is expressed in units of input charge by applying the fC/ADC conversion factors, derived using the CIS. Unless specified otherwise, the deposited energy is estimated from the sum of the measurements in the targeted A and BC cell. Adjacent cells are also taken into account for containment. The average energy, deposited by a specific beam constituent, is obtained from the mean of a gaussian line-shape interpolated around the respective characteristic peak.

**Electrons.** The reconstruction of 20 GeV, 50 GeV and 100 GeV electron signal is tested with the beam targeting Tile cells A2-A5. Since the electromagnetic shower is contained within a short distance in the Tile module, the electron energy is obtained from the respective distribution in each targeted A-cell. The results are summarised in table 6 and displayed graphically in figure 24 as a function of the beam energy. Using these measurements (from 11 Tile cells), the EM scale constant is estimated  $1.04 \pm 0.1\text{pC/GeV}$ , which is consistent with the nominal value of  $1.05 \pm 0.1\text{pC/GeV}$ , derived in precise test-beam studies [15], based on more than 200 Tile cells, using electrons of different energies with  $20^\circ$  incidence. Finally, an example showing the total reconstructed energy distribution (A and BC cells combined) is presented in figure 25a, while figure 25b displays the two-dimensional distribution in the A/BC cell plane, where the characteristic deposits of the different beam constituents (electrons, muons and pions) can be distinguished.

**Muons.** The reconstruction of muon signal is tested with 165 GeV muon beams targeting cells A2-A5. The reconstructed energy distribution for a characteristic case is shown in figure 25c. The most probable values (mpv), estimated for each targeted Tile tower (A- and BC-cells), are listed in table 7. The results are also expressed in terms of energy loss per unit distance ( $dE/dx$ ), using the track length in each Tile cell (31.925 cm for A-cells and 89.391 cm for BC-cells, for  $20^\circ$  incidence).



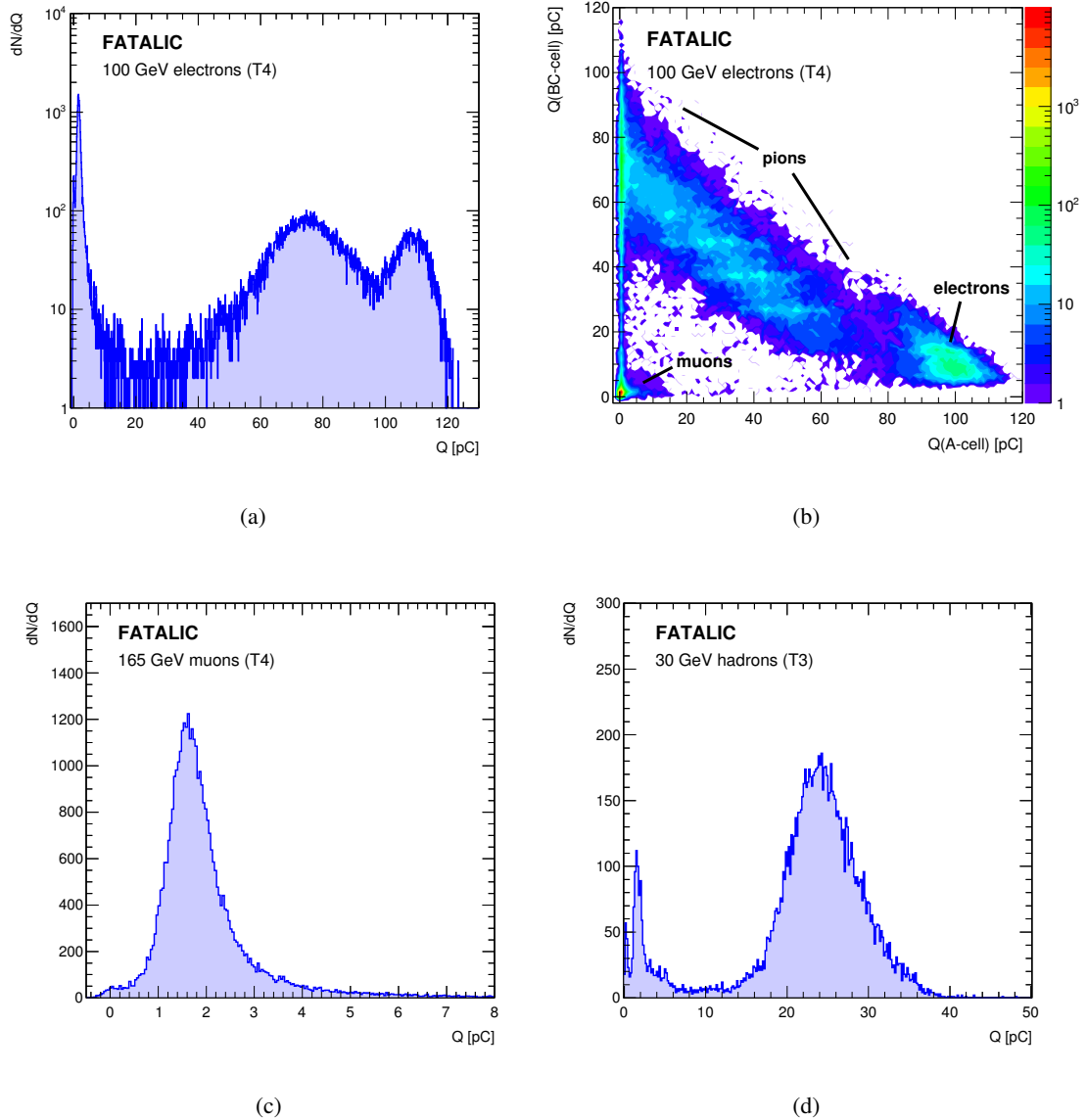
**Figure 24:** Relative mean (a) and standard deviation (b) of the reconstructed electron energy in A-cells as a function of the beam energy. Error bars represent statistical uncertainties from the gaussian fit to the energy distribution in each cell.

Beam	Cell A2		Cell A3		Cell A4		Cell A5	
GeV	$Q_{\text{reco}}$ [pC]	$\sigma$ [pC]	$Q_{\text{reco}}$ [pC]	$\sigma$ [pC]	$Q_{\text{reco}}$ [pC]	$\sigma$ [pC]	$Q_{\text{reco}}$ [pC]	$\sigma$ [pC]
20	23.2	2.3	20.1	2.4	21.6	2.5	19.7	2.2
50	54.3	3.5	50.1	3.5	52.5	3.7	-	-
100	98.2	5.6	98.7	5.5	103.1	4.8	95.1	5.1

**Table 6:** Reconstructed electron energy in the targeted A-cells.

The overall energy loss is  $14.2 \pm 1.9$  fC/cm, which corresponds to  $15.0 \pm 2.0$  MeV/cm considering the EM calibration constant of 1.04 MeV/pC estimated above and the  $e/\mu$  response ratio of 0.91. The result is consistent with the estimate of 15.2 MeV/cm, reported in previous test-beam studies using 180 GeV muons at projective angles.

**Hadrons.** Hadron signal is studied with beams of 30 GeV and 180 GeV pions targeting Tile cell A3. To account for energy leakage towards adjacent Tile cells of the same module, deposits measured in Tile cells A2, BC2, A4, BC4 are also added to the measurement. The results are summarised in table 8, while the reconstructed energy distribution for the case of 30 GeV pions is shown in figure 25d. As expected, the measured energy is lower than the beam energy, since a single Tile module cannot provide full coverage, in solid angle, of the hadronic shower. The energy leakage towards neighbouring Tile cells of the same module is found approximately 11% and 18% in the cases of 30 GeV and 180 GeV, respectively.



**Figure 25:** (a) Reconstructed energy distribution with 100 GeV electron beam targeting cell A4. (b) Two-dimensional distribution in the A/BC-cell plane, demonstrating the characteristic deposits of the different beam constituents. (c) 165 GeV muon beam targeting cell A4. (d) 30 GeV hadron beam targeting cell A3 (adjacent towers are also included for containment).

## 10 Conclusion

The above sections conclude the presentation of FATALIC and demonstrate the full potential of the 130 nm CMOS technology, realised as a FE readout electronic architecture for the strenuous conditions of the HL-LHC. The fast channels offer excellent performance for the processing of detector signals in the input charge range up to 1.2 nC, with a noise of 6.1 fC (8 fC) and linearity

Cell Type	Tower 2(+3)	Tower 3(+4)	Tower 4(+5)	Tower 5
	$Q_{\text{reco}}$ [pC]	$Q_{\text{reco}}$ [pC]	$Q_{\text{reco}}$ [pC]	$Q_{\text{reco}}$ [pC]
A	0.49	0.41	0.47	0.41
BC	1.66	1.17	1.11	1.22
A+BC	2.21	1.60	1.60	1.67
	$dQ/dx$ [fC/cm]	$dQ/dx$ [fC/cm]	$dQ/dx$ [fC/cm]	$dQ/dx$ [fC/cm]
A	15.3	12.8	14.7	12.8
BC	18.6	13.1	12.4	13.6
A+BC	18.2	13.2	13.2	13.8

**Table 7:** Reconstructed energy and energy loss per unit distance of 165 GeV muons targeting cells A2-A5.

Beam	Tower 2+3+4	Tower 3	Tower 2+4
GeV	$Q_{\text{reco}}$ [pC]	$Q_{\text{reco}}$ [pC]	$Q_{\text{reco}}$ [pC]
30	24.4	20.1	2.8
180	150.9	121.4	27.9

**Table 8:** Reconstructed energy of 30 GeV and 180 GeV pions in the targeted tower 3 and adjacent towers 2,4.

better than 1.5% (0.3%), up to approximately 850 pC, according to measurements (simulation). The disagreement between measurement and simulation is not attributed to FATALIC itself but rather to imperfections of the present All-in-One cards to support the slow-channel of FATALIC, as discussed in Section 7. The performance of the fast channels was also probed with particle beams, in which FATALIC was used to measure the energy of electrons, muons and pions, reproducing the nominal estimation of the Tile EM scale constant as well as the average energy loss per unit distance of muons traversing the TileCal.

The slow channel also exhibits the expected performance and was successfully used to process low amplitude currents in calibration scans using the Cs system, in order to correct the PMT gains in the respective readout channels. At the same time, however, it exposes the limitations imposed by the CMOS technology, along with possible directions for improvement. The main limitation is the large, approximately  $7 \text{ nA } 1/f$  noise, introduced by the input stage, which does not comply with the specification ( $<1 \text{ nA}$ ) defined for new the Tile FE electronics. The adopted, current-driven architecture is not offered for further reduction of the noise, which would therefore require migration to a different (bi-CMOS) technology or relocation of the slow channel outside FATALIC.



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