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Digital HCAL Electronics: Status of Production

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Abstract. This is a status report of the production of the readout electronics for the Digital Hadron Calorimeter (DHCAL) prototype. The prototype will be equipped with Resistive Plate Chambers (RPCs), read out with 1 x 1 cm^2 pads. The readout of each channel is simplified to provide a yes or no (digital readout) within a time bin of 100 ns. Each detector layer with an area of 96 x 96 cm^2 contains close to 10,000 readout channels. The total channel count for the entire prototype calorimeter with 38 active layers is approximately 350,000.

1. The Digital Hadron Calorimeter

To fully exploit the physics potential of a future lepton collider, operating at centre-of-mass energies of 0.5 TeV and above, requires an unprecedented jet energy resolution, of the order of a factor of two better than previously attained. The preferred approach to achieve this performance is through the application of Particle Flow Algorithms (PFAs) [1]. PFAs utilize the tracker to measure the momenta of charged particles, the electromagnetic calorimeter to measure the energy of photons and the combined electromagnetic and hadronic calorimeters to measure the energy of neutral hadrons, i.e. the neutrons and K_L^0's. The major challenge of PFAs is the association of energy deposits in the calorimeter to the charged or neutral particles originating from the interaction point. This challenge is met with the development of highly segmented or so-called imaging calorimeters [2].

In this context we develop a Digital Hadron Calorimeter (DHCAL) utilizing Resistive Plate Chambers (RPCs) as active medium. Our RPCs are based on two different designs [3] with either two or only a single glass plate. In the latter case the readout board serves as anode and closes the gas volume. The chambers use 1.1 mm thick glass as resistive plates and are operated in avalanche mode. The gas gap measures 1.2 mm and is maintained with the help of fishing lines spaced 5 cm apart.

The chambers are read out with a readout board containing 1×1 cm^2 pads and a binary (or digital) electronic readout system. The latter is based on the DCAL chip [4] (developed by Argonne and Fermilab), which has been optimized for the readout of large number of channels.

The collaboration is currently assembling a large DHCAL prototype calorimeter with the aim of validating the technological approach and of measuring hadronic showers with unprecedented spatial resolution. This paper describes the status of the assembly and commissioning of the electronic readout system.

The project is being carried out by the DHCAL collaboration [5] including 36 people from Argonne National Laboratory, Boston University, Fermilab, Iowa University and the University of Texas at Arlington. It is part of the scientific program of the international CALICE collaboration [6], which develops finely segmented calorimetry for future lepton colliders.

2. Overview of the Electronic Readout System

The electronic readout system has been optimized for the readout of large number of channels. Figure 1 shows the block diagram of the system. The 1 x 1 cm^2 pads of the pad-board are read out by a custom front-end ASIC, the DCAL III chip. Each chip handles 64 channels and applies a common threshold to all channels. The chips can operate either in high gain (e.g. for the readout of GEMs) or low gain (for the readout of RPCs) mode. The data is acquired either in triggerless (noise measurement, cosmic ray data) or triggered (cosmic ray or test beam data) mode. Each front-end board contains 24 DCAL chips and is connected via dots of conductive glue to the pads of a pad-board. The latter cover an area of 32 x 48 cm^2 and contain 1536 pads.

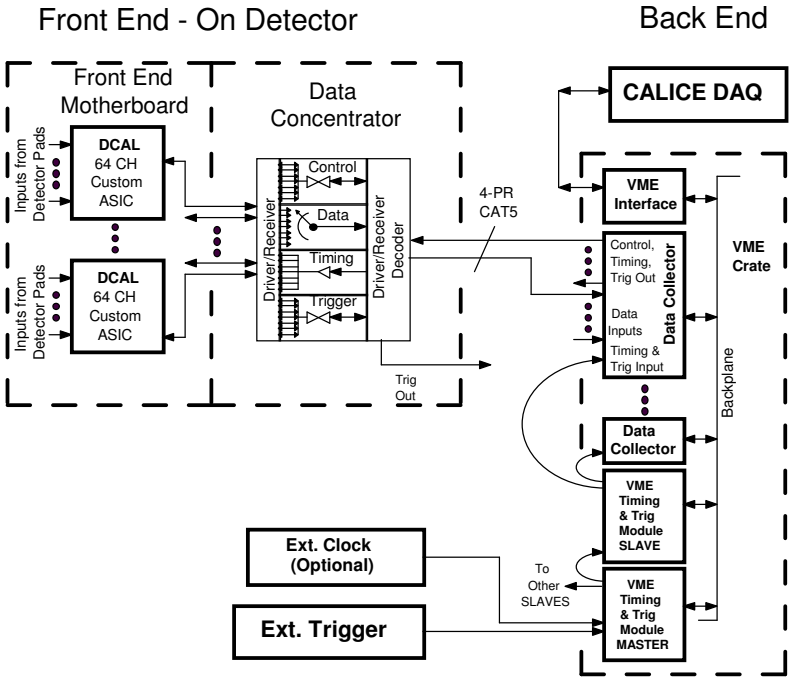

Figure 1. Block diagram of the DHCAL readout electronics.

The data from the 24 DCAL III chips are routed to a data concentrator (DCON), which is located on the edge of the front-end board. A VME-based data collector (DCOL) system receives the data from the DCONs, where each DCOL module connects to twelve DCONs or front-end boards. The entire system counts 20 DCOLs in two VME-crates. A Timing and Triggering Module (TTM) in each crate provides the necessary clock signals, resets and triggers for the front-end. An additional TTM serves as master to co-ordinate the (slave) TTMs in each crate.

3. Status of the Front-end Chip Production

The DCAL III front-end ASCIs were conceived in 0.25 μ CMOS technology. The output of the chips provides a timestamp with a 100 ns resolution and the corresponding hit pattern of its 64-channels. An engineering run produced eleven wafers with of the order of 10,300 parts. Of these a small number of chips were tested extensively on the bench. As an example of these tests Fig. 2 shows

the S-curves for the 64 channels of a chip. Notice the sharp transition from 0 to 100 counts and the tight distribution of the curves. The bench tests failed to identify a single design flaw.

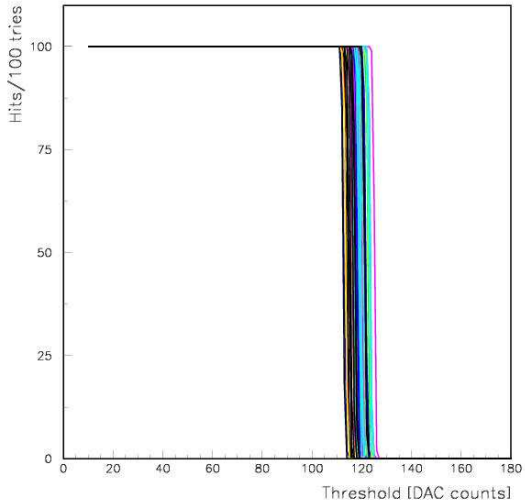

Figure 2. S-curves as measured with the DCAL III chips. The chip was operated in high gain mode and the charge was injected internally.

Before use in the assembly of the front-end boards, all chips were tested at Fermilab with the help of a robotic system, see Fig. 3. Of the initial 10,300 chips 8,644 passed the tests with zero errors, corresponding to an (average) yield of 84%.

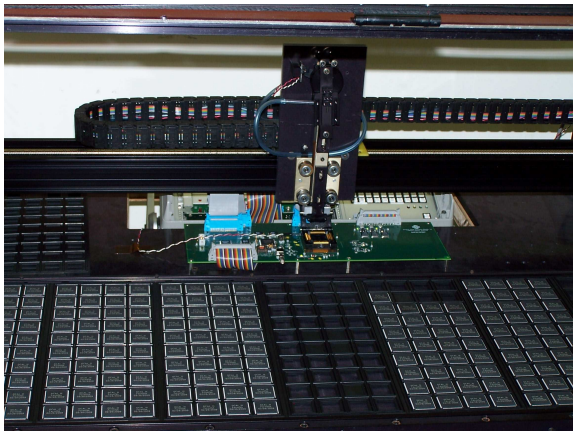

Figure 3. Photograph of the robotic system testing the DCAL III chips.

4. Status of the Front-end Board Production

The front-end boards have been produced and are currently being assembled. Figure 4 shows a photograph of such a board. The darker area of the board indicates the data concentrator part. The firmware for the DCONs has been written and is entirely debugged. The boards have been operated without single malfunctioning for several weeks.

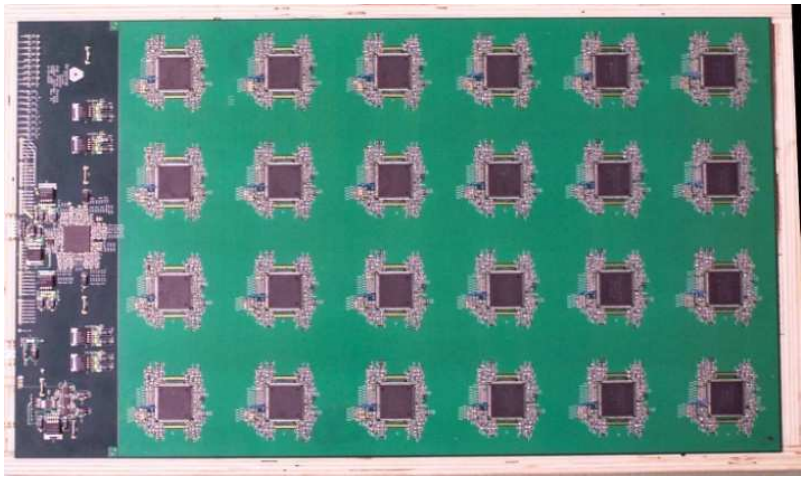

Figure 4. Photograph of a production front-end board containing 24 DCAL III chips.

The pad-boards are currently being fabricated. Since the boards do not contain any active components, no assembly is required.

A fixture for applying the glue dots to connect the front-end boards and pad-boards has been designed and built. To date of the order of 20/228 boards have been successfully glued. The operation takes approximately 55 minutes/board. With further improvements to the gluing fixture the required time is expected to be reduced by about a factor two.

The first cassette containing three RPCs and six front-end boards has been assembled. Figure 5 shows a photograph of the cassette with the top-cover removed to show the location of the front-end boards. The cassette has been operated for several weeks without problems of readout errors.

Figure 5. First detector cassette with six front-end boards. The top cover has been removed to show the location of the front-end boards.

5. Status of the Back-end Production

The data collector system has been fabricated, assembled and tested. The firmware is written and has been completely debugged. This work was carried out by Boston University.

The Timing and Triggering Modules (TTMs) required some modification compared to what was used in previous small scale tests [7]. In order to synchronize the clocks and the readout of separate VME-crates one TTM is configured to act as a master, fanning out the signals to slave TTMs, one per VME-crate. The modifications have been implemented into the design and the boards have been fabricated and (in part) assembled. The boards have been tested and perform as expected. The design work and the development of the firmware have been carried out by Fermilab.

6. Status of the Low-Voltage Power Supply

The operation of the front-end boards requires +5 Volts. The power is generated by Wiener power supplies and subsequently is distributed to the front-end boards. The distribution boxes have been designed and assembled. Figure 6 shows a photograph of one pair of power supply and distribution box. For safety reasons, each power line is separately fused.

Figure 6. Photograph of a Wiener power supply with the power distribution box located underneath.

7. Conclusions

The electronic readout system for a Digital Hadron Calorimeter (DHCAL) with Resistive Plate Chambers (RPCs) as active elements has been designed and developed. The system is optimized for the readout of large number of channels and utilizes the DCAL III chip for the front-end.

Production of the system for a large prototype calorimeter, with of the order of 350,000 readout channels, is ongoing. Particular care was devoted to thorough tests at every step in the prototyping process. Construction of the system is expected to be completed in early summer 2010 and will be followed by several running periods in the Fermilab test beam.

8. Acknowledgements

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