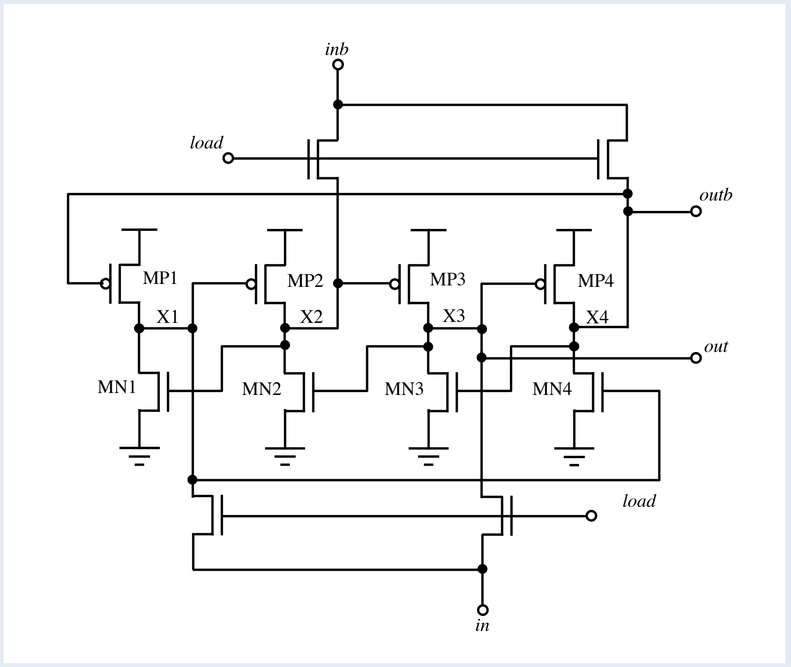
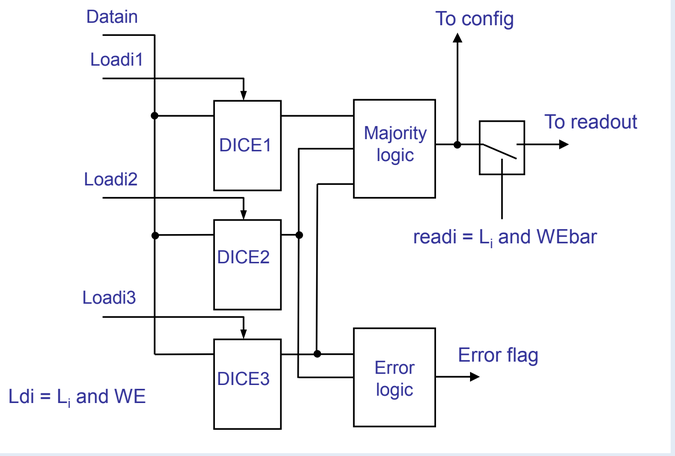
# Single Event Upsets (SEU) in the ATLAS IBL Front End ASICs

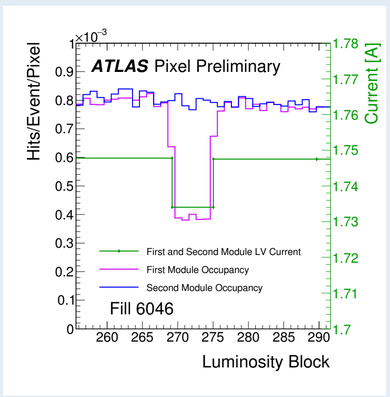
- LHC delivered in 2015/2018 total of 98 $fb^{-1}$ integrated luminosity to ATLAS for 13 TeV pp collisions.
- Maximum of 2.14 $10^{34}$ $cm^{-2}$ $s^{-1}$ peak stable beam luminosity.
- Up to 0.77 $fb^{-1}$ luminosity delivered per LHC fill.
- Pixel detector operated at extremely high-radiation environment, in particular Insertable B-Layer (IBL) at R=3.3 cm.
- IBL pixel front end chip FE-I4-B in 130 nm technology was designed with Single Event Upset (SEU) hard configuration memory.
- Inside the pixels Dual Interlocked Cell (DICE) latches were used.



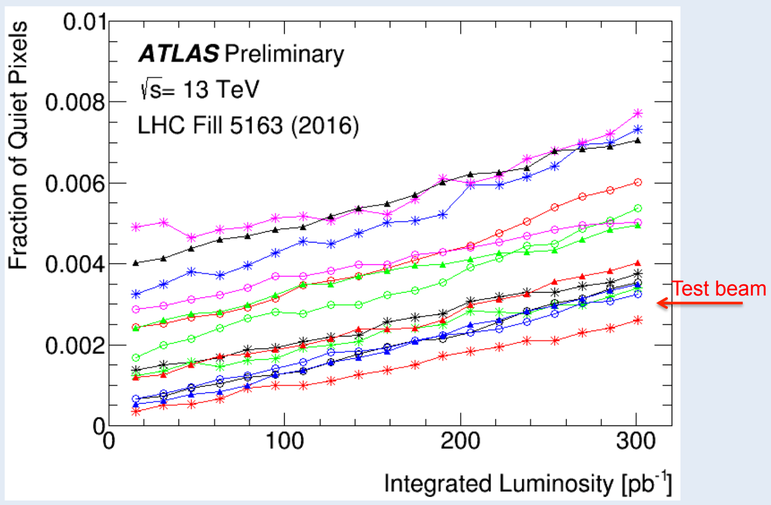

- DICE latches have redundant storage nodes and restore the cell original state when an SEU error is induced in a single node.
- Cross coupled inverter latch structure with four nodes (X1-X4) stores data in two pairs of complementary values.
- If positive upset pulse on X1, than transistor MP2 is blocked, avoiding propagation of this perturbation to node X2.
- The SEU immunity is lost if two sensitive nodes (for example X1-X3) change the state by single particle impact.
- The tolerance to SEU is increased by Hardened By Design (HBD) approach: spatial separation of critical nodes, isolated wells, guard rings and interleaving of cells.
- Global configuration memory is further protected by triple DICE latches with addition of simple majority logic.



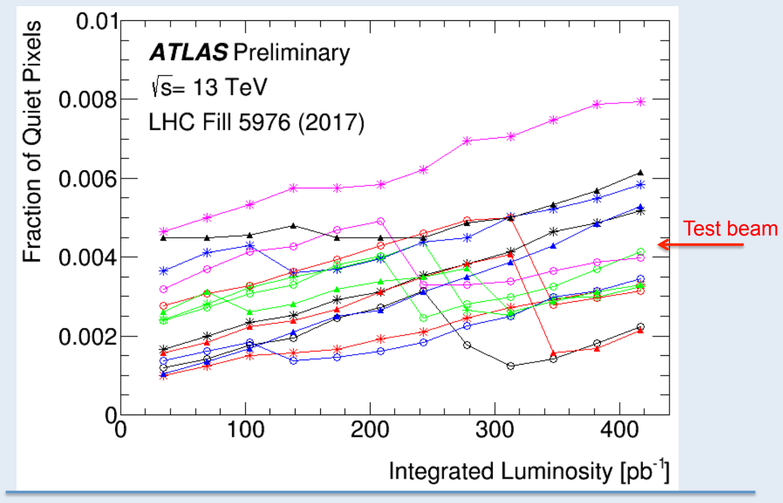

- Global Registers (GR) corruption has big impact on module operation: change of the low voltage consumption, silent modules, desynchronized modules.
- Refreshing of the GR during Event Counter Reset (ECR, ATLAS wide common signal to reset the event counters) signals restore proper function of the module.



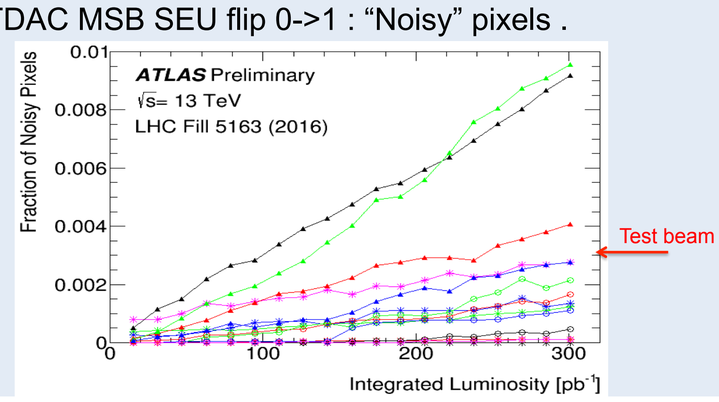

- Pixel local configuration: 13 bits/pixel: Enable, TDAC (thresholds 5 bits), FDAC (feed back current 4 bits), HitBus, Injection Caps (2 bits).
- SEU DICE cross-section measured for FE-I4-A in the 24 GeV proton test beam is 1.1 $10^{-15}$ $cm^{-2}$ (enable bit, 0 ->1 transition).
- Hadron flow at IBL predicted by PYTHIA/FLUKA simulation tuned to ATLAS data: 92.5 $10^{11}$ $cm^{-2}/fb^{-1}$ hadrons with E>20 MeV at planar modules.
- Expect 274 pixels/$fb^{-1}$/chip SEU flips of Enable bit 0->1
- Enable bit SEU flip 1->0 : “Quiet” pixel.
- 2016: no auto-reconfiguration, linear rise of quiet pixels.



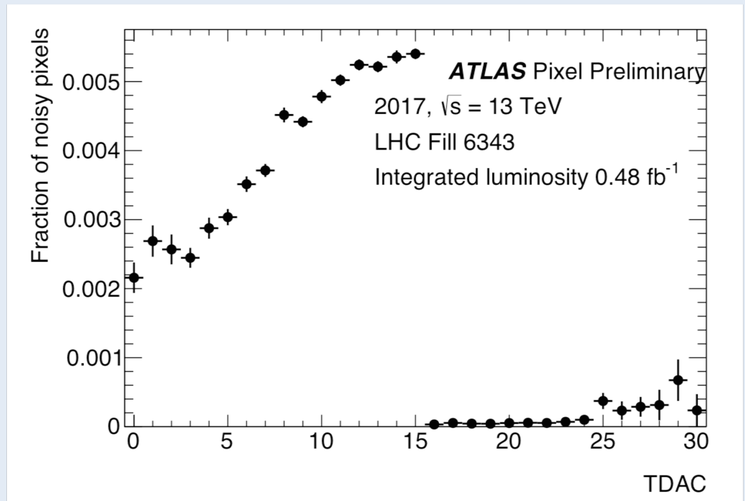

- 2017: auto-reconfiguration actions drops the number of quiet pixels in the middle of the fill.



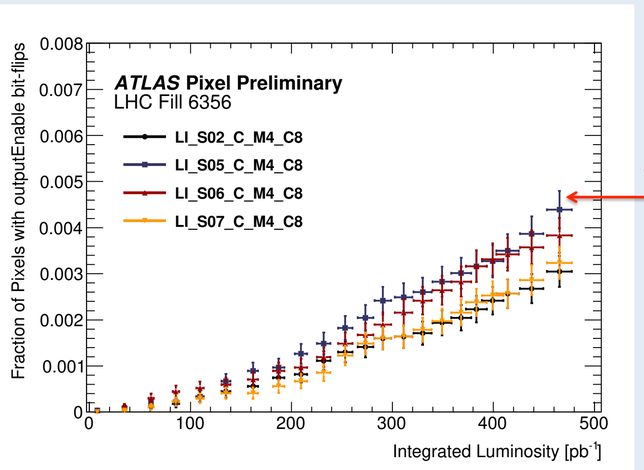

- TDAC MSB SEU flip 0->1 : “Noisy” pixels .



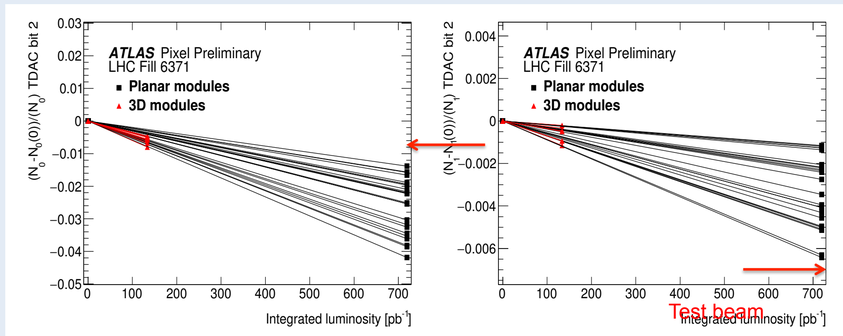

- Correlation of noisy pixels with initial TDAC value.
- Low TDAC values correspond to high thresholds.
- Biggest fraction of the noise happens after SEU flip 0->1 of MSB of TDAC, which sharply reduces the pixel threshold and increases the noise.



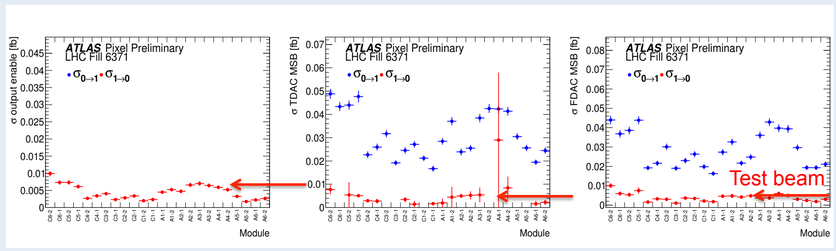

- Test with four 3D modules with all Enable bits set to “0”. During LHC fills some bits are fliped by SEU to “1”.




- TDAC bit#2 transitions 0->1 are more frequent than 1->0 transitions when measured with read back method.




- Variation of SEU in the modules along the stave for “Enable”, “TDAC MSB” and “FDAC MSB” bits with read back method.
- Transitions “1->0” are consistent with test beam results, transitions “0->1” are factor of five higher.




- ATLAS Pixel detector with IBL at R=3.3 cm efficiently operates at high luminosity with expected SEUs.
- Global configuration SEUs mitigated by refreshing the memory during ECR every 5 seconds without dead time.
- Local pixel memory SEUs in the enable bit and 1->0 transitions in TDAC and FDAC are consistent with test beam results.
- SEUs with 0->1 transitions in local TDAC and FDAC are five times higher than test beam results. Probably due to Single Event Transients(SET) glitches.
- Plans to introduce the gradual refreshing of Local pixel configuration during ECR in 2018.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