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Testing and Installation of ZEUS Leading Proton Spectrometer Detector Planes

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Abstract
The assembly and testing of the components which make up a detector plane for the Leading Proton Spectrometer is described. The spectrometer, a part of the ZEUS detector, utilizes single-sided DC-coupled silicon strip detectors and custom VLSI frontend electronics for readout.

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Introduction

The Leading Proton Spectrometer (LPS) [1] is a silicon-based tracking device that is part of the ZEUS experiment at HERA, the first electron-proton colliding beam facility. The LPS is located in the forward proton beam line to tag protons after they have passed through the interaction point (IP). The main goal is to measure the momentum of the protons and to indicate that the proton remained intact - tagging a class of events known as diffractive events. Many references [2] have described the physics motivation in detail.

The spectrometer as designed consists of 6 stations starting at 23.9 m from the ZEUS interaction point (IP) and continuing out to 90.0 m (see Table 1). Each station has 6 detector planes; stations S1, S2 and

Table 1. Stations of the LPS spectrometer and plane characteristics.

Station	z position (m from IP)	Number of layers	Strip angle	Number of channels	Strip pitch (μm)	Number installed summer 1993
S1	23.9	2U	+45°	960	81	0
		2V	-45°	960	81	0
		2Y	0°	640	115	0
S2	40.6	2U	+45°	1024	81	0
		2V	-45°	1024	81	0
		2Y	0°	576	115	0
S3	49.0	2U	+45°	960	81	0
		2V	-45°	960	81	0
		2Y	0°	576	115	0
S4	62.9	4U	+45°	1024	81	4
		4V	-45°	1024	81	3
		4Y	0°	704	115	0
S5	81.1	4U	+45°	960	81	2
		4V	-45°	960	81	0
		4Y	0°	576	115	0
S6	89.9	4U	+45°	960	81	2
		4V	-45°	960	81	0
		4Y	0°	448	115	0

S3 have the planes inserted from the side (a total of 18 detector modules) whereas stations S4, S5 and S6 have 6 planes coming from the top and also the bottom (a total of 36 detector modules). There are 2U (+45°), 2V(-45°) and 2Y (0°) planes per station. The detector planes are located within Roman pots [3], devices which allow the quick and accurate insertion and extraction of the planes to within several centimeters to the beamline.

This paper will describe the assembly and testing procedures of the detector planes, concentrating on the on-plane readout electronics and whole plane tests. Also, a summary of the current status of the installation of the planes into the HERA tunnel will be presented.

Detector Planes

A schematic drawing of a fully assembled detector plane is shown in Figure 1. The components are: a detector, a supporting hybrid, surface-mount components, a set of analog amplifier/comparator chips and a set of digital data storage chips. Each of these components were tested individually before being made available for the assembly process. A brief description is given here of the characteristics and tests made.

The detectors are single-sided, DC-coupled silicon strip detectors manufactured by Canberra(S4) and Micron(S5). The most unusual feature of the detectors is the semi-elliptical cutout at the bottom of the detector which matches the 10σ beam profile determined separately at each station with extensive beam transport studies. The detectors were screened for overall leakage current and bad channels.

The "hybrid" is a printed circuit board manufactured at CERN. It provides the fan-out of calibration and voltage lines to the electronics, support and voltage distribution for the detector and has small water cooling pipes mounted on it to carry away the heat generated in the electronics. The surface mount components are resistors, capacitors and inductors for filtering the various power busses. Each hybrid is systematically checked for shorts and opens before use; the layout is different for each station as both the detector shape and the roman pot dimensions are different.

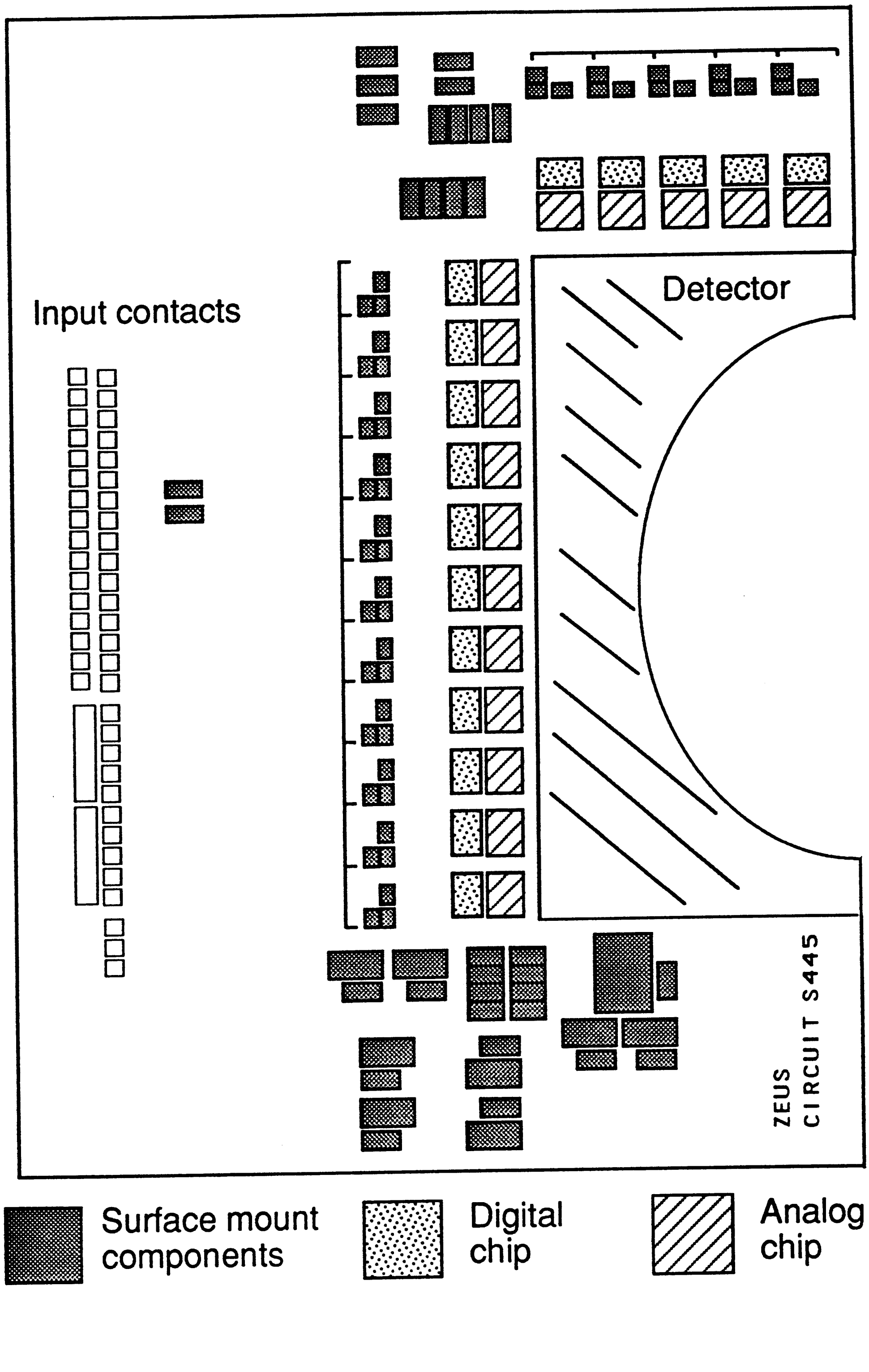

Figure. 1 Schematic drawing of an S4 detector plane.

The 64-channel analog amplifier/comparator chip (TEKZ) is manufactured by Tektronix using SHPi bipolar technology [4]. The design goals included low noise (ENC of <1000 electrons), low power (2.5 mW/channel) and radiation resistance. A scan of occupancy versus threshold voltage for channels on unmounted chips showed a gain of 167 ± 7 mV/fC and a noise of 660 ± 80 ENC. The chip has been shown to be radiation resistant [5] up to 5 MRad of protons or photons. Four calibration lines are fanned out to each chip and then to each channel which has a small capacitor (approx 14 fF) at the input. The input signals from the detector pass through a 2-stage amplifier, then reach a comparator which is AC-coupled to the amplifier stage. The comparator threshold is set to the same value for each channel on the hybrid. The output of the channel is a voltage level which says whether the strip was hit or not.

The digital time-slice chip (DTSC) is a 64-channel data-buffering storage device that is realized in a rad-hard CMOS process by UTMC [6]. The main design aims were low power consumption (<5mW/channel) and compactness. The final chip uses 2.3 mW/channel and the 64-channel chip has a size of 3.6 mm by 5.4 mm. The system runs at 10 MHz, although the DTSC has been successfully tested up to 20 MHz. The function of the DTSC is to accept the digitized output of the TEKZ and to store the data until a level 1 trigger decision is made. It does this using a 64-deep FIFO. If a trigger accept is received, it then stores it in a 32-deep buffer until the level 2 trigger signals that it should be sent to the output bus. Various data, control and power lines are supplied by the hybrid to the DTSC.

Assembly steps

Table 2 gives an outline of the steps used to assemble the hybrids and components into working detector planes. Most of the testing steps are done in the labs at UC Santa Cruz, whereas gluing the chips and all the bonding is done at PROMEX [7].

The threshold scan test is used at various points in the assembly procedure and is similar in technique to that described in detail in Ref. [8]. A prototype of the readout system used at HERA is run by a MacIntosh computer. A sample output for a channel is shown in Figure 2 where the threshold voltage was varied for two different

Table 2. Assembly steps for an LPS detector plane.

0.	Gather components that have passed their own quality checks.
1.	Attach cooling strips and recheck for shorts and planarity.
2.	Glue DTSCs and TEKZs to hybrid. Solder surface-mount components. Bond chips to control/voltage lines and each other.
3.	Run threshold scan test. Diagnose and fix bad channels (if possible).
4.	Align and mount detector on hybrid. Recheck planarity.
5.	Bond detector to TEKZ inputs.
6.	Run threshold scan test again. Debug new problems.
7	Run laser scan of the detector.
8.	Run an extended "burn-in" test and redo threshold scan.

input charges (1 fC and 2 fC), allowing a measurement of the noise (the width of the 1 fC curve) and gain (the difference between the V(50%) points). Typical values (before channels were connected to detectors) were 150 mV/fC for the gain and 625 ENC for the noise, comparable to the values obtained with the unmounted chips. On the hybrids tested so far, the typical number of bad channels was <1%, most of which were due to problems in the electronics.

To verify that each channel was collecting signals properly, a laser system was set up to simulate a minimum-ionizing particle traversing the detector. The details of the setup are described in Ref. [7]. A laser generates a 2-3 ns pulse with a wavelength of 1064 nm. An optical system in combination with an Alessi probe station allows a final spot size of 20 μm. The energy deposition is almost uniform through the 300 μm silicon detector. The spot was focussed on each strip in turn (using a computer controlled stage), the laser was pulsed 50 times and the number of times the strip registered a hit

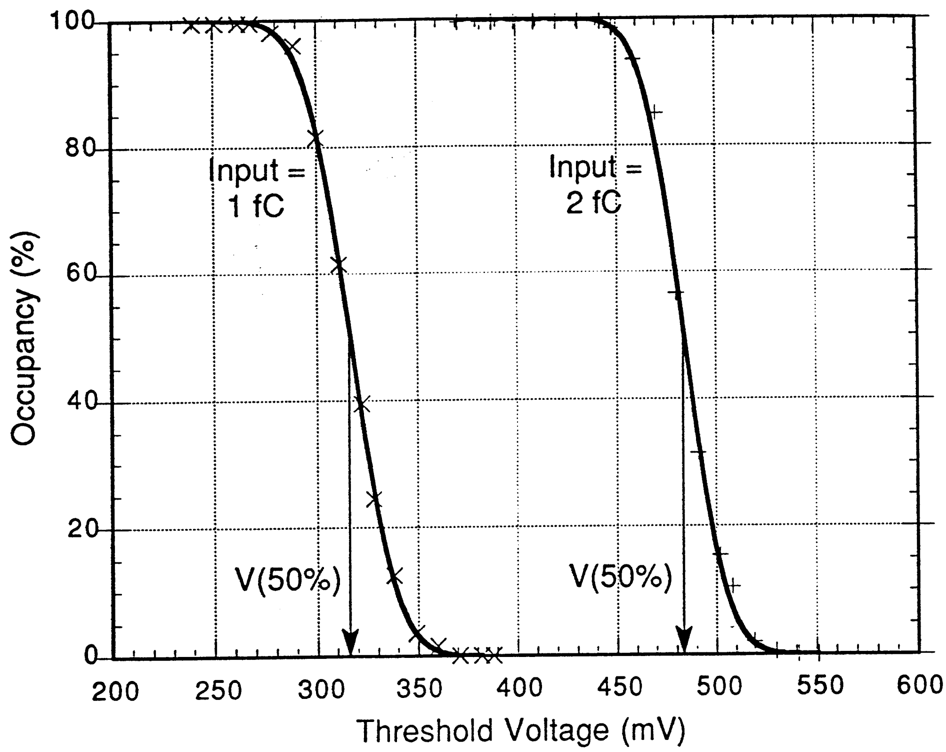

Figure. 2 Output of the threshold scan for a typical channel.

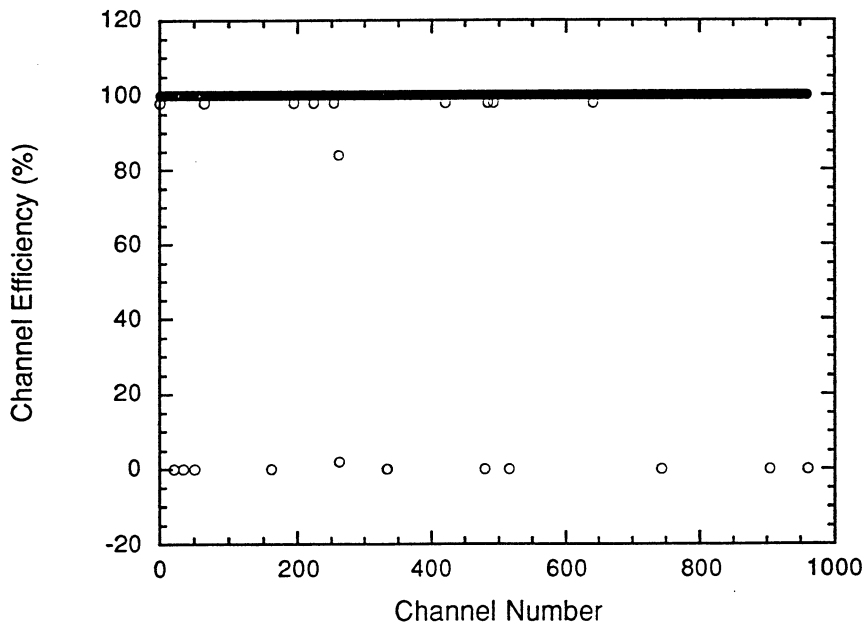

Figure. 3 Efficiency from a laser scan of a typical detector. There were 960 channels on this detector plane.

was recorded. Figure. 3 shows this efficiency as a function of channel number for one of the detectors tested.

Finally, the fully assembled detector planes were run with the clocks at full speed for a period of time to "burn-in" the system. No bias voltage was put on the detectors so the noise caused channels to fire randomly, exercising the DTSC. At the end, the threshold scan test was run again.

Installation status

A partial system has been installed in the HERA tunnel for the summer 1993 run; Table 1 lists the positions that have detector planes. The multi-station partial system will be used to integrate the LPS readout into the ZEUS data aquisition system. The production of more detector planes is progressing.

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