PROCEEDINGS OF SCIENCE

Performance of CATIA ASIC, the APD readout chip foreseen for CMS Barrel ECAL electronics upgrade at HL-LHC

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ABSTRACT: The CMS ECAL barrel electronics will be upgraded for the HL-LHC to meet the latency and bandwidth requirements of the Phase-II Level-1 trigger system. The new front-end electronics will mitigate the increasing noise from the avalanche photodiodes (APDs), discriminate against anomalous APD signals and provide improved timing information. The foreseen solution is to replace the current Charge-Sensitive-Amplifier with a Trans-Impedance Amplifier, which should provide the extra bandwidth needed to maintain the integrity of the detector signal shape. The first ASIC prototype, called CATIA, has been successfully designed in TSMC 130 nm CMOS technology and its test results will be presented.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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PoS(TWEPP-17)036

1. Introduction

The LHC Phase-II upgrade will lead to a significant increase in luminosity, which implies the full replacement of the ECAL Barrel (EB) electronics to meet the Level-1 trigger requirements. Including the very front-end (VFE) electronics in this upgrade can bring significant benefits. The first benefit is to mitigate the increasing noise induced by avalanche photodiode (APD) ageing. In addition, one can expect to improve the suppression capability of signals directly generated into the APD by crossing particles (anomalous APD signals named "spike" signals) and to reach the intrinsic timing resolution of the detector constituted by crystals and APDs, in order to help discriminate between energy deposits coming from different overlapping events. Extensive studies have been made to find the best architecture to cope with the conditions imposed by the HL-LHC. The conclusion is to replace the charge sensitive amplifier (CSA) of the MGPA [1] by a trans-impedance amplifier (TIA) which maintains the integrity of the APD signal shape necessary to discriminate the spike signals and to limit the output bandwidth of the system to a maximum of 50 MHz. The time resolution will be achieved by using a new 12-bit ADC operating at a sampling rate of 160 MHz (Figure 1).

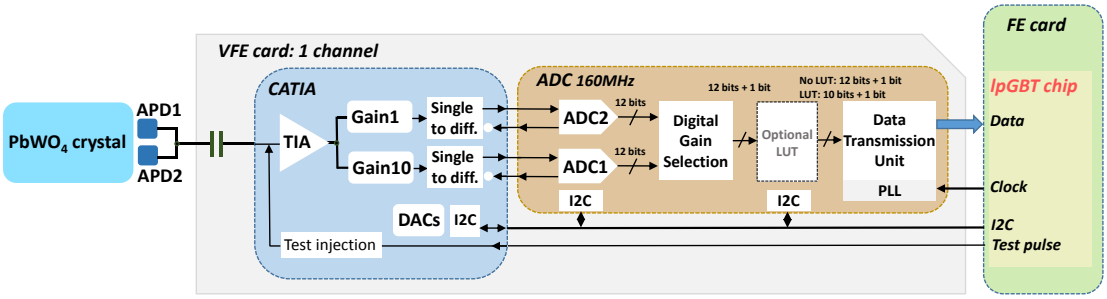

Figure 1: New VFE electronics is formed with CATIA ASIC [Trans-Impedance Amplifier (TIA) with two gain ranges (1 and 10) and 50 MHz of bandwidth (RC of 3 ns)] and 12-bit ADC [two channels sampling each at 160 MSPS].

To validate these studies, two developments have been launched in 2016, one by using discrete components and the other by integrating a circuit called CATIA for which the design and test results are presented in this paper.

2. CATIA architecture

The APD signal processing is done in three functions (Figure 1). The first is to convert the input current signal into a voltage signal by using high speed TIA. The second is to split the output dynamic range into two sub-ranges: 200 GeV and 2 TeV by using two differential amplifiers with different gains called Gain1 and Gain10. Their outputs are filtered with a low pass filter (fc = 50 MHz) and the common mode output voltages are controlled and adjusted to meet the input characteristics of the ADC used to achieve the digitization in the last step of the processing. For the first ASIC prototype, it has been decided to integrate only the TIA part with the two gains in a single-ended output version. This prototype permits the study of the characteristics and performance possible to obtain with the TSMC 130 nm technology. In order to optimize the dynamic range of the TIA, two versions have been designed using different transistors for each according to the voltage supply used: 1.2 V or 2.5 V.

2.1 TIA architecture

The architecture of the TIA is a Regulated Common-Gate (RCG) or Regulated Cascode stage [2] represented in Figure 2. This architecture offers a reduced input resistance compatible with the high input capacitance (200 pF) providing the high bandwidth that is foreseen (50 MHz). It is realized by a common-gate stage (transistor M1 polarized by Ip1 current source and load resistance Rc) to which a loop is added containing a voltage amplifier (common-source transistor M2 with active load Ip2). This topology has the benefit of dividing the input impedance by this amplifier gain. Thus, we can obtain an input impedance as low as 1 Ω with the TIA integrated in CATIA.

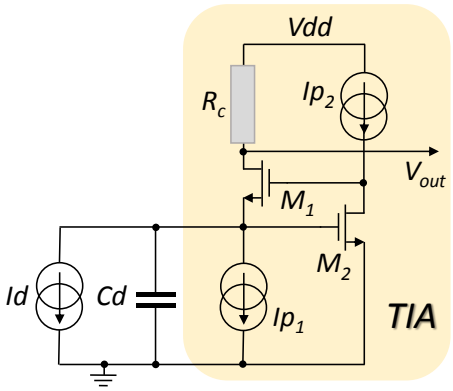

Figure 2: Architecture of the TIA.

The trans-impedance gain is made by the Rc resistor and its value is a trade-off between noise and linearity. On one hand, the gain value is minimized by design in order to preserve the requested linearity (INL < +/- 0.1 %) according to the maximum intensity of the input current. On the other hand, the largest possible value of Rc will permit to reduce the gain and noise contributions of the two output gain stages necessary to fit the ADC input dynamic range. As this technology offers the two supply voltages of 1.2 V and 2.5 V, two TIA versions have been included in CATIA. The Rc value is 136 Ω for the 1.2 V version and 273 Ω for the 2.5 V version, which give at 2 TeV respectively 610 mV and 1220 mV as the maximum dynamic range for the Gain1 channel (the same output dynamic range was set at 200 GeV for the Gain10 channel). The TIA gain is expected to be measured channel by channel to compensate for process variations. In a RCG architecture, the linearity is mainly achieved by avoiding the M1-M2 stage to work in saturation mode.

3. CATIA test measurements

The CATIA chip has been submitted in October 2016 and received in February 2017. The first test has been made in laboratory with a pulse generator to control the functionality of the chip and to check its performance. The measured transfer function of the Gain10 at 1.2 V is 1.358 mV/µA (- 8% less than simulation results) for an INL of +/- 0.35 %. The measured bandwidth is 200 MHz, which enables a global bandwidth of 50 MHz (APD to ADC input).

In addition to the pulse generator input, CATIA has been tested with the current ECAL APD through the legacy motherboard and kapton cable, which will not be replaced for the upgrade. The high value of kapton inductance (75 to 100 nH) means that a resistor of 20 Ω is required at

the CATIA input and, therefore, to reduce the bandwidth to about 35 MHz. The figure 3 shows the response of Gain1 and Gain10 at 2.5 V to sub-ns laser pulses, with the amplitude of Gain1 renormalized to Gain10. The response is stable, with a small overshoot, for a measured bandwidth of 32 MHz.

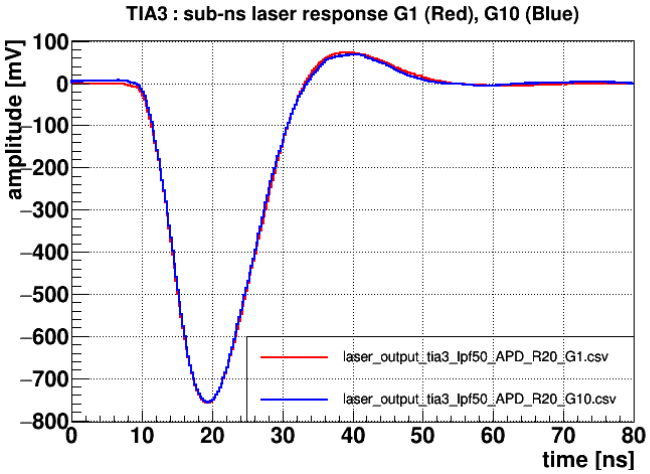

Figure 3: Signals measured at the output of Gain1 and Gain10 stages.

The noise spectral density of CATIA has been also measured (Figure 4) and is very similar to the simulation result. The good agreement between both is confirmed by the RMS noise value, identical in the two methods (noise ≈ 510 µVRMS).

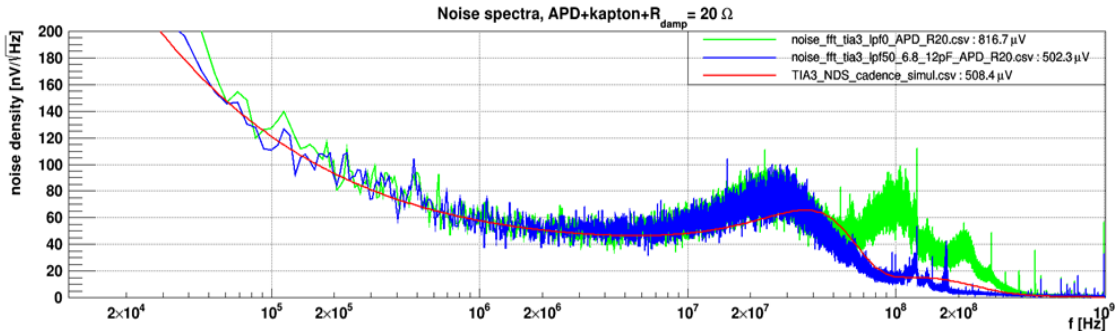

Figure 4: Noise spectral density of CATIA connected to APDs as in ECAL. In green without bandwidth limitations, in blue with a low pass filter at 50 MHz[1] and in red the simulation results ([1] optimal TIA output filter frequency to limit the TIA noise bandwidth).

4. Conclusion

The trans-impedance amplifier foreseen for the CMS Barrel ECAL electronics upgrade Phase-II has been produced and fully tested in laboratory. The results are consistent with expectations from simulations and prove the robustness of the design. The next step is to finalize the circuit by using differential outputs for the Gain1 and Gain10, by integrating a filter with tunable bandwidth and by adding a calibration test facility using I2C interface.

References

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