

Results from CHIPIX-FE0, a Small-Scale Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for HL-LHC

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Abstract - A prototype of a new-generation readout ASIC targeting High-Luminosity (HL) LHC pixel detector upgrades has been designed and fabricated as part of the Italian INFN CHIPIX65 project using a commercial 65 nm CMOS technology. This demonstrator, hereinafter referred to as CHIPIX-FE0, is composed of a matrix of 64×64 pixels with $50 \mu\text{m} \times 50 \mu\text{m}$ pixel size embedding two different architectures of analog front-ends working in parallel. The final layout of the chip was submitted and accepted for fabrication on July 2016. Chips were received back from the foundry on October 2016 and successfully characterized before irradiation. Several irradiation campaigns with X-rays have been accomplished during 2017 at Padova INFN and CERN EP/ESE facilities under different uniformity and temperature conditions up to 630 Mrad Total Ionizing Dose (TID). These studies confirmed negligible degradation of analog front-ends performance after irradiation. First sample chips have been also bump-bonded to $50 \mu\text{m} \times 50 \mu\text{m}$ and single readout electrode $25 \mu\text{m} \times 100 \mu\text{m}$ 3D sensors provided by Trento FBK. This represented a major milestone for the entire CHIPIX65 project, offering to the pixel community the first example of a complete readout chip in 65 nm CMOS technology coupled to such a kind of silicon detectors. Extensive characterizations with laser and radioactive sources have started. This paper briefly summarizes most important pre- and post-irradiation results, along with preliminary results obtained from chips bump-bonded to 3D sensors. Selected components of the CHIPIX65 demonstrator have been finally integrated into the large-scale RD53A prototype submitted at the end of summer 2017 by the CERN RD53 international collaboration on 65 nm CMOS technology.

1. Introduction

CHIPIX-FE0 is a small-scale ASIC demonstrator fabricated in a commercial 65 nm CMOS technology and addressing all key requirements expected for HL-LHC pixel detectors upgrades. It was designed in the framework of the INFN CHIPIX65 project and in close synergy with the CERN RD53 international collaboration on 65 nm CMOS, providing a fundamental intermediate step towards the implementation of the large-scale RD53A prototype [1].

The chip is composed of an array of 64×64 cells with $50 \mu\text{m} \times 50 \mu\text{m}$ pixel size and integrates two different architectures of analog front-ends working in parallel, one synchronous [2] and one asynchronous [3]. An innovative region-based digital Centralized Buffering Architecture (CBA) grouping 4×4 pixels has been implemented in order to withstand 3 GHz/cm^2 hit rate and extended trigger latencies foreseen at HL-LHC [4].

A more exhaustive description of prototype implementation details can be found in [5]. In the following, a concise summary of latest experimental results is reported.

2. Summary of pre-irradiation and post-irradiation results

The test-setup is composed of a custom PCB hosting the chip under test. A dedicated firmware implemented on a Xilinx evaluation board supports all chip operations. It provides also a robust custom implementation of the Ethernet/UDP protocol for data-acquisition, which is handled by a NI/LabView user interface. Off-line data analyses are then performed using a set of Python/ROOT macros. Extensive pre-irradiation electrical tests validated expected chip functionalities [6].

All global DACs and the monitoring ADC placed at the chip periphery exhibit excellent linearity in agreement with simulations, providing reliable bias conditions and charge-injection characteristic for analog front-ends characterizations.

Analog front-ends performance have been assessed by means of S-curves obtained through charge and threshold scans. On the one hand, the synchronous front-end can reach a minimum threshold as low as $250 e^-$ with an Equivalent Noise Charge (ENC) of about $90 e^-$. The measured threshold dispersion with autozeroing is about $100 e^-$ RMS, in agreement with the simulated latch dynamic offset. Low-noise performance have been therefore demonstrated despite continuous latch and region-logic digital switching activity. Additionally, fast ToT counting up to 320 MHz using the latch as a local oscillator has been validated for $5 ke^-$ injected charge. On the other hand, tests on the asynchronous front-end confirmed an expected minimum threshold of about $500 e^-$ with a noise level of about $80 e^-$. The measured threshold dispersion is about $400 e^-$ RMS before digital trimming in agreement with simulations, reduced to $45 e^-$ RMS after per-pixel tuning.

Several irradiation campaigns have been performed on CHIPIX-FE0 with X-rays under different conditions at Padova INFN and CERN EP/ESE facilities: a first non-uniform irradiation at room temperature up to 230 Mrad, a uniform cold irradiation at -20°C up to 600 Mrad and a uniform irradiation at room temperature up to 630 Mrad. Samples were always biased at nominal operating conditions with continuous monitoring of proper chip configuration and data readout. Irradiated chips demonstrated to be fully-functional up to 600 Mrad TID, whereas after 630 Mrad the ASIC completely recovered its electrical functionality after one-week annealing at room temperature. Post-irradiation threshold and charge scans confirmed for both front-end architectures negligible degradation of low-noise and low-threshold performance.

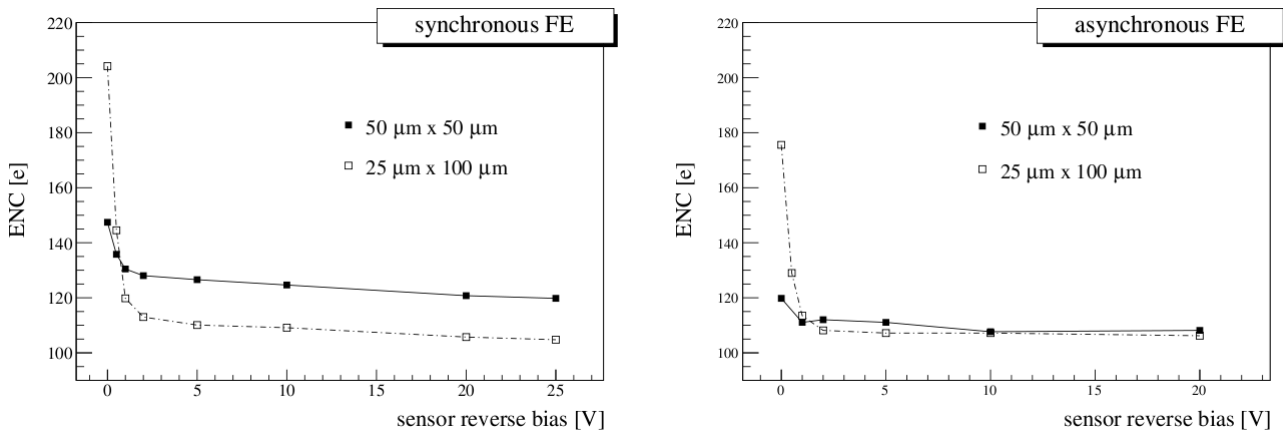


Figure 1: Preliminary results obtained with CHIPIX-FE0 demonstrator bump-bonded to $50 \mu\text{m} \times 50 \mu\text{m}$ and single readout electrode $25 \mu\text{m} \times 100 \mu\text{m}$ 3D sensors designed and fabricated by Trento FBK. Measured ENC as a function of the sensor reverse bias for both synchronous (left) and asynchronous (right) front-end architectures.

3. Preliminary results with 3D sensors

Selected prototypes have been bump-bonded to 3D pixel sensors designed and fabricated by Trento FBK [7]. Bump deposition and flip-chip were performed at SLAC with both $50 \mu\text{m} \times 50 \mu\text{m}$ and single readout electrode $25 \mu\text{m} \times 100 \mu\text{m}$ sensors. Chips have been received back for characterization at the beginning of September 2017. This represented a major milestone for the entire INFN CHIPIX65 project, offering to the pixel community the first example of a complete readout chip in 65 nm CMOS technology coupled to such a kind of silicon detectors.

Proper sensors electrical connectivity with the chips have been validated by measuring the noise increase in analog front-ends connected to sensitive cells, revealing a high-quality bump-bonding despite the small chip size. A preliminary measure of the average ENC as a function of the sensor reverse bias is presented in Figure 1. Very promising and comparable results were obtained for both analog front-end architectures. Extensive characterizations using laser and radioactive sources have started.

4. Conclusions

Latest results from CHIPIX-FE0 have been shortly summarized. This small-scale prototype of a new-generation pixel readout ASIC in 65 nm CMOS represented a fundamental milestone towards the implementation of final chips that will be employed for pixel detector upgrades at HL-LHC.

Encouraging results were collected from all pre- and post-irradiation tests. Irradiation campaigns performed with X-rays at $-20 \text{ }^\circ\text{C}$ demonstrated that chips are fully-functional up to 600 Mrad. Low-noise and low-threshold performance satisfying all design specifications have been validated for both synchronous and asynchronous front-end architectures, certifying negligible degradation of analog key parameters after irradiation.

First samples have been bump-bonded to $50\ \mu\text{m} \times 50\ \mu\text{m}$ and $25\ \mu\text{m} \times 100\ \mu\text{m}$ 3D sensors from FBK and characterizations are ongoing.

Improved versions of both front-end flavors and of the centralized region digital architecture have been included into RD53A prototype, along with additional selected analog blocks such as biasing DACs and bandgap voltage reference.

A new version of the prototype containing further improvements in analog front-ends has been re-submitted as part of the shared RD53A engineering run. Bump-bonding with planar sensors and characterizations of CHIPIX65 components that were embedded into the RD53A prototype are foreseen at the end of 2017.

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References

- [1] N. Demaria et al., *RD53 Collaboration and CHIPIX65 Project for the Development of an Innovative Pixel Front-End Chip for HL-LHC*. Proceeding of the 2014 INFN Workshop on Future Detectors for HL-LHC (IFD). PoS (IFD2014), 010
- [2] E. Monteil et al., *A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC*. Proceeding of the 2016 Topical Workshop on Electronics for Particle Physics (TWEPP). Journal of Instrumentation (JINST), vol. 12 (2017), C03066
- [3] L. Gaioni et al., *65 nm CMOS analog front-end for pixel detectors at the HL-LHC*. Proceeding of the 2015 Topical Workshop on Electronics for Particle Physics (TWEPP). Journal of Instrumentation (JINST), vol. 11 (2016), C02049
- [4] A. Paternò et al., *New Development on Digital Architecture for Efficient Pixel Readout ASIC at Extreme Hit Rate for HEP Detectors at HL-LHC*. Proceeding of the 2016 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC).
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- [5] L. Pacher et al., *A Prototype of a New Generation Readout ASIC in 65 nm CMOS for Pixel Detectors at HL-LHC*. Proceeding of the 2016 International Workshop on Vertex Detectors (VERTEX). PoS (VERTEX2016) 054
- [6] S. Panati et al., *First Measurements of a Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for Extreme Rate HEP Detectors at HL-LHC*. Proceeding of the 2016 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC).
To be published at <http://ieeexplore.ieee.org>
- [7] G. F. Dalla Betta et al., *Development of a new generation of 3D pixel sensors for HL-LHC*. Nuclear Instruments and Methods (NIM) in Physics Research A, vol. 824, pp. 386-387, 2016