PROCEEDINGS OF SCIENCE

Upgrade of the YARR DAQ System for the ATLAS Phase-II Pixel Detector Readout Chip

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Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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PoS(TWEPP-17)076

1. Introduction

The Large Hadron Collider (LHC) research program beyond Run 3 will involve a major upgrade, known as the Phase II upgrade, to produce high luminosity. This high-luminosity LHC (HL-LHC) will be able to deliver 3000 fb^{-1} at $\sqrt{s} = 14$ TeV within 10 years after it begins operations in 2025. This large amount of pp collision data collected at an unprecedented center-of-mass energy will open the doors to explore new physics beyond the standard model as well as measure properties of standard model particles to the highest precision, including the newly discovered Higgs boson.

However, the HL-LHC environment also presents many challenges for the detectors at the LHC. ATLAS [1], one of the two general purpose particle detector experiments at the LHC, is planning on completely replacing their inner tracker with a new all-silicon based inner tracker, ITk [2], to address these challenges. During HL-LHC operation, the average number of pileup interactions will increase from $\gtrsim 50$ (Run 2) to $\gtrsim 200$, and the total ionizing dose experienced by the innermost tracking detector layer will increase from 2.5 MGy (Run 2) to 10 MGy. The ATLAS Level 1 trigger rate is expected to increase to 1 MHz, while the current generation pixel readout chips are designed to handle a 200 kHz Level 1 trigger rate.

New radiation-hard sensors and readout electronics are being developed to withstand the radiation damage, and new sensors will need to have a finer granularity than the current sensors in order to resolve a greatly increased number of vertices from pileup. The current pixel sensors used by the ATLAS inner tracker have dimenstions of 50 μm $\times$ 400 μm for the outer layers and 50 μm $\times$ 250 μm for the inner-most layer, while sensors being considered for the ITk upgrade would have dimensions of 50 μm $\times$ 50 μm for the inner-most layer. In order to cover or expand the fiducial volume of the inner tracker, more of these fine sensors are required, leading to an increase in the number of readout channels from $>$ 90 million channels (Run 2) to $>$ 600 million channels. However, due to the increased density of pixel sensors, the occupancy per pixel is expected to remain the same. With the trigger rate increasing by 5-fold, and the number of readout channels increasing by 6-fold, the total bandwidth of the new pixel system is expected to increase by approximately 30-fold. And with the bandwidth of current readout chips being 160 Mb/s, this means a new readout chip with roughly 5 Gb/s bandwidth will be required for the ITk upgrade. This motivates a completely new redesigned readout chip to handle the dramatic increase in bandwidth and radiation-hardness requirements.

A pixel readout chip known as RD53A [3] which meets these requirements is being developed by the RD53 collaboration. RD53A will be used for R&D leading up to the ITk upgrade. The data acquisition (DAQ) system needed to run scans, calibrations, and to characterize the chip will provide crucial feedback for the final production ITk chip. These proceedings detail many important recent developments and upgrades to this DAQ system.

2. Yet Another Rapid Readout

The Yet Another Rapid Readout (YARR) [4] system provides simple and powerful DAQ for both current generation pixel readout chips, such as FE-I4 [5], and next generation pixel readout chips, such as RD53A. Commands are sent to, and data is read from, the pixel readout chips via a

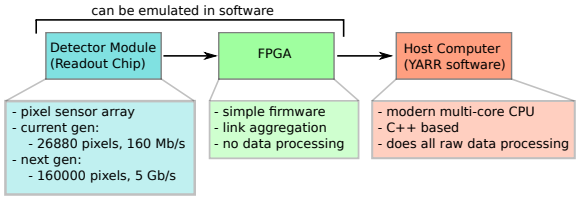

Figure 1: A block diagram showing the basic architecture of YARR. Pixel readout chips are interfaced with a host computer via a PCI-e FPGA board.

PCI-e FPGA board installed in a host computer. The FPGA firmware is simple, only implementing a basic buffer for commands and data, and all of the scan loops and analysis are implemented in software on the host computer. Only using the FPGA as a buffer and not perfoming any processing is enabled by the high PCI-e bandwidth. This would not be possible in systems utilizing other commonly used communication links. The software is optimized for multi-threaded processing, allowing scan loops and analyses of scan results to occur in parallel. The basic structure of YARR is outlined in Figure 1.

A scan procedure consists of a nested loop of the following actions: configuring the registers of the readout chip, looping over the pixel matrix (typically in mask stages since it is not possible to read data out from all pixels simultaneously), and injecting charges and sending triggers. It is then possible to adjust values of registers depending on the response of the pixels, and further scans can be performed with the new values. This allows, for example, the tuning of per-pixel threshold values, such as is shown in Figure 2.

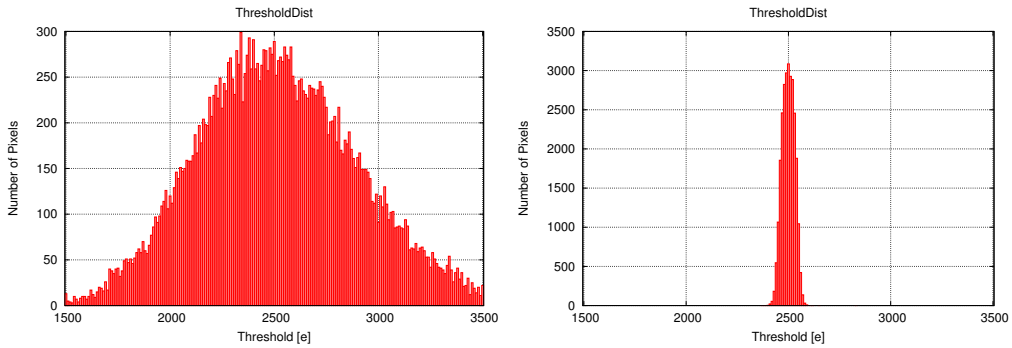

Figure 2: A threshold scan of an FE-I4 chip before applying a per-pixel threshold tune (left) and after (right).

3. YARR Hardware Upgrade

In order to ease the distribution and use of the FPGA board to various labs developing for the ITk upgrade, a critical criteria for the board is that it be commercially available. As such, the PCI-e FPGA board utilized by YARR has recently been upgraded from a SPEC [1] to an XpressK7 [2].

The SPEC board utilized a Spartan 6 FPGA whose transceiver had a maximum bandwidth of 3.125 Gb/s, while the XpressK7 utilizes a Kintex7 FPGA with 4 links, each of which have a

[1] Open source designed, manufactured by multiple companies, https://www.ohwr.org/projects/spec/wiki/wiki
[2] Manufactured by ReFLEX CES.

bandwidth of 12 Gb/s. Also, the SPEC board used a local PCI-e bus bridge chip (GN4124) which only supported PCIe v1.1, which has a maximum bandwidth of 6 Gb/s, while the XpressK7 uses PCI-e v2.1, which has a maximum bandwidth of 20 Gb/s.

It was critical to upgrade the YARR FPGA board in order to increase the bandwidth of the DAQ system, because the new RD53A readout chip can achieve a bandwidth of 5 Gb/s, well over the maximum bandwidth of the SPEC board. The XpressK7 also implements the PCI-e endpoint in the FPGA, while the SPEC board utilized a PCI-e bus bridge. This enables the firmware to be compatible with a wider range of PCI-e FPGA boards, at the cost of handling the PCI-e in firmware.

The design of the XpressK7 firmware is presented in Figure 3. The TxCore is responsible for sending commands to the readout chips, and does not rely on DMA, achieving a slow bandwidth of $\sim$ 160 Mb/s. The more bandwidth-critical operation of receiving data from the readout chips is handled by the RxCore, which relies on DMA and buffering data in DDR3 memory.

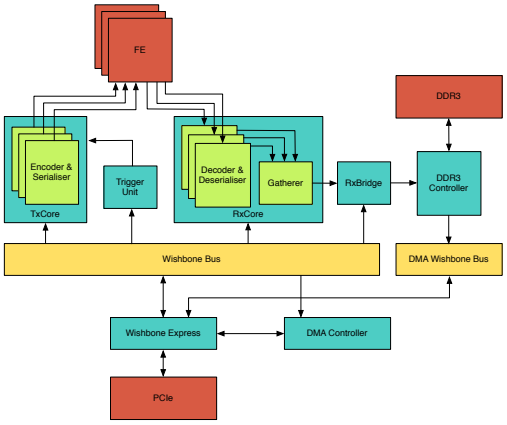

Figure 3: A block diagram showing the firmware architectured used by the XpressK7 FPGA board.

Benchmark measurements were made on the maximum transfer rate with the XpressK7 and the previous FPGA board. A summary of these measurements is presented in Figure 4. The boards are currently operating at $\sim$ 50% of their achievable PCI-e performance due to known inefficiencies in the scatter-gather DMA procedure. There are plans to optimize this in the future, however the XpressK7 board is already able to achieve the desired transfer rate to interface with RD53A chips.

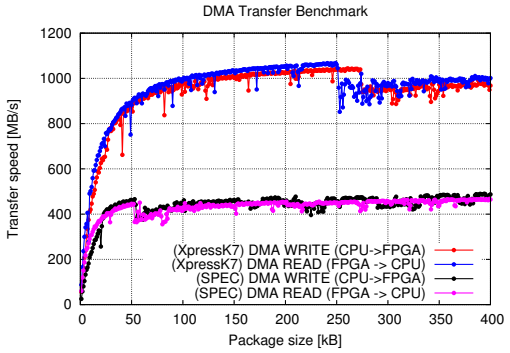

Figure 4: DMA transfer rate benchmark test results.

4. YARR Software Upgrade

The software side of YARR has also been recently upgraded to improve performance, expand features, and improve code quality and maintainability. The software separates running scans, processing data returned from scans, putting the data into histograms, and analyzing the resulting histograms. This allows the software to take advantage of multi-threaded parallel processing, greatly improving the performance of the system. For the current generation FE-I4 chip, the bottleneck in the YARR DAQ system is the FE-I4 communication bandwidth, not the processing done in software. Since all analysis and processing is done in software, this is a great achievement demonstrating the robustness of the YARR DAQ system.

In addition to multi-threaded optimization of the YARR software, critical features have been added. One new feature is the ability to interface YARR with software emulators of readout chips, including FE-I4 and RD53A. This allows for simplified software development, as no hardware is needed outside of the host computer. It also allows for unit tests and continuous integration to be implemented for YARR, where a GitLab Runner [6] can run and analyze scans using the software emulators. This helps to ensure code quality and maintainability.

5. Conclusion

YARR is a robust data acquisition system for current and next generation pixel readout chips. It continues to be improved and upgraded, both in terms of hardware and in terms of software, to enable tests of next generation chips, such as RD53A. The YARR system has been upgraded to handle the bandwidth needs of the RD53A chip and an RD53A software emulator is enabling the preparation of YARR to interface with the chip before it is produced.

References

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