

Low voltage powering of on-detector electronics for HL-LHC experiments upgrades

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All LHC experiments will be upgraded during the next LHC long shutdowns (LS2 and LS3). The increase in resolution and luminosity and the use of more advanced CMOS technology nodes typically implies higher current consumption of the on-detector electronics. In this context, and in view of limiting the cable voltage drop, point-of-load DC-DC converters will be used on detector. This will have a direct impact on the existing powering scheme, implying new AC-DC and/or DC-DC stages as well as changes in the power cabling infrastructure. This paper presents the first results obtained while evaluating different LV powering schemes and distribution layouts for HL-LHC trackers. The precise low voltage power source requirements are being assessed and understood using the CMS tracker upgrade as a use-case.

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1. Introduction

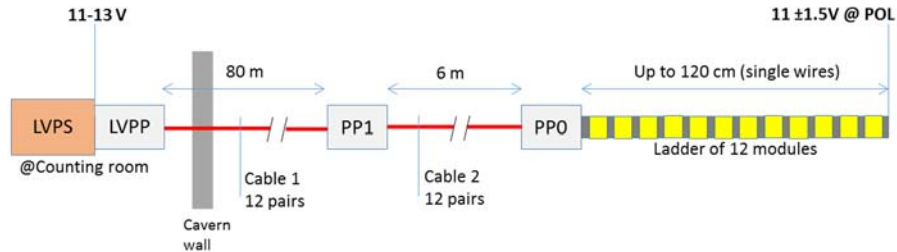
The supply of point of load (POL) DC-DC converters at 12V [1] makes it possible to consider relocating power supplies to the service caverns, and thus avoid the costly development and constrained maintenance conditions of radiation and magnetic field tolerant converters. The feasibility demonstration of this powering scheme was one of the objectives of this project.

The existing LV powering scheme in the experiments can be summarized as follow:

- Power supplies (PS) in counting house and/or experimental cavern (distributed system in most cases).
- Supply of front-end at extra low voltage (ELV, e.g. 2.5Vdc) as well as low noise and ripple requirements.
- Use of linear regulator on certain detectors.
- If in experimntal cavern, PS equipment in harsh environment (Radiation and B-field) leading to custom PS systems: Complex (water cooling, magnetic shielding, etc.), constrained (e.g. limited remote monitoring), costly.

2. CMS tracker phase II upgrade use-case and test setup

To be as representative as possible of the environmental conditions and constraints present in an HL-LHC detector, the CMS tracker upgrade is considered as a use-case. The upgraded CMS tracker consists of 13'300 modules, grouped in different sub-structures depending on location. The baseline assumption for the LV distribution concept is a ladder structure of 12 modules.



Assumption summary:

- 12 modules / ladder, each module uses one POL DC-DC converter
- 1 LVPS channel / ladder
- Monitoring and control granularity at low voltage patch panel (LVPP): individual modules
- Current consumption: 0.7A / module; 8.4A / ladder
- Targeted voltage @DC-DC: 11V +/- 1.5V
- Maximum tolerated input voltage @DC-DC: 13V
- Worst case cable length: 88 m
- Maximum voltage drop from LVPS to furthest DC-DC: 3V

2.1. Tested equipment and setup

The technical requirement for the power system is divided in three parts, the AC-DC power supply (LVPS), the low voltage distribution patch panel (LVPP) and the cabling. The cabling has been treated specifically as part of the CMS tracker use-case. A test PCB receiving up to 12 FEASTMP DC-DC converters was built and a set of electronic loads emulates the front-end chip power dissipation. The measurement equipment consists of an oscilloscope with current probes.

Selected and tested power supplies:

- Adapted Caen A1513 (with LDR)
- Modified Wiener MPOD 0MPV8016 (with CLC)
- UniPower PFE3000-12 (commercial bulk power supply)
- Goessen 33K7 lab PS (commercial lab power supply)

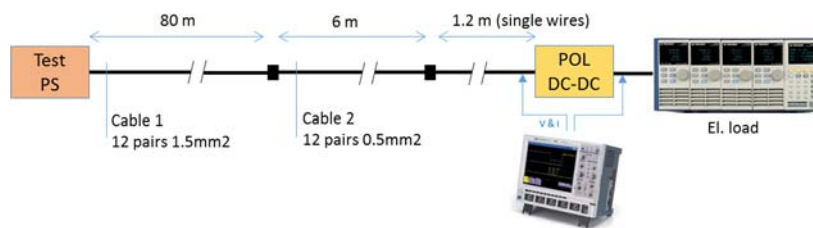
Line drop recovery (LDR) and current based loop control (CLC) are both specific output voltage regulation modes made to compensate the cable Vdrop based on the power supply output current.

The cabling is divided in three sections of 80, 6 and 1.2m. Prototypes were procured from Habia and an IC candidate for the LVPP identified (LM25066: PM bus power management and protection).

3. Measurement and simulation results

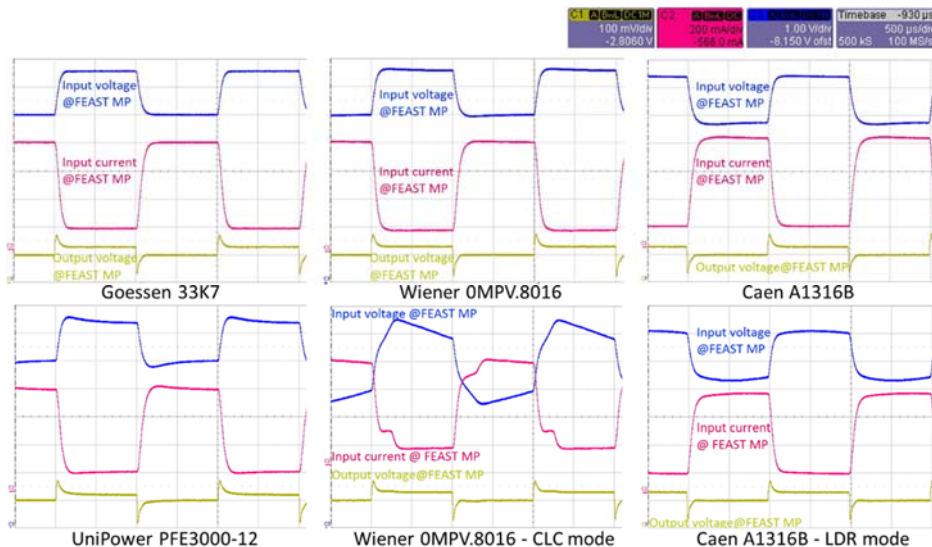
3.1 Various power supplies and long distance cable

The first measurements quantify the impact of different power sources on the POL DC-DC input and output voltages when supplied through long distance cabling (almost 90m).



Test conditions:

- Single DC-DC converter output set to 2.5V, load current swinging from 0.5 to 2.5A
- Load slew rate: 5A/ms

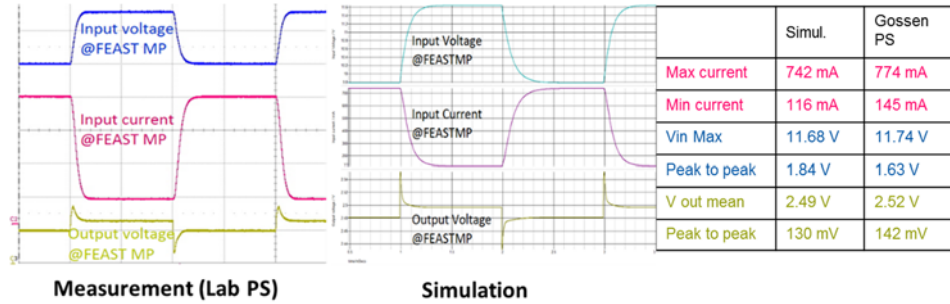


The POL DC-DC regulates its output well ($< 180 \text{ mVpp}$) despite the important input voltage swing (above 3V worst case). With a high slew rate at the load, both output current based regulation modes (CLC and LDR) are not fast enough to compensate fast current variations. The regulation time constant is measured to be 2 and 4ms for Wiener CLC and Caen LDR respectively. In certain powering schemes, compensating the cable drop could nevertheless improve the overall

efficiency especially for long cables. In the use-case considered here this impact would be limited to a few percents over the entire power chain.

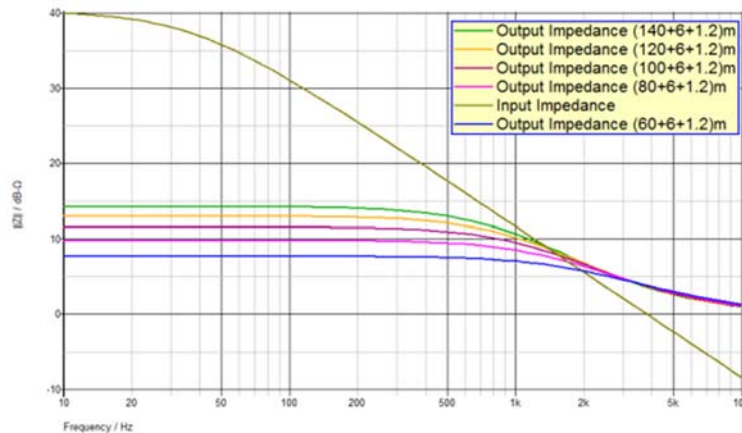
3.2 Simulation results and system impedance

The powering scheme was simulated using the same software used to model the POL DC-DC during its design to benefit from an existing and precise converter model. A representative load, power source and cable model was used in order to compare measured results with simulation.



The simulated and experimental results are matching well once the value of a capacitor of the POL DC-DC input Pi filter was adapted to include its DC voltage derating (from 22 to 11uF).

Once a satisfying match is obtained between the simulation and the experiment, further investigations can be performed based on the model only. The simulation tool offers the possibility to trace Bode plots of the impedances allowing to verify the impedance matching between the LVPS, the full cable length and the POL converter input (Pi input filter).



An input impedance collapse is seen above 1 kHz between the LVPS after the long cables and the converter input. This impedance crossing could potentially lead to resonating oscillations. Measurements show that the POL DC-DC with its input and output filters flatten all current oscillations above this frequency.

3.3 Test results with 12 POL converters

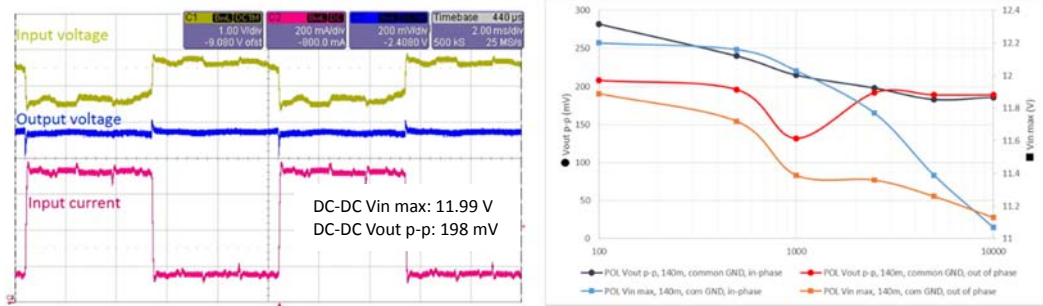
A test pad was assembled to operate a set of 12 POL DC-DC converters in parallel in a way similar to the CMS TK ladder of 12 modules. A set of measurements was preformed using this setup with and without common ground at the POL DC-DCs.

Test conditions:

- UniPower PFE3000-12 (commercial bulk power supply)

- o 12 DC-DC converters; output 2.5V, load swing from 0.5 to 2.5A, slew rate: 5A/ms

The measurement results for 12 DC-DC with common ground over 80+6m of cables with the load channels out of phase, show that the output voltage swing remains acceptable, within 200mV, despite the relatively important input voltage span of up to 1.6V.



With an increased cable length of 140+6m and while varying the load frequency from 100Hz to 10kHz, the results are similar when the load channels are not in phase. However, synchronizing the loads to switch in phase has an important impact with the DC-DC output rising over 280 mV peak-to-peak for a load switching at 100Hz. Similarly, with 80+6m of cable length, the peak-to-peak output voltage goes above 260mV.

4. Conclusion

The results contribute in building confidence that placing the low voltage power sources in a service cavern can be envisaged, thanks to the well operating POL DC-DC converter and to the low inductive cable prototypes procured for this project. The test of a selection of power supplies shows that the use of specific regulation modes is not necessarily needed and can in certain circumstances even worsen the voltage stability at the converter input. The results also show that some PS parameters (output ripple and regulation precision) can be relaxed compared to present PS equipment specifications. The measurements with 12 converters in parallel with common ground show that the scheme envisaged for the CMS TK upgrade is operating with certain limitations (cable length) unless appropriate compensations (filtering important load current slew rate) are applied.

Based on the results and for the use-case considered, a few key conclusions can be listed:

- o Standard regulated PS are perfectly suitable.
- o The cable inductance should ideally remain below 1uH/m.
- o Depending on the maximum tolerable DC-DC output ripple, for long cable lengths (above 80m) and/or inductance (typically above 1uH/m), load current slew rate should be limited (e.g. by additional point of load filters).

References

[1] *Point of load DC-DC converter FEASTMP module.*
<http://project-dcdc.web.cern.ch/project-dcdc/public/DCDCmodulesDatasheets.html>