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A study of SEU-tolerant latches for the RD53A chip

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The RD53 collaboration was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC and requiring extreme rate and radiation tolerance. The 65 nm CMOS process has been adopted in order to satisfy the high level of integration requirement. However, the SEU immunity should be carefully considered for a deep submicron process like the 65 nm. Indeed, the device dimensions are small and the capacitance of the storage nodes becomes very low. A chip prototype including different SEU tolerant structures was designed in a 65 nm technology. Several proton irradiation tests were carried out in order to estimate the SEU tolerance of the proposed structures and the level of improvement comparing with a standard architecture.

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1. Introduction

The 65 nm CMOS process is a promising technology for the pixel readout chips at HL-LHC (High Luminosity-LHC) in terms of high integration density and a first 65 nm demonstrator chip, RD53A [1], containing 76800 pixels of 50×50 µm² was submitted end of August 2017.
Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about 2.10^{16} n/cm² (1 MeV neutron equivalent) corresponding to a Total Ionizing Dose (TID) of 1 Grad over ten years of exploitation. Irradiation studies [2] were done in order to estimate the TID tolerance of the 65 nm process. The main requirements from these studies were respected in our design, by increasing the size of the devices, in order to ensure a good functionality in these aggressive operating conditions.
The main characteristics of the RD53 [3] front-end chip relevant to the SEU aspect are summarized in the following table (Table 1).

Table 1: RD53 specifications

Specification	value	comments
Number of pixels	160 k	-
Pixel size	2500 µm²	-
Number of pixel configuration bits	160k×8 = 1.28 10^6	-
Global memory size	8 kbits	-
Peak fluence	$0.5.10^9$ p/cm²/s	layer 0 radius: 3.7 cm from the interaction point
TID	500 Mrad	for 5 years

This paper shows some Hardened By Design (HBD) approaches to be followed in order to reduce the effect of the single bit upsets.
Three different structures have been designed and implemented in a 65 nm chip prototype. The memory structures studied are:

- ✓ Hamming coded version.
- ✓ Triple Redundancy Latches (TRL) cell.
- ✓ Dual Interlocked CEll (DICE).

Furthermore, the submitted prototype was used to measure the influence of a Deep N-Well (DNW), in terms of SEU tolerance. In fact, the digital blocks of the RD53A chip were implemented on the DNW layer in order to shield the sensitive analog design from the digital noise. The DNW layer could potentially decrease the SEU tolerance [4].
Irradiation tests were carried out at CERN. For all SEU tests, we usually use a 24 GeV proton beam line in the "IRRAD" proton facility at the east zone of the Proton Synchrotron (PS).
The prototype chip designed to study SEU effects is described in order to explain our experimental approach. Then, each architecture implemented in the prototype chip is summarized, and finally the main results obtained for the three studied structures are presented and compared.

2. The SEU prototype chip

A prototype chip (~2×2 mm²) (Figure 1a) was designed in a 65 nm technology to study SEU effects. The chip includes different architectures of memory separated in several columns (Figure 1c). The dedicated area for the SEU block is approximatively 0.7×1 mm² including the pad ring (Figure 1b).

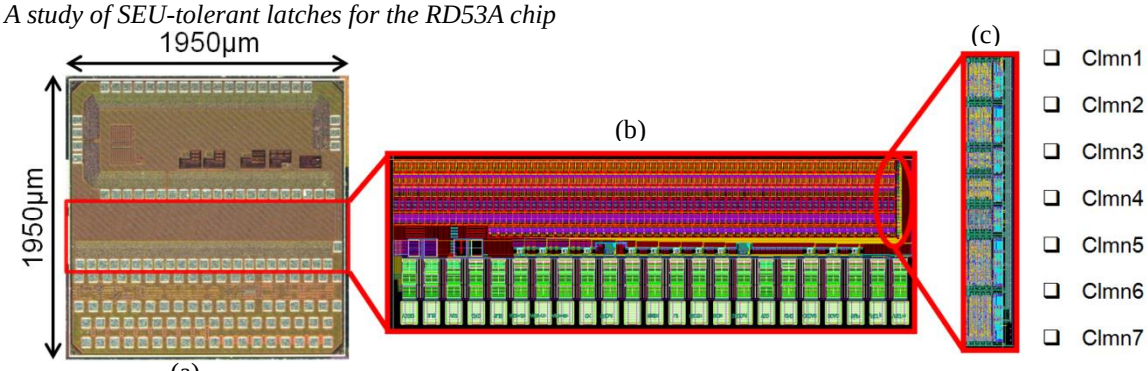


Figure 1: SEU chip layout. (a) SEU prototype chip,(b) SEU prototype chip, (c) seven independent SEU memories columns

The SEU chip is divided into seven independent columns of 640 cells. It requires five input bits ("LOAD", "CLOCK", "READBACK", "CLEAR", "DIN") plus three bits ("ClAdd<2:0>") dedicated to the column selection. One output bit ("DOUT") is common to the entire chip and corresponds to the output of a shift register from the selected column.
This system allows us to calculate the number of errors for each column by comparing the injected input pattern against the output pattern. As this operation is performed in synchronization with the proton beam, the reading of the output pattern contains the state change of each memory considered here as an error. The comparison of the different latches consists of an error monitoring in the read back pattern between the standard latches (from the digital library) implemented inside the shift register, and the full-custom latches implemented in each column of the chip.

3. Latch design variant

3.1 Hamming-coded version

This version is based on a dynamic error correction. The implemented logic generates some parity bits depending on the binary value of the stored data. Typically, four parity bits are needed to detect a change in eight data bits. In total, twelve bits are required for eight configuration bits (Figure 2).

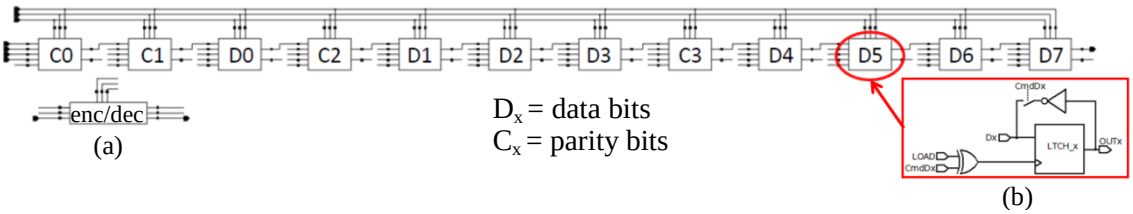


Figure 2: Hamming-coded version schematic. (a) encoder/decoder logic cell, (b) one memory cell

The main advantage of this architecture concerns the schematic of one bit cell (Figure 2b), which is very simple. It needs only one standard latch plus one switch and an inverter. The drawbacks are related to the case of a double error occurrence, which cannot be corrected, and to the dedicated area of the encoder/decoder logic (Figure 2a), which can reach up to 65% of the whole cell area.

3.2 DICE version

The DICE latch (Figure 3) is based on the redundancy of the storage node [5]. The main drawback of this structure is its potential sensitivity to charge sharing. If two sensitive nodes of the cell storing the same logic state are struck simultaneously by an ionizing particle, the DICE latch would be definitely corrupted. To minimize this effect, these sensitive nodes can be isolated and separated spatially by using an interleaved layout technique.

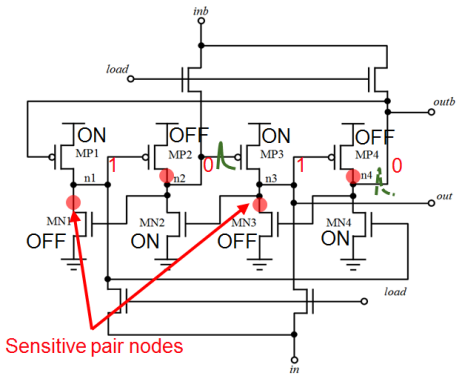


Figure 3: DICE latch schematic (example of a stored data = 1)

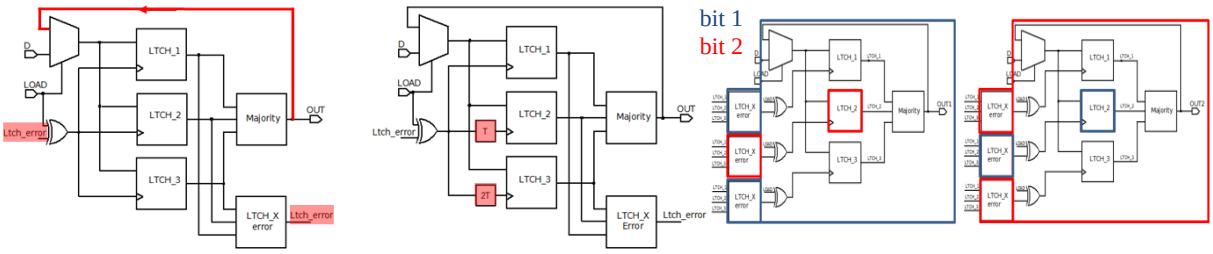
This architecture remains interesting because of the very small area penalty, representing less than 3% in a pixel of 2500 µm² for eight configuration bits.

Five variants have been designed:

1: DICE with a minimal size
2: DICE with guard ring
3: DICE with an interleaved layout (distance between two pairs of nodes ~14 µm)
4: DICE with an increased size of transistors (transistor length = 400 nm)
5: Version 4 with an interleaved layout (distance between two pairs of nodes ~14 µm)

3.3 TRL version

The Triple Redundant Latch (TRL) version includes an error self-correction with a feedback driven by the latch error detection (Figure 4a). Particular attention has been paid to the combinatorial logic controlling each single latch of the TRL and the global nodes were triplicated in order to prevent the transient errors occurring in the control logic to be propagated to the latches (Figure 4b, 4c). However, it consumes a rather large area and cannot be implemented inside the pixel. Nevertheless, it can be used in the chip periphery where it should increase the SEU-hardness quite drastically. Three variants of this cell have been implemented in our SEU prototype chip.



(a) (b) (c)

Figure 4: TRL versions. (a) standard version, (b) with a delay (5 ns ±1 ns),(c) TRL with a triplication of a global node and an interleaved layout (distance between 2 pairs node ~17µm) for two bits

4. SEU Results and conclusions

The SEU tests were carried out at CERN, using the "IRRAD" beam line of the Proton Synchrotron (PS) facility. It provides a 24 GeV proton beam. The beam contains 3-5 spills per cycle with a duration of around 400 ms. The fluence can be tuned typically from 5.10^{10} to $1.5.10^{11}$ protons/spill. The comparative table presented below (Table 2a), shows a direct comparison with a standard latch implemented in the D Flip-Flop (DFF) from the library of the technology. The mentioned values are the error rates measured per spill and the associated gain we obtain with the use of each architecture.

Table 2: Tests results. (a) SEU measurements for each architecture, (b) Mean time between errors for the pixel chip

Cell	Error rate/spill 0 → 1	1 → 0	all	Gain
Standard latch W_{pmin} = 300nm	2.58	2.29	2.43	-
TRL	20E-3	1.8E-3	11E-3	×220
TRL + 3×LOAD	4E-3	1.9E-4	2.1E-3	×1160
TRL + 3×LOAD interleaved	1.2E-3	4.6E-5	6.2E-4	×3920
DICE	0.46	0.63	0.54	×4.5
DICE + guard ring	0.36	0.51	0.43	×5.6
DICE interleaved	0.26	0.29	0.27	×9
DICE (L=400nm)	0.12	0.18	0.15	×16
DICE (L=400nm) interleaved	0.07	0.12	0.095	×26
Hamming code 8d+4c	0.467	0.185	0.326	×13

(a)

	Mean time between 2 errors Pixel config.	Global config.
Memory size	1.28 Mbits/chip	1 kbits/chip
Standard latch	55 ms	71 s
TRL	209 s	74 hours
DICE	0.5 s	639 s
DICE (L=400nm) interleaved	1.7 s	36 mn
Hamming code 8d+4c	0.7 s	923 s

(b)

During the SEU campaign, enough statistics were reached to estimate the cross-section of the different latches. Based on the DFF cells error numbers, the equivalent cross-section of the standard latch is estimated to 2.8 10^{-14} cm²/bit.

The TRL cell with an interleaved triplication of the global node is clearly efficient with a measured gain of ~4000 in comparison with the SEU error probability of the standard DFF. Following this result, this cell has been implemented in the periphery of the RD53A chip for the global configuration register.

The DICE latch is less immune than the TRL but it is still an interesting structure because it leads to a good compromise between the area it requires and the SEU-hardening it brings. We have shown from measurements that optimization of the transistors size is a good way to increase the tolerance to SEU of these cells.

The Hamming-coded version presents only an improvement factor of about thirteen over the DFF. To improve the SEU tolerance of this architecture, two main points should be investigated:

1: The robustness of the parity bits management.

2: The optimization of the glue logic/latches area ratio.

Finally, a calculation of the mean time between two errors is presented (Table 2b) taking into account the future environment of the RD53 chip. This table shows a significant improvement by comparing the performance of the DICE latches and standard latches. The mean time between two errors reaches 1.7 second for a DICE latch version, if an interleaved layout with optimised size transistors is chosen. This is thought to correspond to a manageable in-pixel error rate for the environment in which the IC will be used.

The TRL version with a triplication of a global node is interesting for a peripheral global registers where the mean time between two errors could be evaluated to be 74 hours. Despite the importance of the global configuration bits, it is thought that the error rate would allow for safe operation in the HL-LHC environment.

Finally, the possible effect of the Deep-N Well layer was investigated. Complementary measurements done concerning this point show that the SEU immunity is not degraded when the configuration latches are implemented on this layer.

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