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ATLAS EXPERIMENT

Design and testing of the high speed signal densely populated ATLAS calorimeter trigger board dedicated to jet identification

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  - Power and thermal simulation
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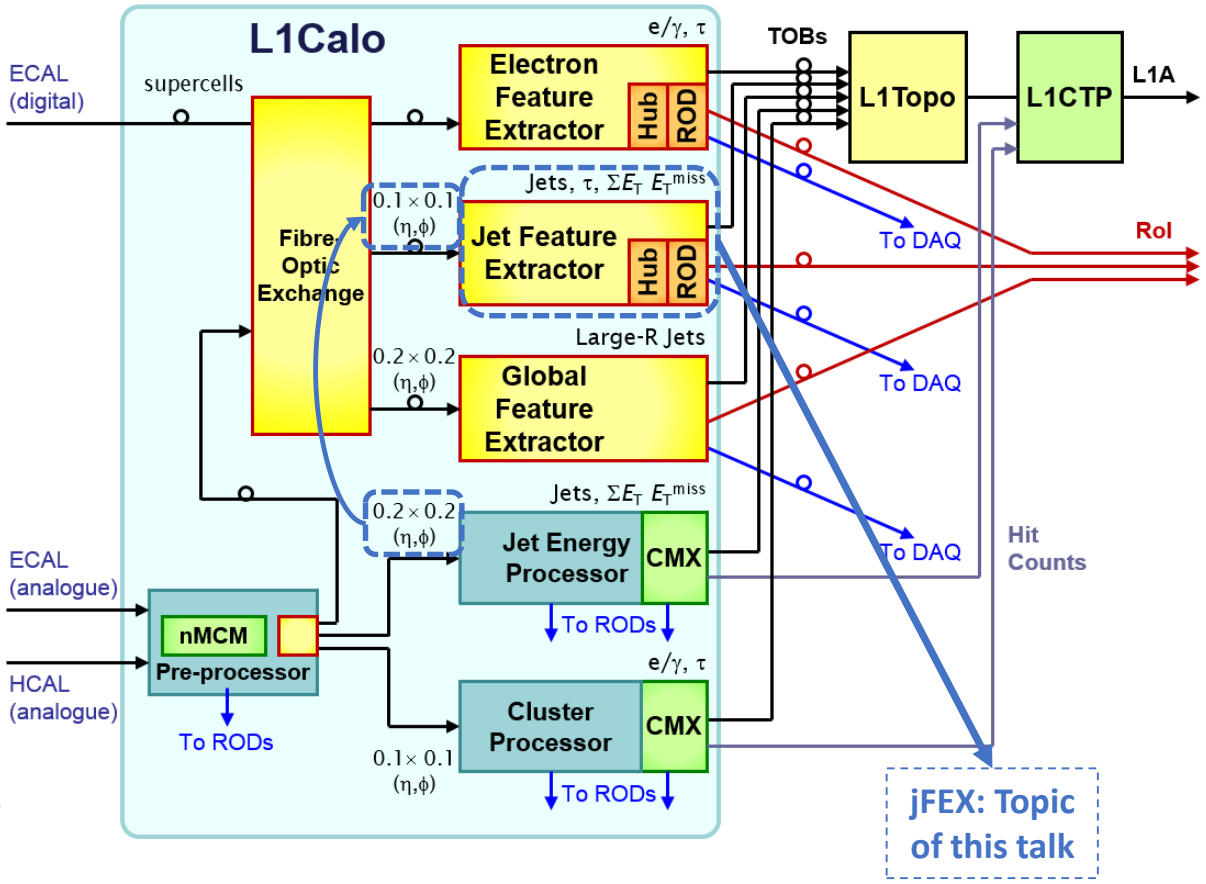
Introduction

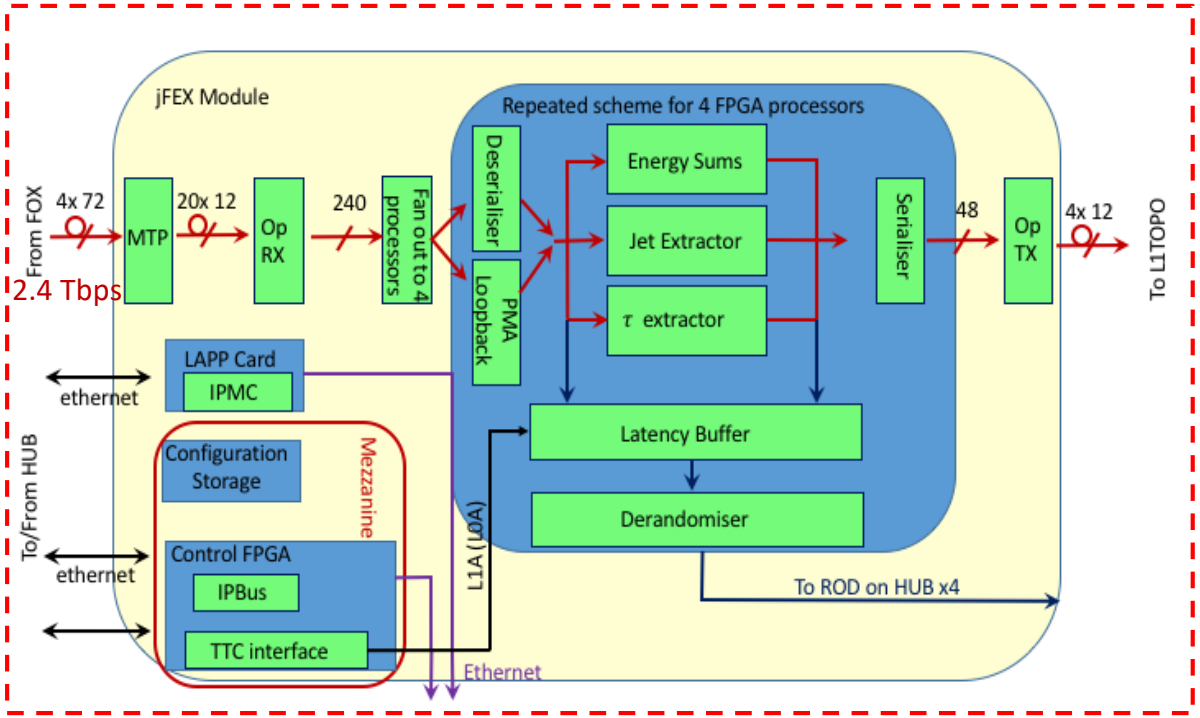
- New operational conditions on the Large Hadron Collider (LHC) after the Long Shutdown (LS2)
  - Increased luminosity: ~$2.5 \cdot 10^{34}$ $cm^{-2}s^{-1}$
- ATLAS TDAQ Phase-I Upgrade
  - Upgrade of the ATLAS first level calorimeter trigger (L1Calo)
    - Trigger rate will remain at up to 100 kHz
      - Level-1 trigger latency envelope of 2.5 µs
  - Forward compatibility with Phase-II upgrade (after 2026)
    - L0 trigger rate up to 4 MHz
  - Increased granularity for jet finding
    - Gaussian filtering algorithms instead of pure sliding window



jFEX requirements

- For each bunch crossing, the jFEX should identify:
  - jet candidates
  - ΣE_T and E_T^{miss}
  - large-area tau
- Digitized input from central and forward calorimeters
- **High input bandwidth (2.4 Tbps) and large processing power**
- **7 modules required**

Jet Feature Extractor (jFEX) block diagram



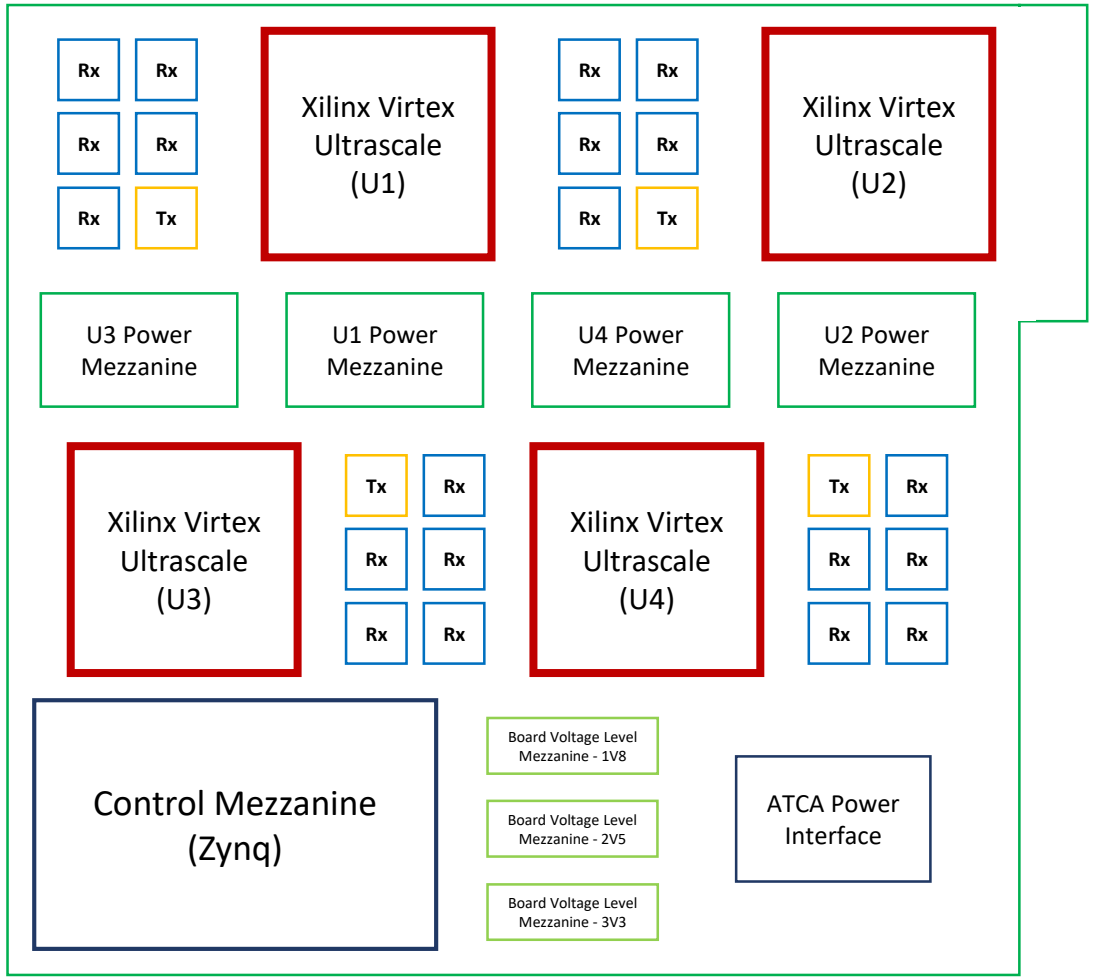
jFEX design challenges

- **High input bandwidth and large processing power**

1. Signal integrity
    1. High density PCB
    2. Tight routing space (possible cross-talk)
        - 198 high speed links
        - 396 parallel IOs
2. FPGA power consumption
    - VCCINT (0.95 V) -> up to 4x60 A
    - MGTAVCC (1.0 V) -> up to 4x18 A
    - MGTAVTT (1.2 V) -> up to 4x16 A
3. Maintain large processing resources to keep the possibility for future improvements
4. Cooling

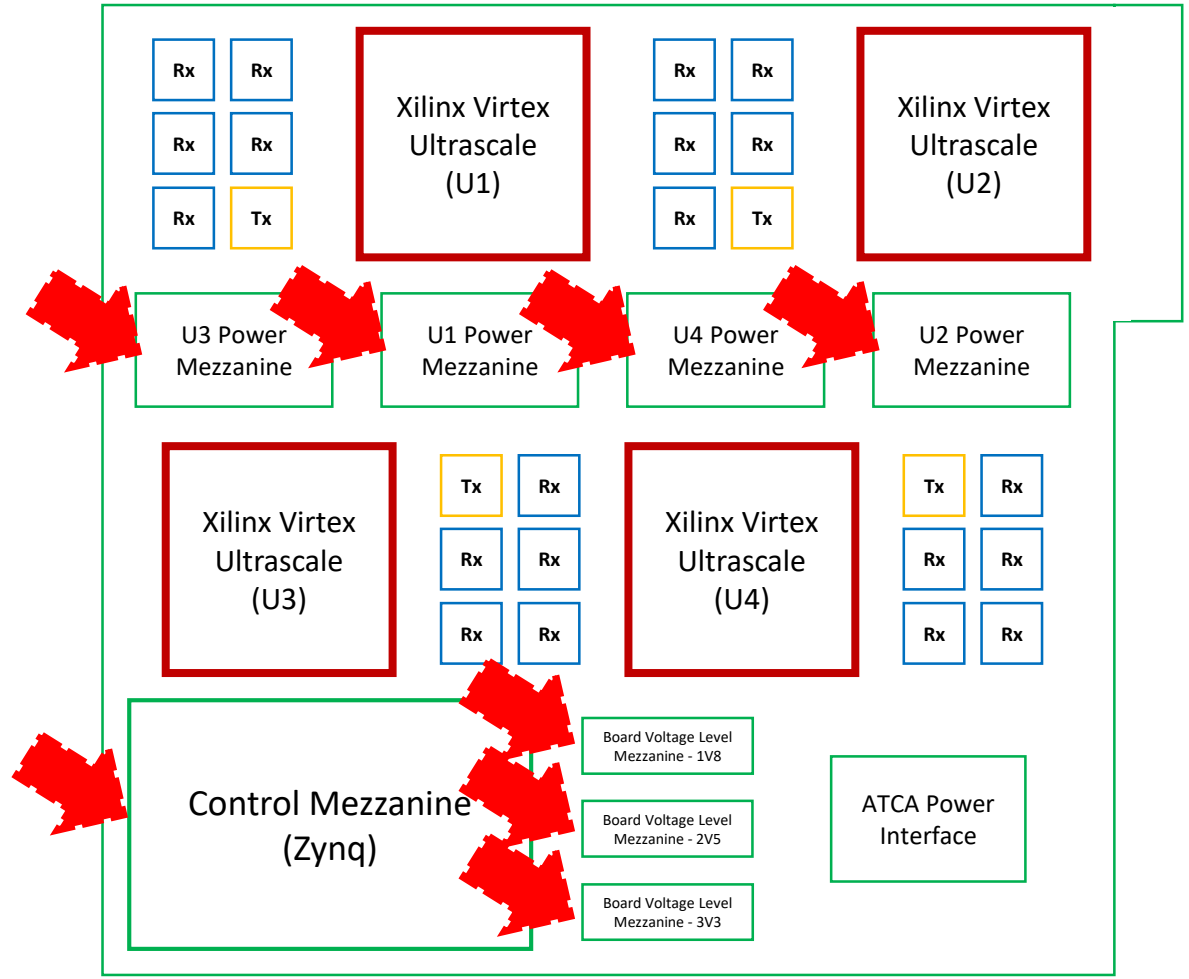
Hardware overview

- ATCA board
- 4 Xilinx Ultrascale FPGAs (XCVU190FLGA2577) per module
  - Up to 120 MGTs x 4 per module-> up to 2.4 Tbps in input bandwidth
  - 2 types of MGTs: GTH and GTY
- 24 MiniPOD: 20 RX + 4 TX
- Board control (**mezzanine**):
  - Carrier board for the PicoZed (Zynq)
- Two power **mezzanines**
  - Board level voltages and FPGAs



Layout concept

- Control and power mezzanines
  - Flexibility for new functionalities and future requirements



Layout concept

- Control and power mezzanines
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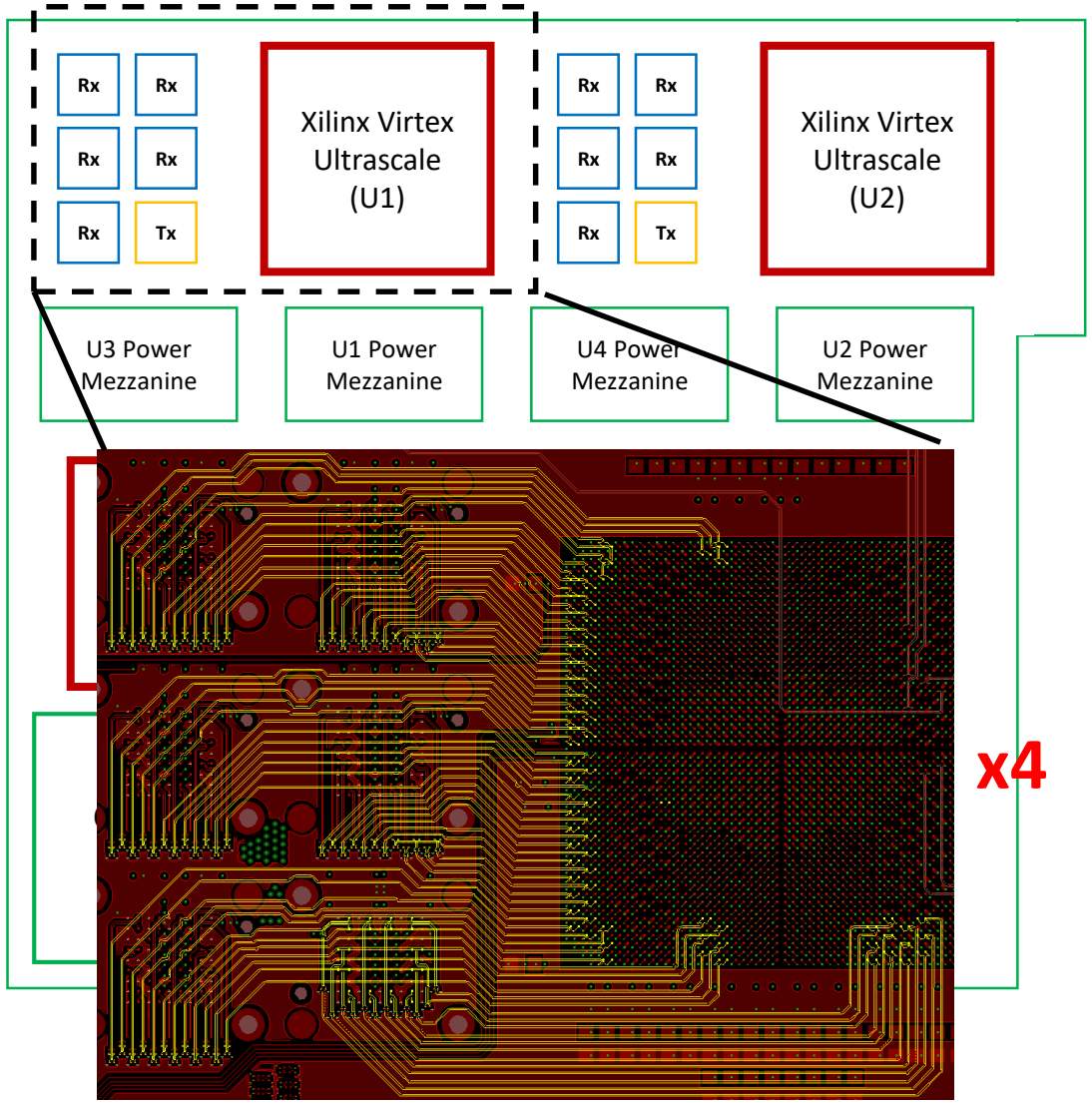
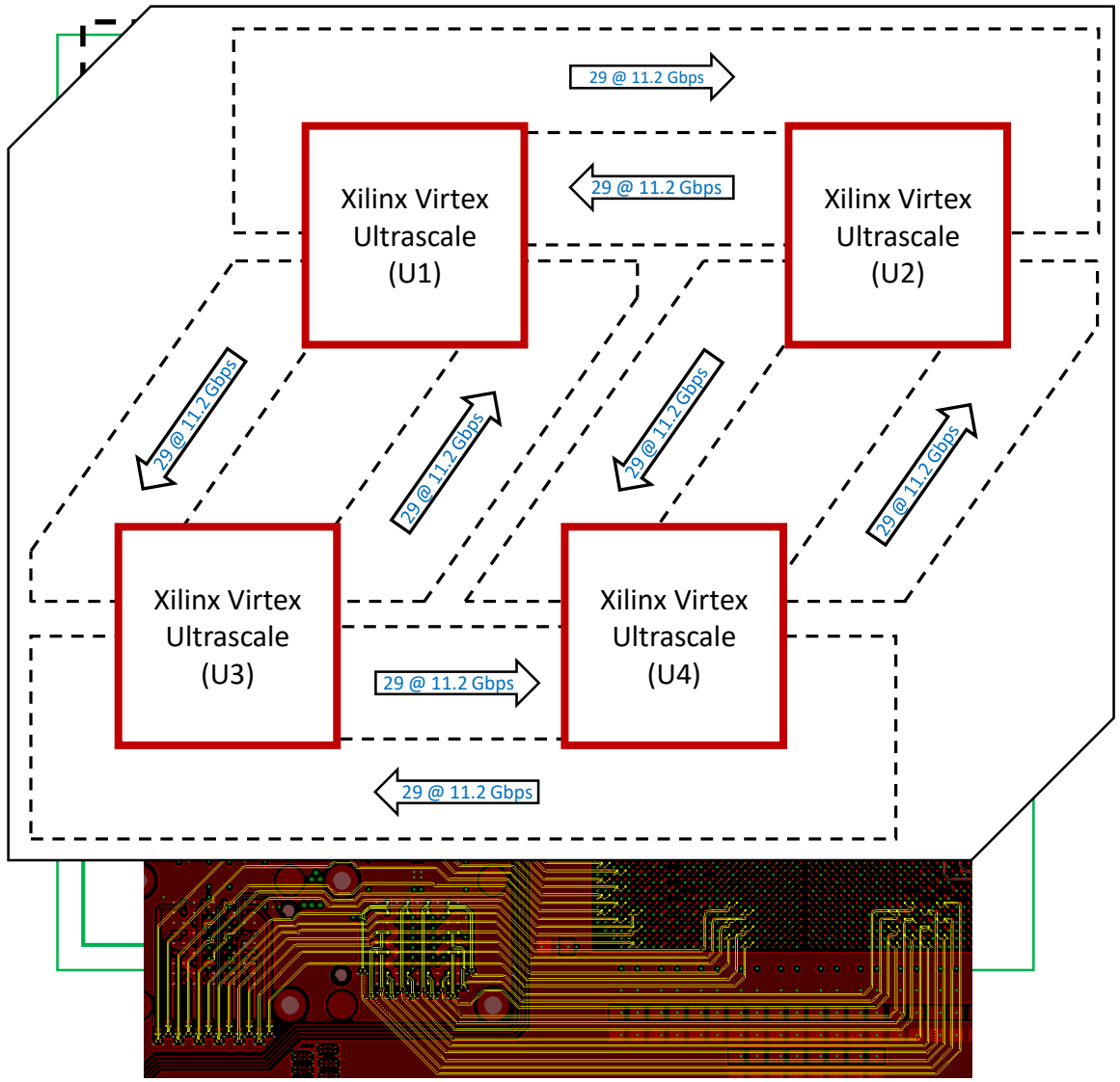
- **Modular** design
  - Same routing for each FPGA/miniPOD block
  - For high speed links and parallel IO



Layout concept

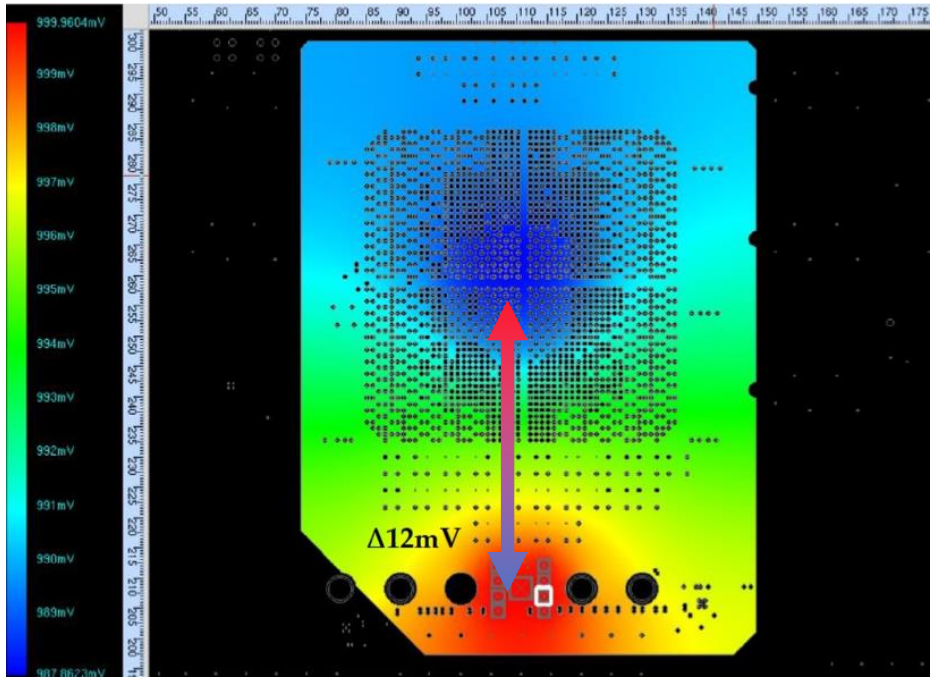
- Control and power mezzanines
  - Flexibility for new functionalities and future requirements
- **Modular** design
  - Same routing for each FPGA/miniPOD block
  - For high speed links and parallel IO
- No crossing busses to minimise possible cross-talk



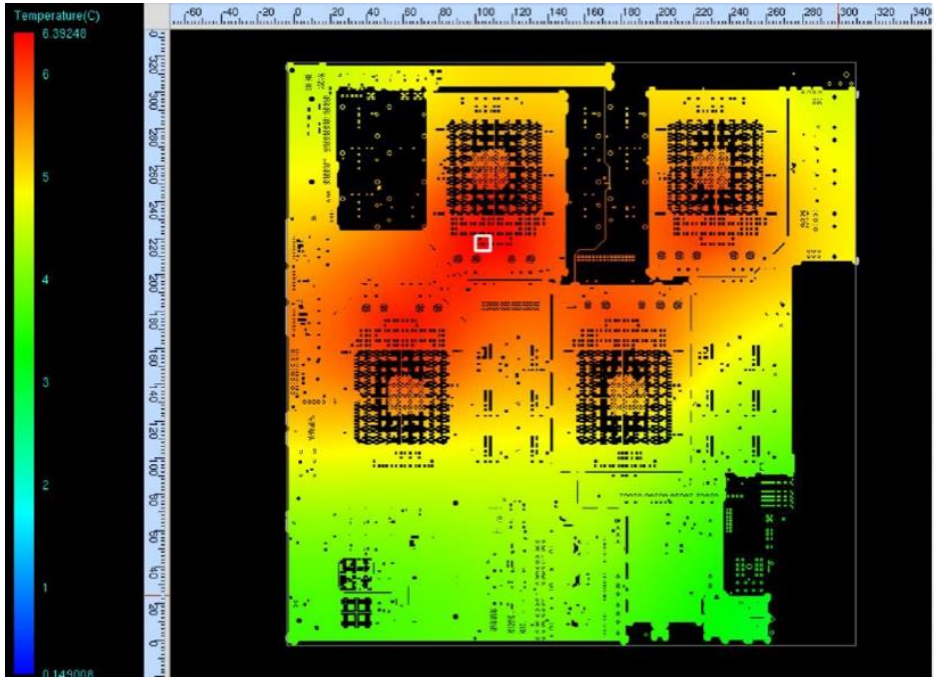
jFEX power/thermal simulation

- VCCINT - 0.95V/60 A
- Design optimized after several interactions in order to cope with Ultrascale voltage drop specification (20 mV)

Voltage drop: Max. ΔV~12 mV

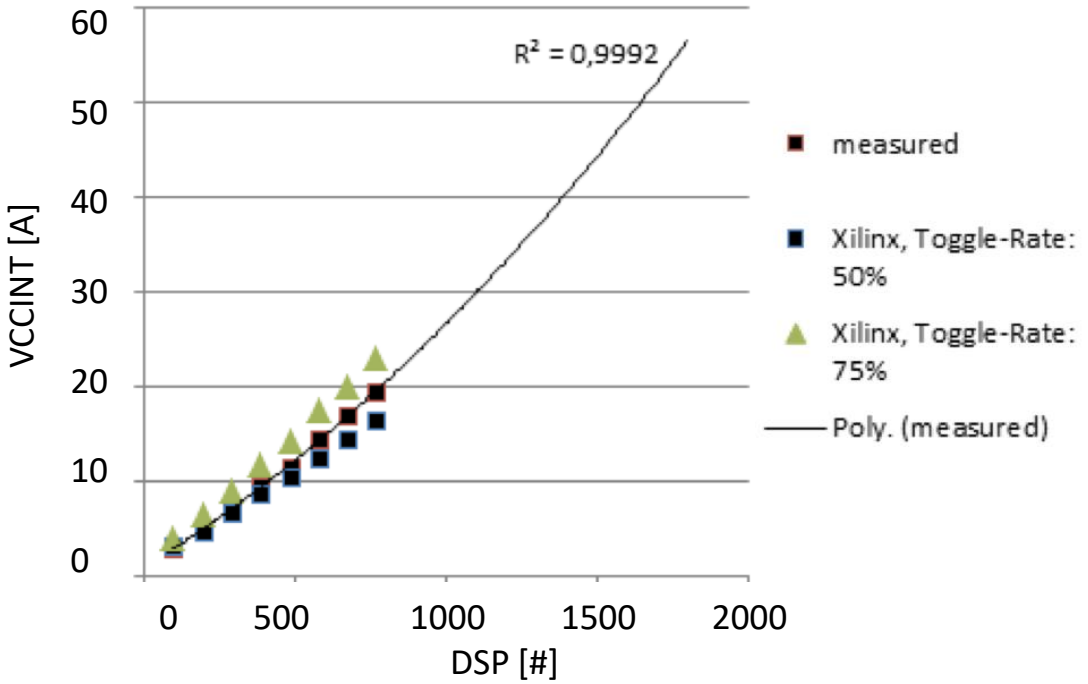


Thermal simulation: Max ΔT~6.4^{o} C



FPGA power consumption estimation test

- Algorithm might be modified and further optimised in the future
  - Prototype design is based on the Xilinx Power Estimator (XPE)
  - Validation with measurements on Xilinx Evaluation Board
- Measurement of the FPGA power consumption as function of the FPGA resource's usage (DSP)
  - DSP estimate usage for the final algorithm version ~60% (1200 DSP)
  - Expected maximum current is around 35 A

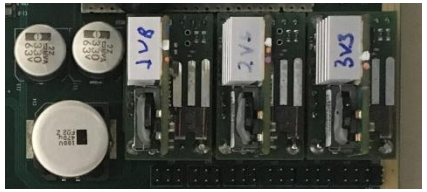


Power modules

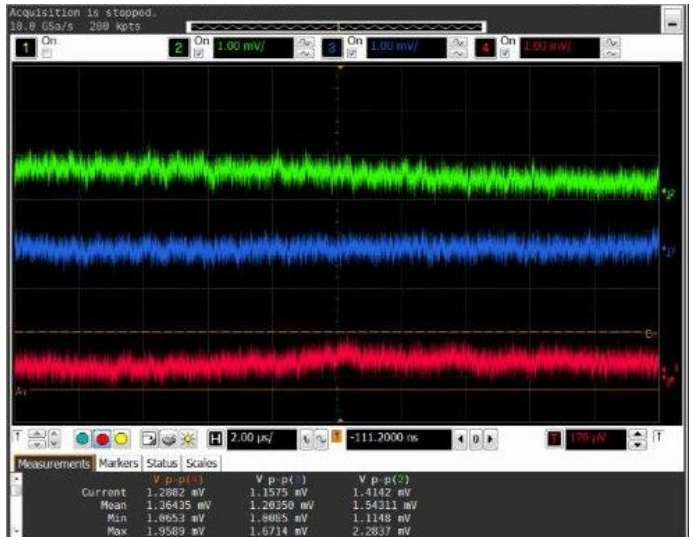
- FPGA and board level power mezzanines
  - Gain in flexibility during prototype tests
  - Critical ripple requirement for MGTAVCC and MGTAVTT
    - Vout ripple (peak-to-peak) < 10 mV
- Current solution
  - SIL20C (Artesyn)
    - Successfully tested
      - Special PCB designed for testing the mezzanines
    - Vout ripple (peak-to-peak) ≈ 3 mV
- Next step
  - iJX series (TDK-Lambda)
    - To include PMBus functionality and cope with VCCINT current estimations
    - iJA (35 A) and iJB (60 A)

FPGA Power Supply

Board Level Voltages



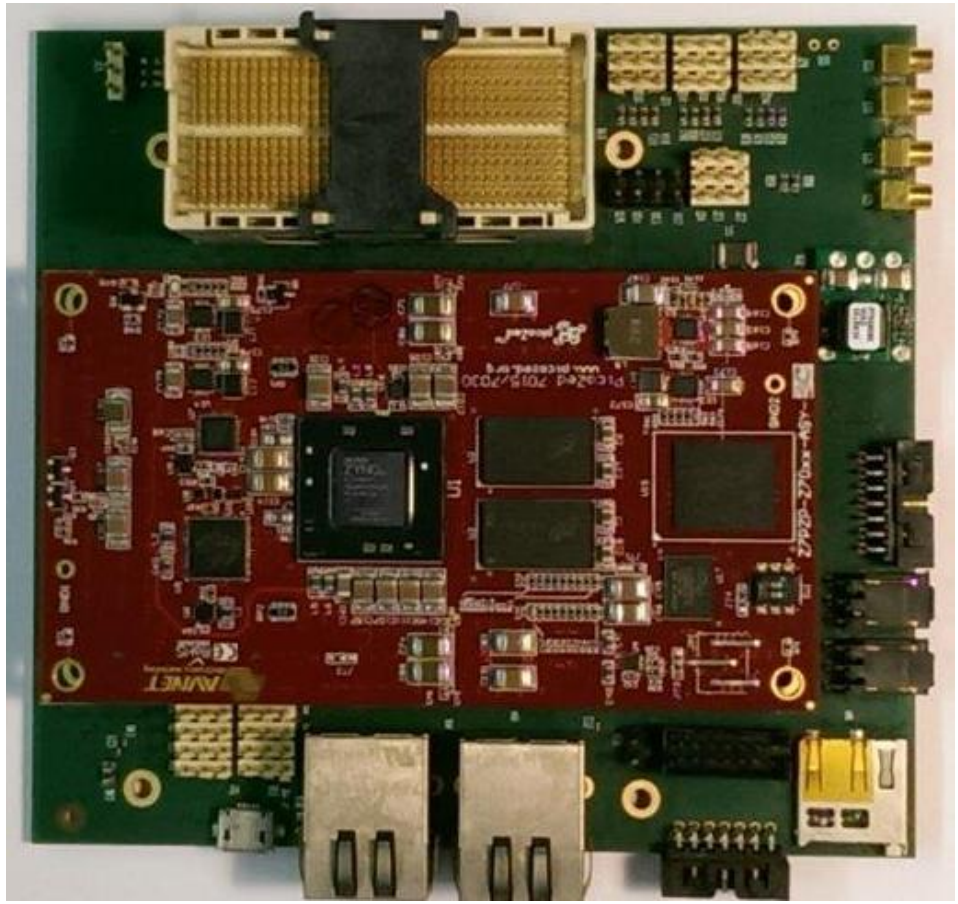
Vout Ripple measurement



VCCINT
MGTVCC
MGTVTT

Control mezzanines

- PicoZed (Zynq) carrier board
- Main functionalities
  - FPGA configuration (SelectMAP mode)
  - Jitter attenuating clock multiplying circuitry using the Si5345
  - Reception and decoding of the TTC (Trigger, Timing and Control)
  - IPBus master
  - Access to I2C buses

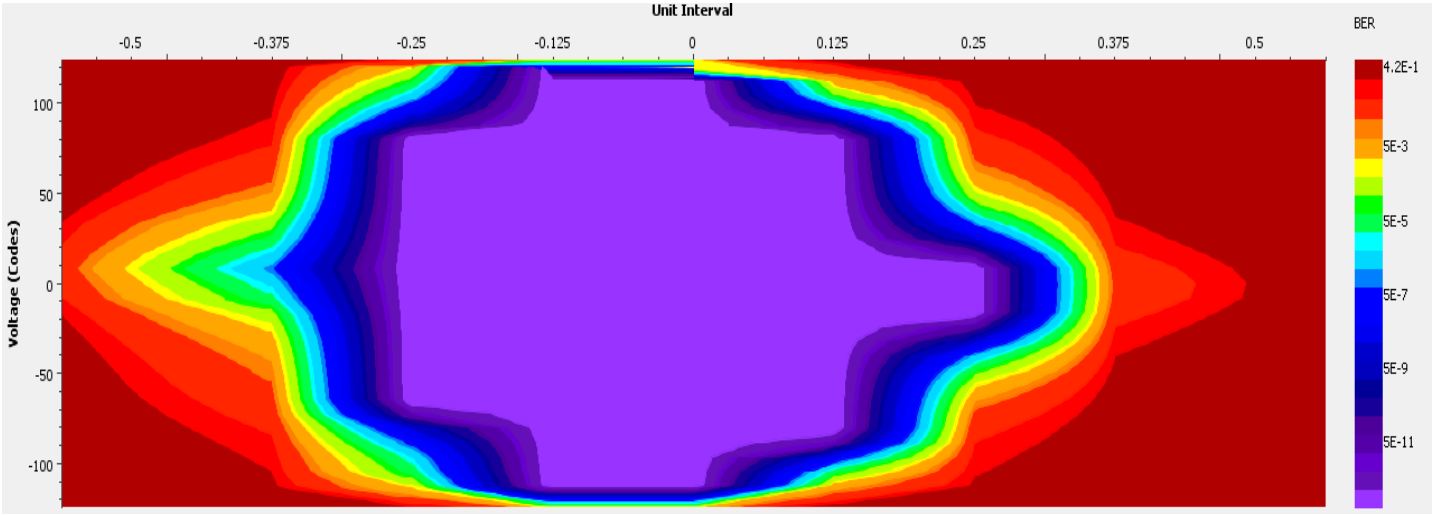


PMA loop-back measurement

- The jFEX algorithms require data duplication between the FPGA
- Use Xilinx Evaluation Board (VCU110) equipped with same Ultrascale FPGA used on jFEX to prove the feasibility of the data duplication

PMA Loop-back scheme

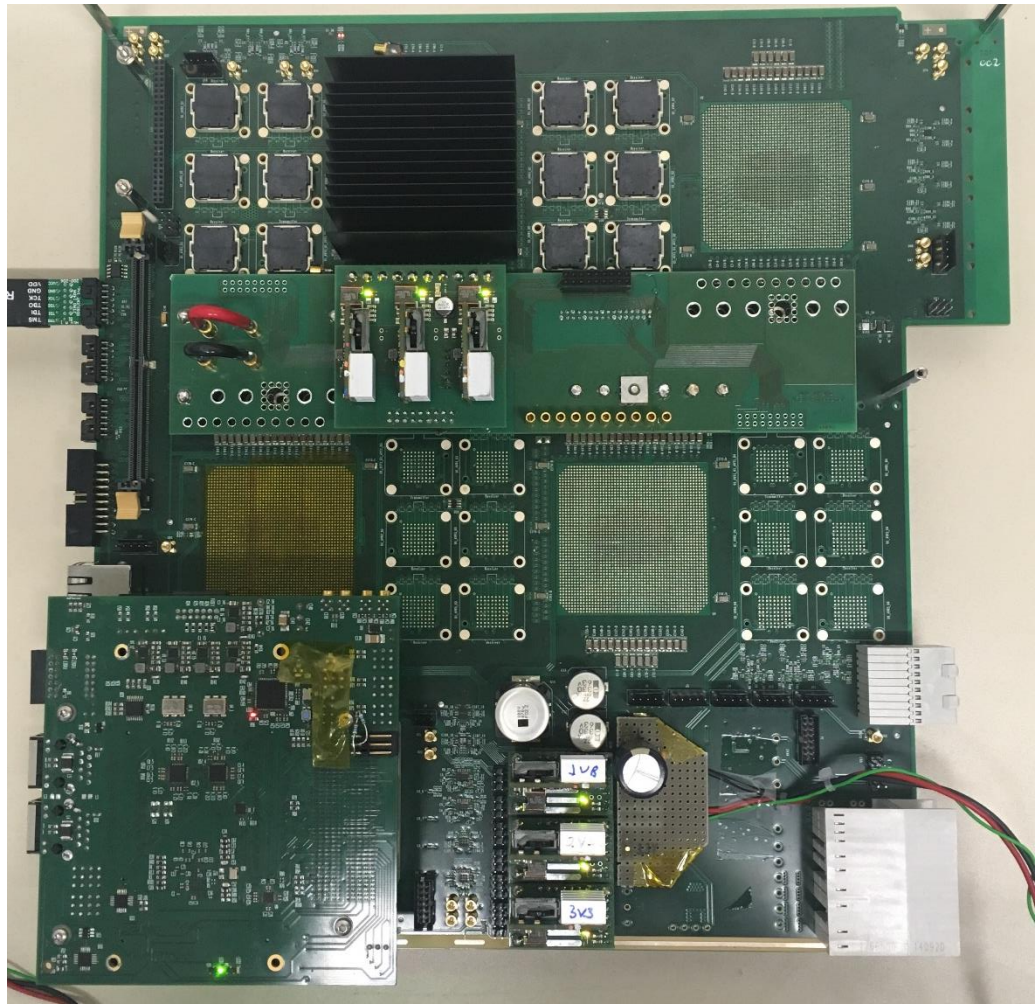
IBERT 2D eye-scan @28 Gbps



BER< 2.15x10^-16 @28 Gbps

jFEX prototype

- 1st prototype received December ’16
  - 1 FPGA; multiple FPGAs to be mounted on next PCB
- Preliminary tests
  - Power sequencing controlled by CPLD (XC2C256)
  - JTAG chain
  - Temperature monitor using XADC
    - Automatic shutdown
  - jFEX loop back test @12.8G with 12 links



Summary

- New conditions in the LHC after the Long Shutdown 2
  - Required the design of a new Level-1 Calorimeter trigger system
- One of the 3 feature extractors of the new L1Calo system is the jFEX
  - jFEX board is an ATCA board with 4 Xilinx Ultrascale FPGAs
  - Up to 120 MGT per FPGA
  - 2.4 Tbps input bandwidth
- First prototype equipped with one FPGA produced
  - Board layout optimised through power and thermal simulations
  - Very successful test results
    - Control and power mezzanines