# A REAL-TIME, DISTRIBUTED POWER MEASURING AND TRANSIENT RECORDING SYSTEM FOR ACCELERATORS' ELECTRICAL NETWORKS

E. Freddi, O. O. Andreassen, K. Develle, J. Lahaye, I. Mätäsaho, A. Rijllart, CERN, Geneva, Switzerland

# Abstract

Particle accelerators are complex machines with fast and high power absorption peaks. Power quality is a critical aspect for correct operation. External and internal disturbances can have significant repercussions causing beam losses or severe perturbations.

Mastering the load and understanding how network disturbances propagate across the network is a crucial step for developing the grid model and realizing the limits of the existing installations.

Despite the fact that several off-the-shelf solutions for real time data acquisition are available, an in-house FPGA based solution was developed to create a distributed measurement system. The system can measure power and power quality on demand as well as acquire raw current and voltage data on a defined trigger, similar to a distributed oscilloscope. In addition, the system allows recording many digital signals from the high voltage switchgear enabling electrical perturbations to be easily correlated with the state of the network.

The result is a scalable system with fully customizable software, written specifically for this purpose. The system prototype has been in service for two years and full-scale deployment is currently ongoing.

# **INTRODUCTION**

CERN's high voltage electrical network is composed of more than 100 substations that operate at voltage levels of 3.3 kV, 18 kV, 66 kV and 400 kV. With thousands of electrical equipment and a wide range of different technologies installed, the operation, control and supervision of the network constitutes a challenging task. Furthermore, the electrical network has a critical role in the accelerators' reliability, this being directly correlated to the network availability and quality of supply.

This paper presents a digital data acquisition system developed at CERN and called Transient Recording System (abbreviated CTRS). Its purpose is to perform transient analysis, measurements of network parameters (voltage, power), power quality and disturbances. One of main objectives of the CTRS is to correlate accelerators' instabilities to the electrical network behaviour.

The same hardware platform can be used to perform power flow analysis, just by swapping the on-board software.

Measurement of power flows is particularly important in the accelerators networks where the load profile is rapidly changing with spikes of several hundreds of kVA within a few seconds and with cycles lasting up to several minutes [1]. The power curves can be used for network analysis, either directly or in conjunction with computational models of the network.

Network disturbances also play an important role with the accelerators overall availability, having a great impact on the beam stability and often causing beam losses or perturbations. Understanding and identifying the correlations between power quality and beam stability helps to plan network consolidations and upgrades.

The transient recording function greatly benefits postmortem investigation after faults on the electrical network, reducing the time to diagnose the failure as well as giving important data for subsequent analysis.

In addition, the system is capable of providing power quality data for statistical purposes. Being based on a scalable platform, additional features can always be developed and added even with the system in service.

A number of different solutions ranging from an entire off-the-shelf to a fully in-house system have been explored in the early stage of the project [2]. The final solution tries to take the best from the two worlds, featuring a hybrid system composed by some commercial components, several in-house hardware parts and the software and its source code owned by CERN [3]. This option permits to control every system feature, also allowing interfacing it easily with other CERN monitoring systems such as beam or machines status.

# HARDWARE SETUP

The CTRS is a distributed data acquisition system (DAQ) able to monitor a scalable number of high voltage bays and other network-related analog or digital signals.

HV Busbars (18 kV, 3.3 kV)



Figure 1: Base configuration for analog acquisition.

and DOL In its base configuration (Fig. 1), the CTRS acquires publisher, three phase voltages and currents from a given feeder directly from the voltage and current transformers already installed in the cubicles. It is also capable of recording binary inputs such as circuit breaker statuses or dry work. contacts from other equipment. The selected acquisition unit is the CompactRIO-9035 from National Instruments. the

The power system signals are collected and conditioned of in a dedicated chassis before being sent to the analog to title digital converter (ADC).

author(s). The analog bandwidth of the input chain is 5 kHZ (-3 dB); for power quality measurement the system shall measure up to the 50<sup>th</sup> harmonic (2.5 kHz).

the The acquisition chain is designed to cope with potential attribution number of events such as short-circuits or overvoltage transients. Voltage and current probes from Verivolt LLC have been adapted to CERN specification and were tested during the development phase of the project.

naintain Short-circuit withstand is mainly achieved by interposing a measurement current transformer (MCT) on must the secondary circuitry of the protection CT; the MCT saturation limits the thermal stresses on the transducers in work case of primary short-circuit. In addition, the current probes have been specified to withstand 70 A for this 5 seconds: this allows for direct installation on the Content from this work may be used under the terms of the CC BY 3.0 licence (© 2017). Any distribution of secondary protection CT circuit, should it be required.

Table 1: DAO Main Specifications

1					
Analog Inpu	its				
Voltage channels count	32				
Rated voltage input	100 V				
Overvoltage withstand	$500 \mathrm{V} - 10 \mathrm{s}$				
Voltage cut-off frequency	5 kHz				
Current channels count	32				
Rated current input	1 A or 5 A				
Overcurrent withstand	70  A - 5  s				
Digital Inpu	its				
Number of channels	3 x 32				
Max. operating voltage and	$48~V~DC~\pm\!20\%$				
polarization output voltage					
cRIO interface voltage	15 V DC				
Digital Outp	uts				
Number of outputs	2 x 4				
Rated current / voltage	2 A / 250 Vrms				
Activation time	10 ms				
Release time	5 ms				
Common charact	eristics				
Inputs/outputs insulation	$> 100 \text{ M}\Omega$				
Common mode insulation	2.5 kV RMS				
Max. CM overvoltage	4.0 kV				
Max. DM overvoltage	1.0 kV				

Overvoltage atmospheric transients are infrequent since the CERN high voltage network is predominantly comprised of buried cables. Withstand capability (e.g.

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• 8 554 against indirect lightning) is achieved by the selected transducers that tolerate up to 500 V for 10 s. This equates to 90 kV on the network side without considering the damping effect of the voltage transformer, thus no additional protection equipment (surge arrestor) is required. To avoid potential aliasing problems, a low-pass second order filter tuned at 5 kHz is implemented in the voltage probes.

The analog input crate is engineered to collect up to 32 current signals and 32 voltage signals. The installed transducers convert the current inputs to voltage and scale down the voltage input to a suitable level for the cRIO-9205 ADC.

The digital input crate is built out of standard electronic components and allows optical isolation between the binary inputs and the cRIO-9425 acquisition module. The digital input crate can either send the polarity for the external dry contacts or receive externally polarized inputs.

The acquisition unit is located within a dedicated crate, which interfaces with the analog and digital input crates, as well as the CERN Technical Network (TN) for control and communication. The acquisition crate is directly powered from the high reliability 48 V DC supply of the substation where it is installed, with a step-down converter used to supply the 24 V DC required by the CompactRIO.

Table 1 lists the main DAO technical specifications.

#### SOFTWARE ARCHITECTURE

The initial development of the software has been outsourced to the company CIM.AS before being continued internally.



Figure 2: System architecture.

Each DAQ station is equipped with an on-board processor, allowing for direct analysis of acquired data, without the need to transfer it to an external unit. The software installed in the DAQ allows for continuous sampling, filtering and data processing. The DAQ primarily features:

• Sampling rate of 7.81 kHz, able to detect spikes and quick events;

- Continuous acquisition cycle, with trigger-dependant storage, i.e. the sampled and processed data is archived only upon an external or automatic trigger;
- Inter-trigger between units over Ethernet;
- Configurable recording window up to 10 s with settable pre- and post-periods;
- Real-time FFT analysis, primarily for power quality (harmonics) measurement;
- Remote configuration and programming capabilities, with different configurations to fit each specific substations' needs;
- Automatic recognition of disturbances type and characteristics, e.g. voltage variations magnitude and duration;
- Export data in COMTRADE format [4];

The CERN IT network architecture presents two separated networks: the Technical Network, dedicated to the accelerators and technical services, and the General Purpose Network for offices and infrastructure.

The CTRS is designed as a distributed architecture, connected on the TN. To be able to access the system from the GPN, a central controller interfaces the data viewer and the configuration tools with the DAQ (Fig. 2).

Each DAQ station is composed by two separate layers: an FPGA application and a Real Time (RT) application.

The FPGA acquires raw data, buffer and transfer it to the RT application. Additionally, the FPGA can control different relay outputs to give information of the cRIO status. FFT calculation is also carried out within the FPGA, taking advantage of its high speed.





The RT application has multiple functions. It analyses the raw signals received from the FPGA, maintains a data buffer in order to save the data in case of trigger and communicates with the central controller. In order to reduce FPGA memory overhead, the Real-Time application buffers some data before sequentially sending it back to the FPGA for FFT calculation. Figure 3 illustrates the architecture of the DAQ station software.

All the DAQ stations can be configured remotely. The system features channel-specific triggering; for each channel, different triggers can be configured: maximum or minimum instantaneous value, maximum or minimum RMS value in a cycle (50 Hz), over- and under-frequency, harmonics content. Triggering can also be propagated over the different DAQ stations; this allows taking a "snapshot" of the entire electrical network when a problem occurs.

 Table 2 synthetises the main system technical data.

 Table 2: Main System Performances

	Tormanees
Analog Acquisiti	ion
Sampling frequency	7.81 kHz
Maximum recording length	10 s
Data rate	1.25 Mb/s
Input range	$\pm 5 \mathrm{V}$
Conversion time	4 μs
Analog input resolution	16 bits
Synchronizatio	n
Synchronization accuracy	< 2 ms
Global triggering delay	< 10 ms

# **USER INTERFACE**

The user interface is composed of two applications, one for the system configurators and one for the operators.

The configuration tool shown in Fig. 4 allows setting up each channel of every DAQ station. Setup includes gain, offset, trigger thresholds and trigger types. The configuration tool communicates directly with the central controller, and it can be used to send a general trigger to all the DAQ stations at once.

172.18.203.10 Master Connected	Control 09:36:11 08/21/2017					🔁 check DS sync				Frit Exit	
vetwork Status			C	C Setup			D S Setu	p			
AQ Station BE:172.18.193.78									0	Apph	
General AI	DI			AlTrigger			DITrigger			Relay	
I Channel		Enabled	Mask T.O.	Mask Enabled	Data Gain	Data Offset	Spec. Gain	Spec. Off	Identifier	Phase I	
Enable Channel	AICh000	True	01:00:00.00	False	22,060	0.010	1.010	0.000	EMD1 BE	R	
fask	AICh001	True	01:00:00.00	False	22,060	0.010	1.010	0.000	EMD1 BE	s	
	AICH/02	True	01:00:00.00	False	22.060	0.010	1.010	0.000	EMD1 BE	т	
HASK TIMEOUT ENADIE MASK	AJCh/03	True	01:00:00.00	False	821.000	0.010	1.010	0.000	401kV_UR	R	
00:00:00 00	AJCh/04	True	01:00:00.00	False	821.000	0.010	1.010	0.000	401kV_US	S	
MM/DD/YYYY	AJChI05	True	01:00:00.00	False	821.000	0.000	1.010	0.000	401kV_UT	Т	
	AJCh106	True	01:00:00.00	False	22.868	0.000	1.010	0.000	EMD1_BE_L	R	
aling	AICh807	True	01:00:00.00	False	22.868	0.000	1.010	0.000	EMD1_BE_L	S	
0.00 Data Gain 0.00 Data Offset	AICHI08	True	01:00:00.00	False	22,860	0.000	1.010	0.000	EMD1_BE_L	Т	
101 Spartnum Gain 0.00 Spartnum Offrat	AICh009	True	01:00:00.00	False	22,060	0.010	1.010	0.000	EMD2 BE L	R	
apectuari carri apectuari cinec	AICh010	True	01:00:00.00	False	22,060	0.010	1.010	0.000	EMD2 BE L	S	
nalog Channel Info	AJCh011	True	01:00:00.00	False	22.060	0.010	1.010	0.000	EMD2 BE L	т	
Channel Identifier Channel Phase Identification	AJCh012	True	01:00:00.00	False	22.060	0.010	1.010	0.000	EMD3_BE_L	R	
	AJCh013	True	01:00:00.00	False	22.060	0.010	1.010	0.000	EMD3_BE_L	S	
Vionitored Circuit Components	AJCh014	True	01:00:00.00	False	22.060	0.000	1.010	0.000	EMD3_BE_L	Т	
	AICh015	False	01:00:00.00	False	22,060	0.000	1.010	0.000			
Chappel Units	AJCh016	False	01:00:00.00	False	22,860	0.010	1.010	0.000			
	AICh017	False	01:00:00.00	False	22,060	0.010	1.010	0.000			
Channel Time Skew (ur)	AICh018	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
o	AJCh019	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
0	AJCh020	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
Min Data Value Max Data Value	AJCh021	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
0 0	AICh022	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
Transformer Ratio Primary Factor	AJCh023	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
0	AJCh024	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
Primary/Secondary Data Scaling Identifier	AICh025	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
S .	AJCh026	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
Fransformer Ratio Secondary Factor	AJCH027	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
0	AJCH/J28	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
	Alch029	False	01:00:00.00	False	1.010	0.010	1.010	0.000	AICh017		
	*										

Figure 4: Configuration tool interface.

The data viewer depicted in Fig. 5 is a COMTRADE file reader with searching and filtering capabilities for files on the storage server. Despite fact that the files recorded by the CTRS can be read by any COMTRADE compatible software, the data viewer is embedded in the electrical SCADA system [5] and it is particularly suited for filtering the many recordings available after an event.



# **FUTURE DEVELOPMENTS**

The CERN Transient Recording System has been presented and the main features highlighted in this paper. The system has been in development for four years and it is now being deployed in the main HV substations.

Further developments of the system are ongoing or planned, with a particular focus on:

- Improving of the automatic disturbance type recognition for statistical analysis and data consolidation;
- Automatically linking the electrical perturbation on the network to the accelerators' behaviour (RF and magnets) during the run in order to discover and potentially prevent incipient failure modes;
- Improving the data viewer capabilities to allow advanced COMTRADE file analysis, automatic selection of the most relevant recordings after a network fault or disturbance to help the operation teams to better identify the type and the cause of the problem;
- Implementing a continuous acquisition and storage mode with scalable base time, e.g. hourly, daily or weekly.

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