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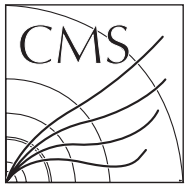

The Compact Muon Solenoid Experiment

Conference Report

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The front-end data conversion and readout electronics for the CMS ECAL upgrade

Gianni Mazza for the CMS Collaboration

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The High Luminosity LHC (HL-LHC) will require a significant upgrade of the readout electronics for the CMS Electromagnetic Calorimeter (ECAL). The Very Front-End (VFE) output signal will be sampled at 160 MS/s (i.e. four times the current sampling rate) with 13 bit resolution. Therefore, a high-speed, high-resolution ADC is required. Moreover, each readout channel will produce 2.08 Gb/s, thus requiring fast data transmission circuitry. A new readout architecture, based on two 12 bit, 160 MS/s ADCs, lossless data compression algorithms and fast serial links have been developed for the ECAL upgrade. These functions will be integrated in a single ASIC which is currently under design in a commercial CMOS 65 nm technology using radiation damage mitigation techniques.

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The front-end data conversion and readout electronics for the CMS ECAL upgrade.

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Abstract: The High Luminosity LHC (HL-LHC) will require a significant upgrade of the readout electronics for the CMS Electromagnetic Calorimeter (ECAL). The Very Front-End (VFE) output signal will be sampled at 160 MS/s (i.e. four times the current sampling rate) with a 13 bits resolution. Therefore, a high-speed, high-resolution ADC is required. Moreover, each readout channel will produce 2.08 Gb/s, thus requiring a fast data transmission circuitry. A new readout architecture, based on two 12 bit, 160 MS/s ADCs, lossless data compression algorithms and fast serial links have been developed for the ECAL upgrade. These functions will be integrated in a single ASIC which is currently under design in a commercial CMOS 65 nm technology using radiation damage mitigation techniques.

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1 Introduction

The Compact Muon Solenoid (CMS) detector is one of the four main experiments of the Large Hadron Collider (LHC) accelerator at CERN. It is a general-purpose detector which is designed to observe any new physics phenomena that LHC might reveal. CMS features two calorimeters for the measurement of the energies of the particle produced in the collisions, the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL).

The CMS ECAL, shown in Fig. 1, consists of a barrel section and two endcaps and is located between the silicon tracker, which is the detector closest to the beam line, and the HCAL. The cylindrical barrel consists of 61200 $PbWO_4$ crystals divided into 36 supermodules and 2448 readout units. Each readout unit is divided into 5×5 crystals connected to Avalanche PhotoDiodes (APDs).

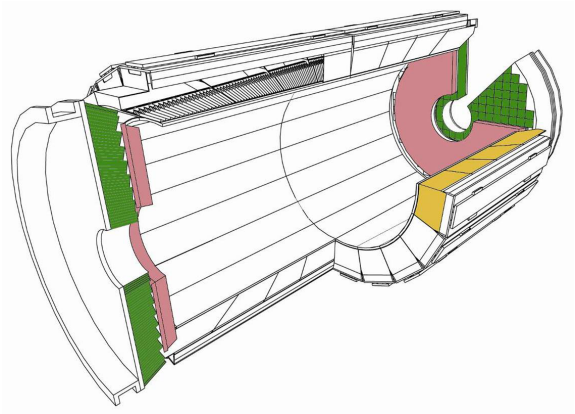

Figure 1. The CMS Electromagnetic Calorimeter.

The upgrade of the LHC accelerator and the draft schedule of the High Luminosity LHC program will result in an increase by about a factor of five of the luminosity and by one order of magnitude of the integrated luminosity [1].

The LHC upgrade has a number of implication in the design of the ECAL detector. The APDs operating temperature will be reduced from 18 °C to 9 °C in order to mitigate the radiation damage. An improved rejection of signals from direct hadron interaction in the APD (spikes) is also required, toghether with the need to cope with an increased pile-up (up to 200 events). It is therefore required an upgrade of the barrel ECAL readout electronics. The upgrade must also cope with the foreseen level-1 trigger increase in both rate (from 150 kHz to 750 kHz) and latency (from 6.4 μm to 12.5 μm).

2 The CMS ECAL readout architecture

The legacy readout architecture is shown in Fig. 2. The APDs are readout by a Multi-Gain Pre-Amplifier (MPGA) [2] which provides three outputs with different gain (namely $\times 1, \times 6$ and $\times$ 12) for each APD . The three outputs are converted by a multi-channel, 12-bit, 40 MS/s ADC chip [3]. The MPGAs and ADCs are hosted by a Very Front-End (VFE) card connected to the APDs via kapton cables. The ADC outputs are sent to a two-level data concentrator and trigger generator circuit based on the FENIX ASIC [4]. The FENIX output is then sent out via an optical transceiver [5] to the DAQ and trigger systems. The FENIX and the optical transceiver circuitry are mounted on a Front-End (FE) card, which controls five VFE cards.

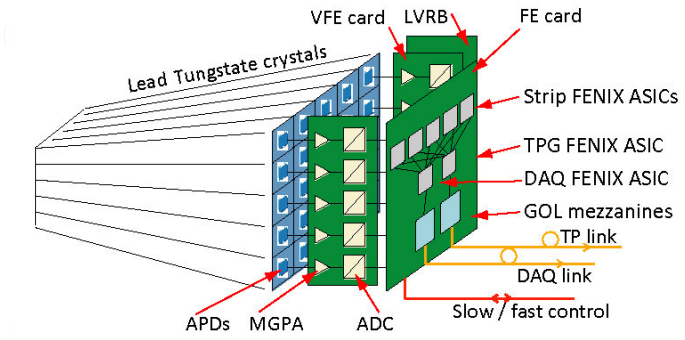

Figure 2. The CMS ECAL legacy readout system.

The readout system depicted in Fig. 2 will not be able to satisfy the requirements of the ECAL upgrade. A higher bandwidth preamplifier and a faster sampling rate are needed to improve the spike rejection and to cope with the increased pile-up. The fourfold increase in sampling rate leads to a proportional increase in data rate, entailing the redesign of the FE circuitry.

In order to cope with the new requirements a new readout scheme has been proposed [6] and is depicted in Fig. 3.

In the new system the MGPA charge sensitive preamplifier is replaced by a faster Trans-Impedance Amplifier (TIA), in order to follow as close as possible the input signal

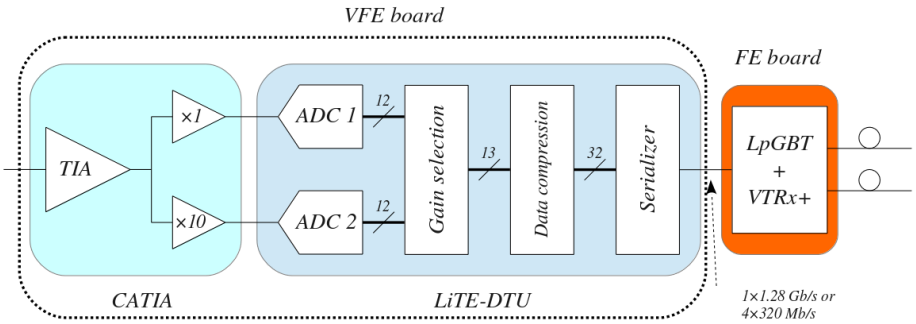

Figure 3. New readout system.

shape. The TIA provides two output gains (namely ×1 and × 10) which are fed to a dual 12-bit, 160 MS/s ADC. The ADC data, after gain selection and data compression, are connected to the lpGBT optical transceiver [7] without data concentrator electronics.

3 ASIC developments

Two custom ASIC developments are ongoing in order to cope with the new requirements in terms of input bandwidth, conversion rates, transmission rates and radiation tolerance. The two ASICs, named CATIA and LiTE-DTU, will be hosted by a new VFE board with the same form factor and cooling system as the legacy system.

3.1 CATIA preamplifier

The CATIA (CAlorimeter TransImpedance Amplifier) is a fully analog ASIC designed in a commercial CMOS 130 nm technology. It is based on a regulated cascode common gate input stage in order to obtain high bandwidth and low input impedance. The input stage drives two output amplifiers with gains ×1 and ×10. The output stages provide differential outputs with a differential voltage swing of 1.2 V.

A first prototype (with single-ended drivers) has already been produced and succesfully tested. A transimpedance gain of 275 Ω has been measured with a bandwidth of 35 MHz. The equivalent input noise is around 170 nA. The prototype has been tested connected to the detector in dedicated beam tests to assess whether the performances are sufficient for the ECAL application. Beam test data analysis is currently ongoing.

3.2 LiTE-DTU

The LiTE-DTU is a data conversion, compression and transmission ASIC which is designed to be coupled with the CATIA amplifier. The ASIC, currently under design, will be implemented in CMOS 65 nm technology and is based on a 12-bit, 160 MS/s radiation tolerant ADC IP block. A simplified schematic of the LiTE-DTU is shown in Fig. 4.

The ADC is the most critical component of the LiTE-DTU. It has to provide a resolution of 12-bit at Nyqvist frequency with a sampling rate of 160 MS/s. Moreover, it has to sustain a maximum total ionizing dose of 10 kGy and implement a single event upset

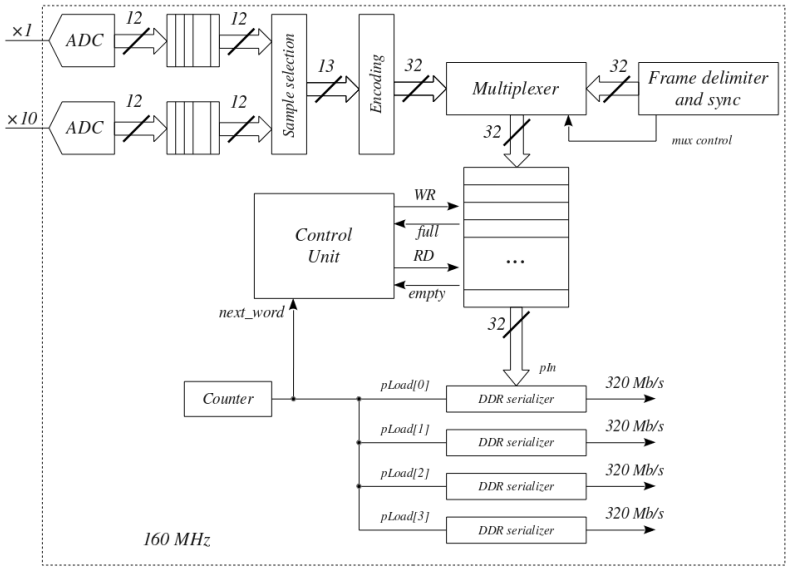

Figure 4. A simplified schematic of the LiTE-DTU ASIC.

protected control logic. Two ADC blocks will be integrated in the LiTE-DTU in order to convert in parallel the two outputs of the CATIA ASIC.

The ADC will be based the successive approximation architecture which can provide the required resolution and sampling rate at lower power consumption than other architectures (e.g. pipeline or folding and interpolating). Owing to the challenging requirements, the design of the ADC cell will be done by an external company with experience in design of such high resolution, high sampling rate converters.

3.3 Data selection and compression

The converted data from the two ADCs will be fed into two small FIFOs, as depicted in Fig. 4. For each time slot, the high-gain sample will be selected if none of high-gain samples in an appropriate time window around it are saturated, as illustrated in Fig. 5, where a typical sequence of sampled events for the two gains are shown. Here the red and blue crosses represent the samples taken at 160 MHz for the high- and the low-gain, respectively. This algorithm prevents the mixing of samples from different gains in the same detector signal.

The LiTE-DTU is designed to be directly connected to the lpGBT and Versatile Link+ radiation tolerant transceiver and optical module. The lpGBT provides a 8.96 Gb/s user bandwidth (in FEC5 mode) over a optical link. The interface with the front-end is based on differential electrical links at 320, 640 or 1280 Mb/s.

The lpGBT modularity does not match well with the LiTE-DTU one, since its output bandwidth is 2.08 Gb/s per channel. However, it is possible to take advantage of the statistical distribution of the output values to perform a lossless compression based on the Huffman encoding [8]. Indeed, the probability to have events with more than 6 and 7 significant (non-zero) bits is below 2.4×10^{-4} and 1.4×10^{-5}, respectively.

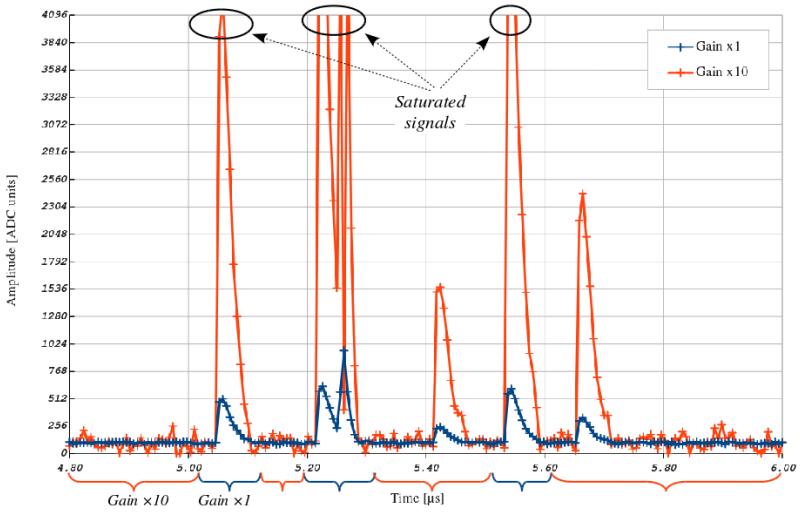

Figure 5. Illustration of the data selection algorithm.

Figure 6 shows a possible data encoding scheme. The data are organized in 32-bit packets. Each packet can accomodate up to five 6-bits consecutive samples ("baseline" data formats) or up to two 13-bits samples ("signal" data formats). Both "baseline" and "signal" data formats are encoded in two versions depending on whether it is possible to fill the packet with consecutive samples of the same type. A frame delimiter packet is inserted every 51 packets in order to check the correctness of the data. The frame delimiter includes the number of samples in the frame, the frame number and a CRC of the data in the frame.

"Baseline" data format	01	6 bits sample	6 bits sample	6 bits sample	6 bits sample	6 bits sample
"Baseline" data format 1	10	sample map	6 bits sample/00	6 bits sample/00	6 bits sample/00	6 bits sample
"Signal" data format	001010	13 bits sample	13 bits sample			
"Signal" data format 1	001011	0101010101010	13 bits sample			
Frame delimiter	1101	8 bits #samples	CRC12	8 bits frame #		
Idle pattern	1110	101010101010				

Figure 6. Data encoding scheme.

The estimated data rate for the encoding scheme is 1.08 Gb/s, thus leaving a 16% free bandwidth on the 1.28 Gb/s (or 4×640Mb/s) available lpGBT electrical link bandwidth. An idle packet with a clock-like pattern is inserted when no data is available in order to avoid a loss of synchronization on the lpGBT side.

The data is thus encoded in 32-bit packets and inserted into a FIFO which is used to compensate for the packet rate variation intrinsic to the compression process. The FIFO size will be determined to provide a trade-off between the amount of data to be stored in

high pile-up events and the system latency. The FIFO output is continuosly read-out by four 320 Mb/s serializers and sent to the lpGBT.

4 Summary

The CMS ECAL upgrade foresees a redesign of the front-end electronics in order to cope with the new, more demanding requirements. The most critical ones are the improved rejection of signals from direct hadron interaction in the APD and the increased pile-up, since they require a faster front-end amplifier, a higher sampling rate and, as a consequence, a higher output bandwidth.

Therefore both the VFE and the FE cards and ASICs will be redesigned. The VFE card will be based on two new ASICs, the input preamplifier CATIA and the data conversion, compression and transmission logic LiTE-DTU. The first prototype of the CATIA ASIC has already been produced in a commercial CMOS 130 nm technology and tested, while the second version is currently been designed. A first synthesized version of the LiTE-DTU architecture has been designed and is currently under extensive simulations, while the ADC IP block will be designed by an external company. Full protoypes of both ASICs will be sent to foundry for production in 2018.

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