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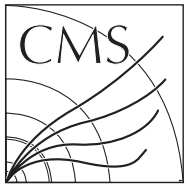

The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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Next generation ATCA control infrastructure for the CMS Phase-2 upgrades

Wesley Smith for the CMS Collaboration

Abstract

A next generation control infrastructure to be used in Advanced TCA (ATCA) blades at the CMS experiment is being designed and tested. Several ATCA systems are being prepared for the High-Luminosity LHC (HL-LHC) and will be installed at CMS during technical stops. The next generation control infrastructure will provide all the necessary hardware, firmware and software required in these systems, decreasing development time. It includes an Intelligent Platform Management Controller (IPMC), a Module Management Controller (MMC) and an Embedded Linux Mezzanine (ELM) processing card. The chosen architectures, their testability, integration and the advantages over existing solutions will be discussed.

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PROCEEDINGS OF SCIENCE

Next generation ATCA control infrastructure for the CMS Phase-2 upgrades

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A next generation control infrastructure to be used in Advanced TCA (ATCA) blades at CMS experiment is being designed and tested. Several ATCA systems are being prepared for the High-Luminosity LHC (HL-LHC) and will be installed at CMS during technical stops. The next generation control infrastructure will provide all the necessary hardware, firmware and software required in these systems, decreasing development time and increasing flexibility. The complete infrastructure includes an Intelligent Platform Management Controller (IPMC), a Module Management Controller (MMC) and an Embedded Linux Mezzanine (ELM) processing card.

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[1]Speaker

1. Introduction

Several institutes are presently designing hardware, firmware and software that will be used in CMS for data taking during the High Luminosity LHC (HL-LHC) physics runs, starting in 2025 [1]. Most of the architectural choices have been focused in designing Advanced TCA (ATCA) blades and, as part of the PICMG 3.x standard [2], each blade needs to implement a set of control and management functionalities.

The next generation control infrastructure presented includes three different hardware systems that together implement the PICMG 3.x standard, provide additional features, flexibility and decrease the time necessary to design and test an ATCA blade.

1.1 Embedded Linux Mezzanine

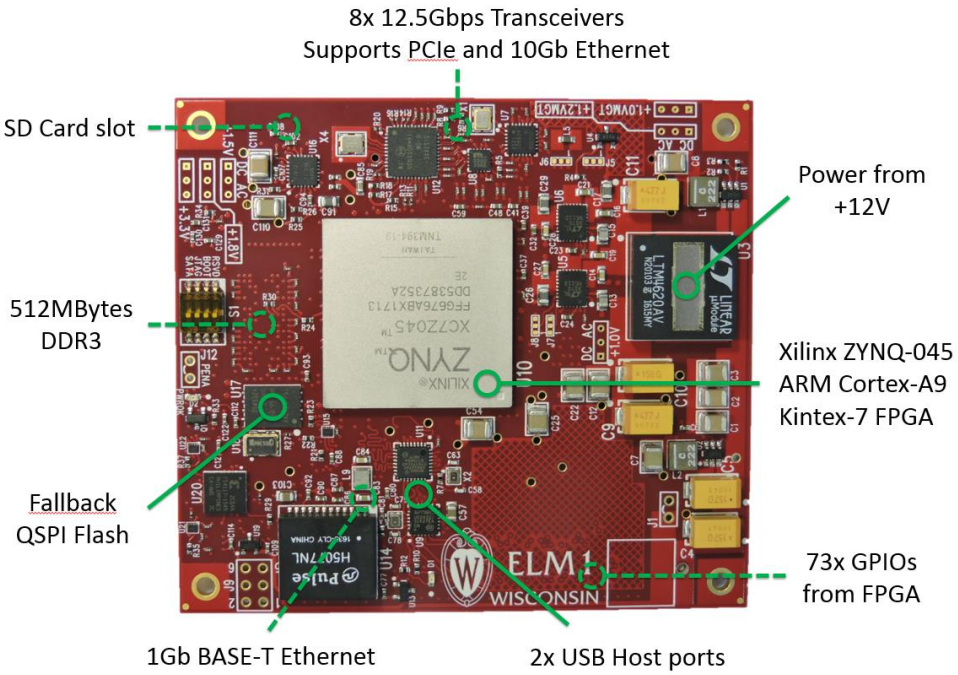

Figure 1: Embedded Linux Mezzanine (ELM)

The Embedded Linux Mezzanine (ELM), depicted in Figure 1, is intended to be used as the blade's on-board computer and its primary access point. It features a dual core ARM processor packed inside a high-end Xilinx ZYNQ System-on-Chip (SoC) running a full-fledged Linux distribution. Expandability is provided by the ZYNQ's FPGA section where 73 general purpose input/outputs (GPIOs) and 8 multi-gigabit transceivers (MGTs) are available to the hardware designer and can drive several standards and custom protocols, such as:

- JTAG Master Controller (Xilinx Virtual Cable),
- AXI Chip2Chip (parallel high-speed GPIOs, Aurora),
- PCI Express (x1, x2, x4 and x8 lanes),
- 10Gbit Ethernet (XFI, XAIU).

Blade peripherals are connected to GPIOs or MGTs and configured using Xilinx ecosystem, predominantly made up of Xilinx Vivado and standard AXI inter-connectivities. Common peripherals can be other FPGAs (e.g. Xilinx Ultrascape+) or simpler devices such as EEPROMs, allowing them to be accessed and configured through Linux or exposed by Ethernet. Figure 2 exemplifies how the ELM can be connected to other peripherals.

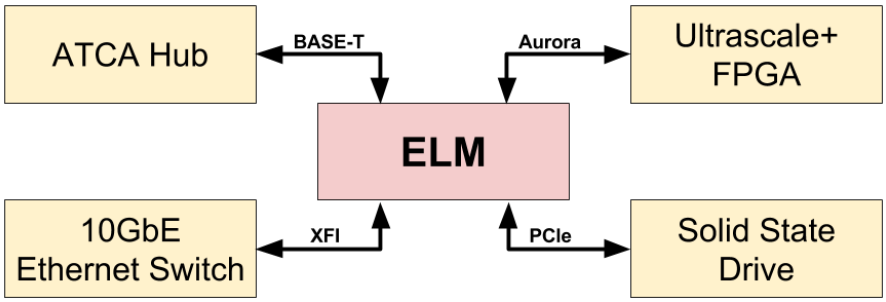

Figure 2: ELM connectivity example

1.2 Intelligent Platform Management Controller

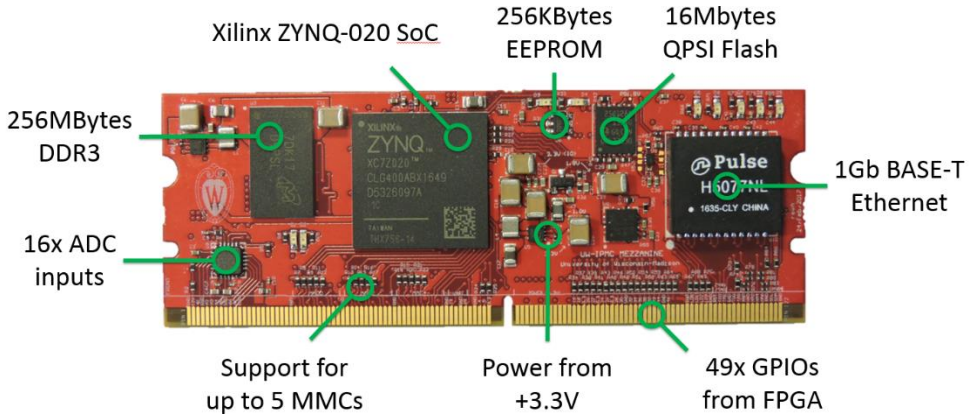

Figure 3: Intelligent Platform Management Controller (IPMC)

The Intelligent Platform Management Controller (IPMC) mezzanine, shown in Figure 3, is intended to be the next generation of blade controllers that communicate with ATCA Shelf Managers (ShMC). It is part of the PICMG 3.x specification and each blade needs to have one of such controllers. They are responsible for doing blade related health checks (e.g. temperature, voltages) and to act in case of problems, such as over-temperature or over-voltage.

The IPMC design has a low-cost Xilinx ZYNQ SoC that runs FreeRTOS, which is ideal for time sensitive applications, and uses FPGA logic to do parallel comparisons of sensor data versus threshold values, allowing the IPMC to trigger on alarms at sub-millisecond rates. The firmware, depicted in Figure 4, uses FreeRTOS queues coupled with a publisher/subscriber broker system to relay important messages across different tasks, such system allows for easy debugging and logging when needed.

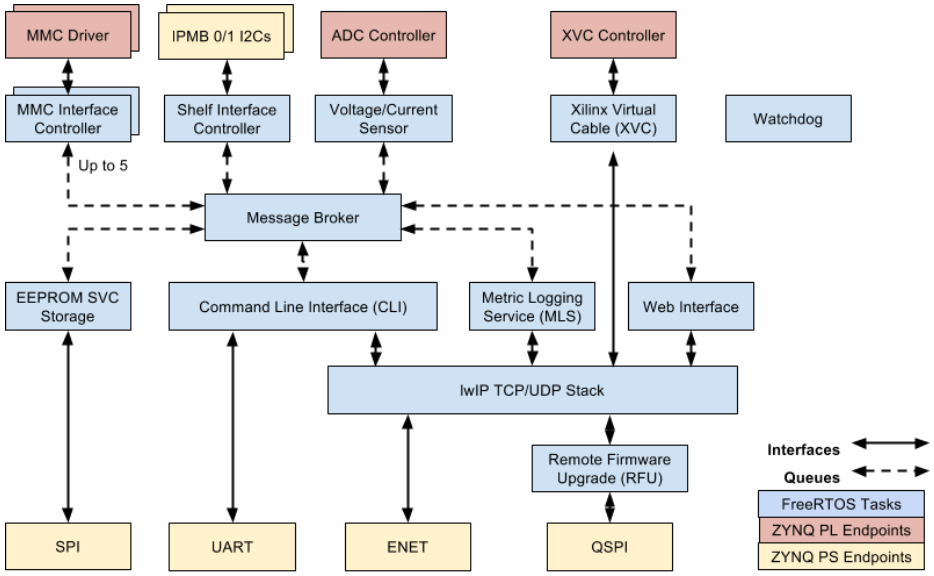

Figure 4: IPMC firmware and software architecture

Five independent Modular Management Controller (MMC) interfaces allows the IPMC to manage Advanced Mezzanine Cards (AMCs), this prevents bus locking in case one AMC fails during operation. For expandability, 49 GPIOs are available at the mezzanine connector and wired to the FPGA section, allowing the IPMC to interface with power, monitoring or management related components on the ATCA blade. They can also be used to add more MMC interfaces.

Access to the IPMC is done through Ethernet via the ATCA Hub card or through the IPMI bus.

1.3 Module Management Controller

The next generation Module Management Controller (MMC) is provided as a reference design and not as a mezzanine due to its simplicity. The design moves away from RISC architectures to ARM microprocessors by using Atmel's SAM4N. Similarly to IPMCs, several ADCs and GPIOs allow the MMC to manage and monitor AMCs which are pluggable and hot-replaceable modules in ATCA blades. Rear Transition Modules (RTMs) are also supported.

The firmware implementation uses FreeRTOS for time sensitive tasks, such as sensor monitoring and alarming. Communication with the IPMC is done through a dedicated I2C bus.

References

[1] Contardo, D., Klute, M., Mans, J., Silvestris, L., Butler, J., *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, HCC-P-008

[2] PICMG, *AdvancedTCA Base Specification 3.0*, Revision 3.0