AIDA-2020-MS64

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

Milestone Report

Final design review of 130nm ASICs

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Advanced European Infrastructures for Detectors at Accelerators

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MILESTONE REPORT

FINAL DESIGN REVIEW OF 130NM ASICS

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Abstract:

The chip that will be used to read out the SIPM calorimeter of WP13 and the RPC timing detector of WP14 was reviewed by external experts before fabrication. Their recommendations led to the fabrication of the 32-channel chip in July 2017, so that it can meet deliverable D4.2 (Month 36).

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 4 years.

Delivery Slip

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Executive summary

The choice of TSMC130 nm in milestone MS22 and large commonalities with calorimeter upgrades at the LHC have led to the design of a versatile ASIC which matches the requirements of WP13 and WP14. The ASIC has been reviewed by external experts in April 2017. The timetable of review meeting is available at https://indico.cern.ch/event/634985/. The fabrication of the chip was launched in July 2017 allowing the completition of deliverable D4.2.

1. INTRODUCTION

Task 4.3 targets high speed, low noise, large dynamic range ASICs for calorimeter readout and high speed timing measurements. These ASICs will be used to read out the detectors of WP13 and WP14, which constitute the deliverables of WP4.3. The choice of TSMC130 nm in milestone M23 made it possible to optimize synergies with calorimeter upgrades, in particular the HGCAL developed for CMS upgrade.

2. ASIC DESCRIPTION

The chip developed for the applications in WP13 and WP14 is a very versatile 32-channel ASIC named HGCROC. It provides a charge measurement over a 10 pC range, which is split into two modes. One linear range is read by a 10 bits ADC up to 100 fC with 0.1 fC resolution. The other range is read with a Time over Threshold (TOT) technique, when the preamplifier saturates, covering 100 fC to 10 pC on 12 bits with 2.5 fC resolution. The noise level is kept below 0.32 fC (2000 electrons) for a 60 pF detector capacitance. The ASIC also provides the Time of Arrival (TOA) information with 20 ps resolution for signal larger than 10 fC. Charge and time information are stored in a large memory for 12.5 µs to wait for a valid L1 trigger and read out at 1.28 Gb/s e-links.

With this architecture the chip can be used to read out Silicon diodes as in the HGCAL of CMS upgrade, Silicon photomultipliers for WP13 and RPCs foreseen for WP14 or CMS muon chambers upgrade.

The chip has been designed as a collaboration between CERN, CEA/IRFU and Imperial College.

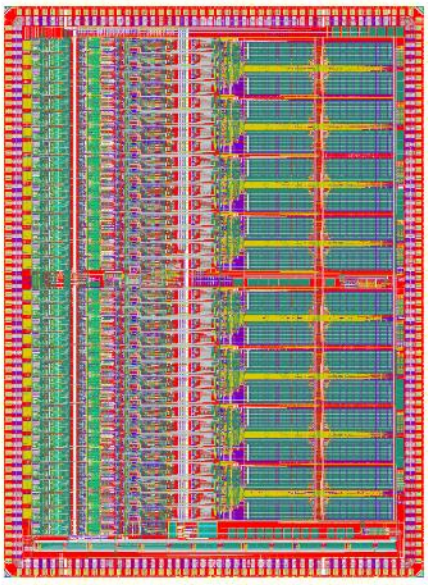
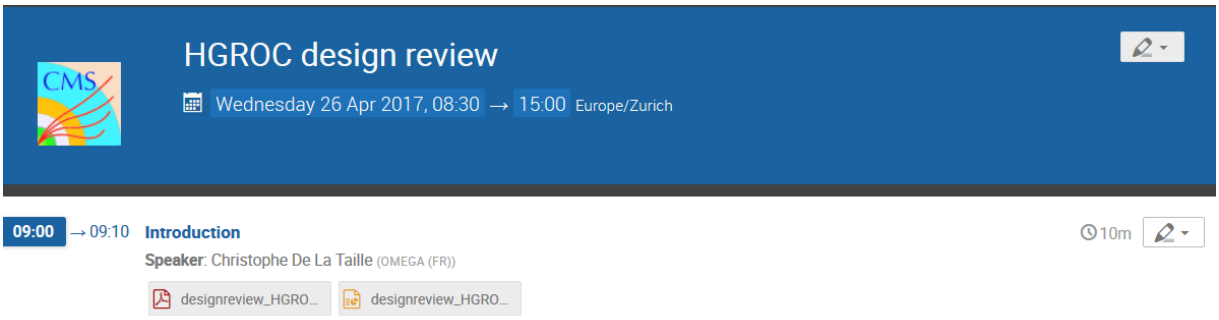


Figure 1: View of the HGCROC chip layout.

3. DESIGN REVIEW OUTCOME

The chip was reviewed at OMEGA by Johan Borg (Imperial), Olivier Gevin (IRFU), Kostas Kloukinas (CERN) and Sandro Marchioro (CERN). Details can be found at https://indico.cern.ch/event/634985/



During the review, the detailed schematics and layouts were examined as well as the simulation results. The main analog part had been tested previously thanks to two test vehicles fabricated in 2016 and reported in ref [1]. The digital part and the testability have been improved thanks to the reviewer's comments.

4. CONCLUSION

Following the review results, the ASIC has been validated and sent to fabrication in July 2017. It will be received in October 2017 and constitute deliverable D4.2

The review achieves successfully milestone MS64.

5. REFERENCES

[1] D. Thienpont et al. « Test vehicles for CMS HGCAL readout ASIC » proceedings of the TWEPP 2017 conference Santa Cruz USA