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Depleted fully monolithic CMOS pixel detectors using a column based readout architecture for the ATLAS Inner Tracker upgrade

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Abstract: Depleted monolithic active pixel sensors (DMAPS), which exploit high voltage and/or high resistivity add-ons of modern CMOS technologies to achieve substantial depletion in the sensing volume, have proven to have high radiation tolerance towards the requirements of ATLAS in the high-luminosity LHC era. Depleted fully monolithic CMOS pixels with fast readout architectures are currently being developed as promising candidates for the outer pixel layers of the future ATLAS Inner Tracker, which will be installed during the phase II upgrade of ATLAS around year 2025. In this work, two DMAPS prototype designs, named LF-MonoPix and TJ-MonoPix, are presented. LF-MonoPix was designed and fabricated in the LFoundry 150 nm CMOS technology, and TJ-MonoPix has been designed in the TowerJazz 180 nm CMOS technology. Both chips employ the same readout architecture, i.e. the column drain architecture, whereas different sensor implementation concepts are pursued. The design of the two prototypes will be described. First measurement results for LF-MonoPix will also be shown.

Keywords: Depleted monolithic CMOS pixels, particle tracking detectors (solid-state detectors), Front-end electronics for detector readout, VLSI circuit

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Contents

1 Introduction

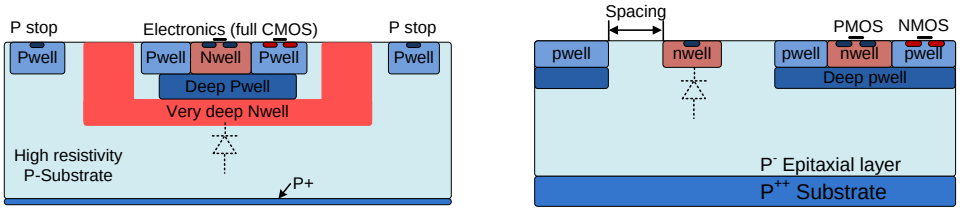
Monolithic active pixel sensors (MAPS) have already matured enough to be used in high energy physics experiments, as high precision tracking and vertexing devices [1–3]. They are now making their path into the high-rate and high-radiation applications, where a depleted sensing volume is mandatory for charge to be collected sufficiently fast by drift [4]. CMOS pixels with depleted sensing volume, also labelled as depleted monolithic active pixel sensors (DMAPS), can be achieved by exploiting the high-resistivity and/or high-voltage add-ons of modern CMOS technologies. Many such devices have been reported, showing high radiation tolerance towards the requirements of experiments in the High-Luminosity LHC (HL-LHC) era [5–8]. Moreover, multiple nested wells, available in many commercial CMOS processes, allow to implement full CMOS electronics inside the pixel (see Section 2), and therefore fast readout architectures like hybrid pixels are possible, beyond the rolling shutter readout traditionally used in MAPS.

As a part of the CMOS program for the future ATLAS Inner Tracker (ITk), DMAPS integrating fast readout architectures are under development. They may serve as a high performance and cost effective option for the outer pixel layers of ITk, replacing the complex and expensive hybrid pixel modules. This work presents two DMAPS prototypes, i.e. LF-MonoPix and TJ-MonoPix. Both of them use a column based readout architecture named column drain readout, similar to the one used in the current ATLAS pixel detector [9]. The LF-MonoPix was designed and fabricated in the LFoundry 150 nm CMOS technology, featuring a large charge collection electrode, usually preferred for high radiation tolerance. In contrast, a small sensing node is used in TJ-MonoPix, where a fully depleted sensitive layer can be expected by profiting from a modified process in the TowerJazz 180 nm CMOS imaging technology [10]. The two different sensor concepts will be described in Section 2, followed by an overview of the chip design in Section 3. In Section 4, first measurement results for LF-MonoPix will be shown. Section 5 will summarize the work.

2 Sensor concepts

The implementation of a depleted CMOS pixel cell can be generally categorized by the fill factor, i.e. the ratio of the sensing electrode area to the total pixel area [11]. Both large and small fill factor approaches are pursued in this work and implemented as described in the following.

LF-MonoPix Figure 1(a) shows the cross section view of a pixel cell in LF-MonoPix. The sensing volume is a high resistivity P-substrate (> 2 kΩ·cm). The charge collection node is formed by a very deep N-well, which encloses the in-pixel electronics. Full CMOS circuitry is possible because of the isolation between the N-well, hosting the PMOS transistors, and the charge collection N-well, by a deep P-well. High charge collection efficiency after radiation damage can be expected from a large charge collection electrode, together with the possibility of applying back-side reverse bias to achieve more uniform drift field. Measurement of a previous prototype shows that a depletion depth over 100 μm is achievable with such sensor design after particle fluence of 10^{15} n_{eq}/cm^2 [12], the expected NIEL radiation fluence for the ITk outer pixel layers. However, it may suffer from large detector capacitance, e.g. ~ 400 fF, especially when complex in-pixel logic is needed to implement a fast readout architecture [11, 13]. The large detector capacitance will slow down the pre-amplifier and increase the noise, which can only be compensated by increasing the power. Moreover, such sensors are sensitive to the cross talk introduced by the in-pixel electronics to the sensing node, and many design efforts are required to mitigate this issue [13].



(a) (b)

Figure 1. Cross section view of one pixel cell implemented (a) in the LFoundry 150 nm CMOS technology featuring a large charge collection electrode and (b) in the TowerJazz 180 nm CMOS technology featuring a small sensing node.

TJ-MonoPix As depicted in Figure 1(b), TJ-MonoPix uses a high-resistivity (> 1 kΩ·cm) P-type epitaxial layer as the sensitive layer, located on top of a highly P-doped wafer substrate. The typical thickness of the epitaxial layer is between 18 μm and 40 μm. The charge collection electrode is created by a small N-well (e.g. several μm^2). The deep P-well is used to shield the N-wells that host the PMOS transistors, which would otherwise work as competing charge collection nodes. The main motivation of using a small sensing diode is its very small detector capacitance (e.g. < 5 fF), which allows to minimize the analog power consumption with given analog performance [14]. The use of small collection node in high radiation environment is also encouraged by recent R&D progress to improve the sensor depletion by using a modified process [10]. Despite the small charge

collection electrode, a test chip called Investigator, fabricated with the modified process, showed uniform efficiency for 25 μm and 30 μm square pixels, even after fluence of 10^{15} n_{eq}/cm^2 [8].

3 Chip overview

LF-MonoPix is the first fully monolithic prototype of a DMAPS series implemented in the LFoundry technology [15, 16]. Its design has significant inputs from its ancestor LF-CPIX [16], e.g. pre-amplifier, guard ring structure, chip floor plan. DMAPS development in the TowerJazz technology follows the successful experience of the ALPIDE chip for the ALICE-ITS upgrade [2]. The TJ-MonoPix is part of the TowerJazz DMAPS R&D, aimed to translate the well understood column drain architecture, based on the experience of LF-MonoPix, into the TowerJazz sensor design with small charge collection node. The two chips are large scale demonstrator chips. Some main parameters for these designs are listed in Table 1.

Table 1. Main parameters of LF-MonoPix and TJ-MonoPix.

Parameter	LF-MonoPix	TJ-MonoPix
CMOS tech.	LFoundry 150 nm	TowerJazz 180 nm
Sensor concept	Large fill factor	Small fill factor
Chip size	$\sim 1 \times 1$ cm^2	$\sim 1 \times 2$ cm^2
Pixel pitch	50×250 μm^2	36×40 μm^2
Pixel matrix	129×36	224×448
Static current/pixel	~ 20 μA	< 1 μA
Output data link	$1 \times$ LVDS@160 MHz	$4 \times$ CMOS@40 MHz

3.1 Architecture

Though having different layout floor plans, both LF-MonoPix and TJ-MonoPix follow the same architecture as depicted in Figure 2.

The readout chain starts with the pixel front-end (FE) circuit, i.e. the pre-amplifier and the discriminator. The discriminator fires when the analog signal pulse crosses its threshold, and the output holds until the analog pulse falls below the threshold. Coarse analog information can be obtained by measuring the width of the digital pulse at the discriminator output, a technique called time over threshold (ToT). Two gray encoded time stamps, corresponding to the leading edge (LE) and trailing edge (TE) of the discriminator output, are written into the two in-pixel RAM cells to record the hit time and pulse width. The pixel readout is arbitrated by a token propagation, with the topmost pixel having the highest readout priority. The pixel column interfaces with the End-of-Column (EoC) circuitry, which includes the gray counter running at 40 MHz to generate the time stamp, the sense amplifiers to receive the column data, and the EoC logic to perform the column-level readout priority scan and transmit data to the serial link. In these first prototypes, for design simplicity, the readout controller, which controls the readout sequence, is implemented in an FPGA. Triggering buffers are not included either, hence all the hit data is transmitted through the serial link off chip.

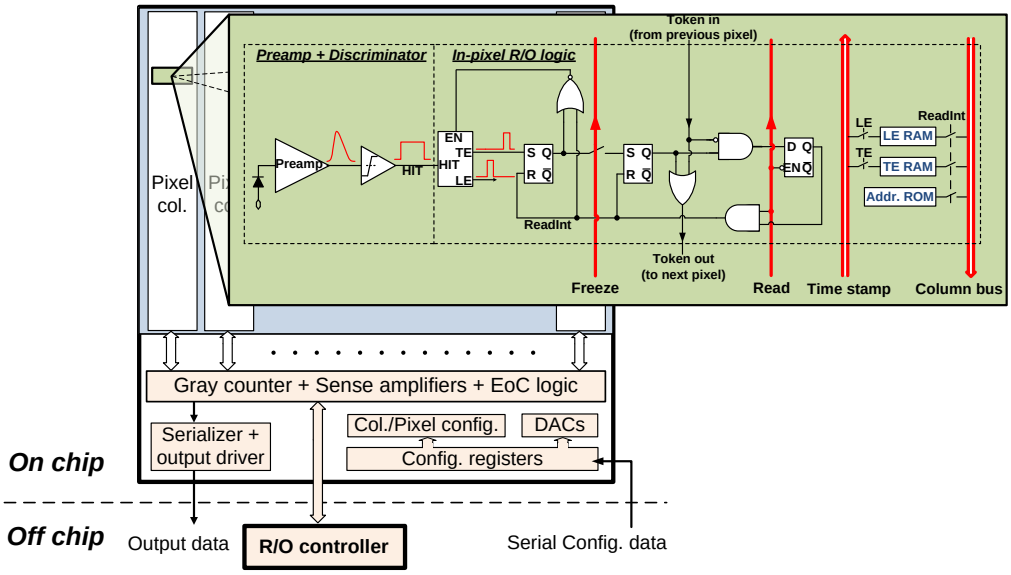


Figure 2. The chip architecture of the two prototypes in this work.

It is noted that a second readout concept was implemented in LF-MonoPix, where the pixel contains only the FE circuit. The digital block is placed at the column end, with one to one connection to the corresponding pixel. This was mainly motivated by reducing the potential cross talk to the sensing node introduced by the digital logic, but more complex wiring in the matrix layout was needed.

3.2 Pixel

The different sensor concepts of the two prototype chips have led to different pixel designs in terms of sensor geometry and FE circuit.

LF-MonoPix The layout of a typical pixel in LF-MonoPix is shown in Figure 3 (upper). The pixel size is 50×250 μm^2. The charge collection well is represented by the shaded area, giving a fill factor about 55%. The schematic of the FE circuit is also shown in Figure 3 (lower). The pre-amplification stage is a typical charge sensitive amplifier (CSA), AC coupled to the sensor. The signal charge is integrated on the feedback capacitor C_f. The DC feedback, mainly composed of the current mirror M1 and M2, stabilizes the operation point and continuously discharges the integrated signal. Such a DC feedback allows for high feedback resistance, regardless the discharge current which is defined by I_{FB} [17]. The output of the CSA is sent to a discriminator, whose threshold can be trimmed by a 4-bit in-pixel DAC. Thanks to the AC coupling between the CSA and discriminator, the baseline of the discriminator input is set to V_{BL} via the MOS resistor M3, independent on the DC level of the CSA. The biasing of M3 is set globally by an on-chip current DAC adjusting the current I_{BL}.

TJ-MonoPix The layout of 4 neighboring pixels in TJ-MonoPix is shown in Figure 4 (left). Each pixel has an area of 36×40 μm^2. The charge collection well is located in the center of the pixel, and it has an octagon shape with a diameter of 2 μm. The spacing between the charge collection

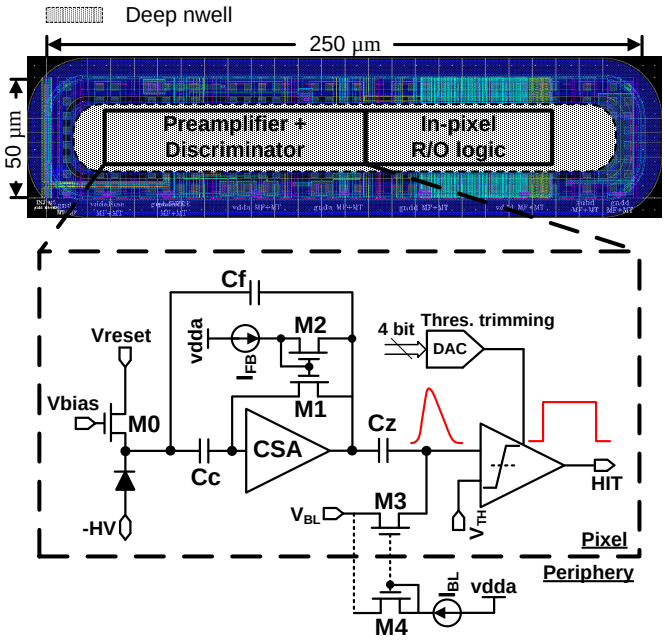


Figure 3. Layout of a typical pixel cell in LF-MonoPix (upper) and schematic of its FE circuit (lower).

node and its nearest P-well is 3 μm (refer to Figure 1(b)). The estimated detector capacitance is less than 5 fF, almost two orders of magnitude smaller than LF-MonoPix. The small detector capacitance allows the use of a very compact and low power FE circuit derived from the ALPIDE chip [18], the schematic of which is sketched in Figure 4 (right). The signal charge is integrated on the capacitance of the input node PIX_IN. It is noted that the low capacitance leads to large voltage excursion at the input node. The resulting voltage signal is then amplified and shaped by the FE circuit, generating a voltage pulse at the node $OUTA$. The charge-to-voltage conversion gain seen at $OUTA$ can be as high as several mV/e$^-$. Such a high gain makes it possible to use a simple inverting stage (M6 - M8 in Figure 4) as the discriminator without threshold trimming.

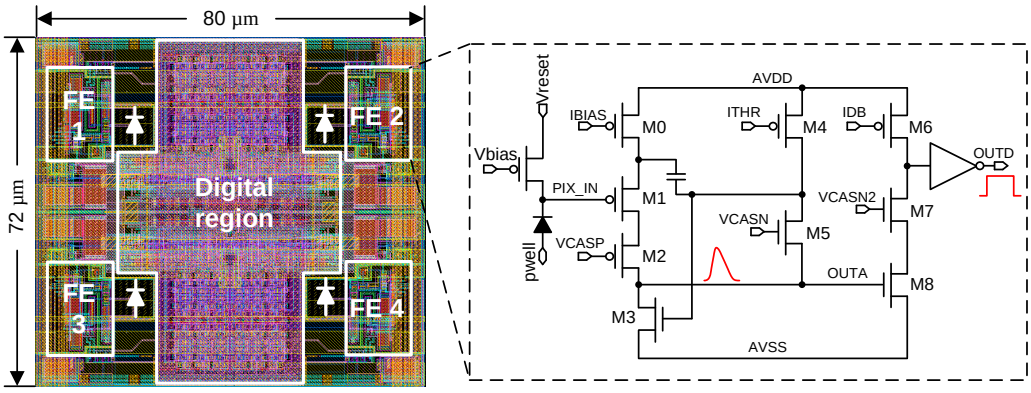


Figure 4. Layout of four neighboring pixels (left) and schematic of the FE circuit (right) of TJ-MonoPix.

4 First results for LF-MonoPix

The LF-MonoPix wafers were back from the foundry in March 2017, and the chip is fully functional. Extensive characterization is currently in progress, both in lab and in beams. This section shows some first laboratory measurement results.

I-V curve The sensor depletion can be enhanced by a high bias voltage. The highest voltage that can be applied is limited by the sensor breakdown behavior. Therefore, the sensor leakage current was measured as a function of reverse bias voltage. Figure 5 shows the I-V curve of LF-MonoPix measured at room temperature. The breakdown was measured at -280 V, an improvement over previous chip generation in the same technology [15], thanks to a new guard ring structure [16]. Such high breakdown voltage is likely to ensure a sufficient depletion after irradiation [7, 12].

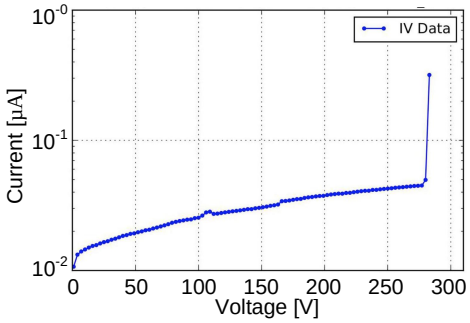


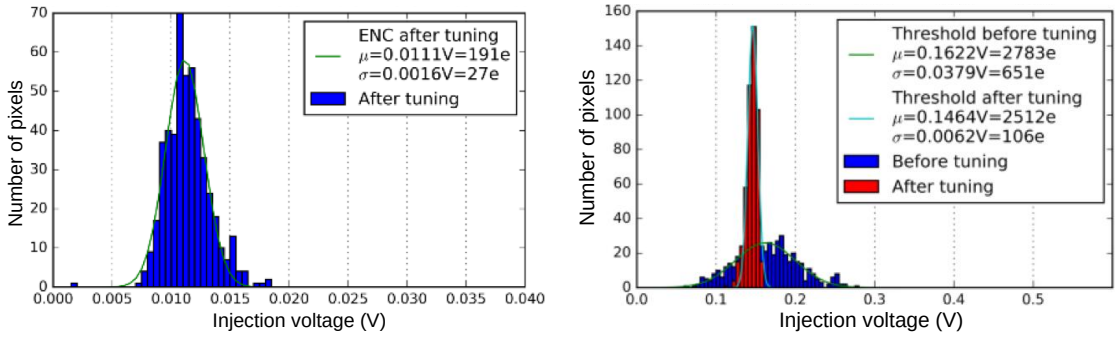
Figure 5. I-V curve of LF-MonoPix measured at room temperature. The voltage value refers to the reverse bias voltage.

Noise and threshold distribution The noise performance and threshold distribution were studied by scanning an external injection voltage and recording the sensor response. The injected signal was calibrated by an ^{241}Am radioactive source and X-ray fluoresce of Terbium. Figure 6 shows the noise and threshold distribution of four pixel columns, composed of one pixel variant with full in-pixel readout logic. Its pre-amplifier has complementary input transistors as described in [16]. The average noise value is 191 e^-, with dispersion of 27 e^-. The threshold was tuned to around 2500 e^-, and the dispersion is about 100 e^-. It is noted that the threshold shown here should not be regarded as the minimum operation threshold. A lower value may be achieved by improving the tuning algorithm. Systematic study on the performance of different pixel variants is still ongoing, which will allow us to choose the best design in terms of pre-amplifier, discriminator, layout scheme and readout concept.

5 Summary

Two large scale DMAPS prototypes are presented in this work, both having the column drain readout electronics integrated on the sensor substrate. The goal is to demonstrate the feasibility of using fully monolithic CMOS pixels in the outer pixel layers of the future ATLAS ITk.

The LF-MonoPix, fabricated in the LFoundry 150 nm CMOS technology, employs the large fill factor sensor concept, as a safe choice for radiation hardness. Preliminary test results on the



(a) (b)

Figure 6. (a) Noise distribution and (b) Threshold distribution before (blue) and after (red) tuning for one pixel variant with full in-pixel readout logic and using a CMOS input pre-amplifier.

LF-MonoPix IC (Integrated Circuit) show that the chip is fully functional with a high break down voltage of -280 V. First measurement of one pixel variant having full in-pixel digital logic showed a tunable threshold of ~ 2500 e^- and a noise value of ~ 200 e^-, which are comparable to the current ATLAS pixel detector [19]. Two test beam campaigns have been recently performed, one using the electron beam at ELSA (University of Bonn), the other with pions at CERN SPS. The efficiency and timing analysis are ongoing. Chip samples irradiated with neutrons and protons, with dose levels up to 2×10^{15} n_{eq}/cm^2 and 150 MRad respectively, will also be characterized to study the irradiation performance.

The TJ-MonoPix, which has been recently submitted, is implemented in the TowerJazz 180 nm CMOS technology. By using a novel modified process, full depletion in the sensitive layer can be expected even with a small sensing electrode. Its small detector capacitance brings the benefits of low power (< 2 μW/pixel) and small pixel (< 50 μm $\times$ 50 μm). The TJ-MonoPix demonstrator is expected to be back from the foundry at the end of 2017.

Acknowledgments

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