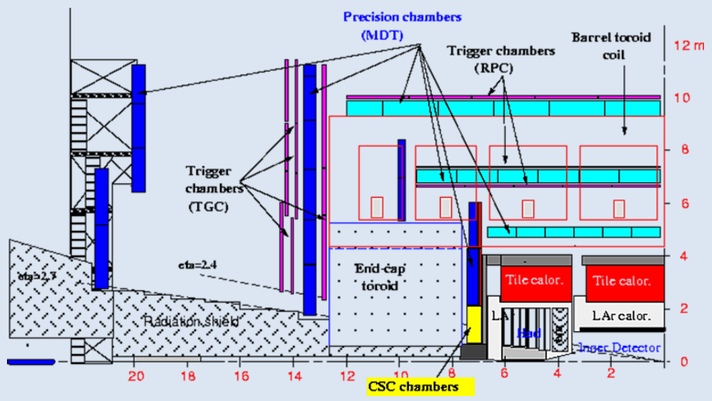
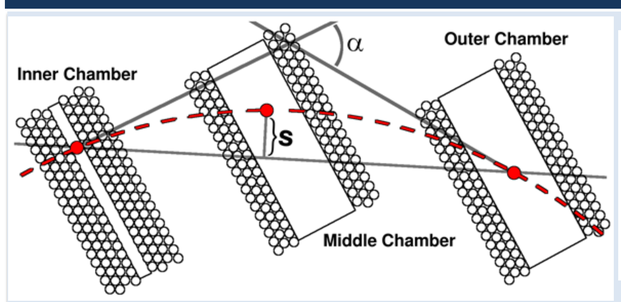
Upgrade of the ATLAS Monitored Drift Tube (MDT) Electronics for the HL-LHC

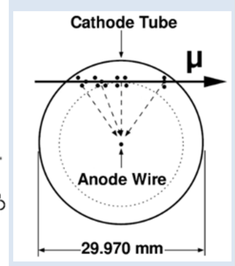
Background



- The ATLAS muon spectrometer is composed of precision tracking and trigger chambers.
- Precision measurements of the muon track coordinates are provided by three stations of Monitored Drift Tube (MDT) chambers up to |η| =2.5.
- Cathode strip chambers (CSC) with higher granularity are used in the innermost station covering 2.0<|η|<2.7.
- Resistive plate chambers (RPC) located in the barrel region (|η|<1.05) and thin gap chambers (TGC) in the endcap region (1.05<|η|<2.4) are used to provide trigger information.

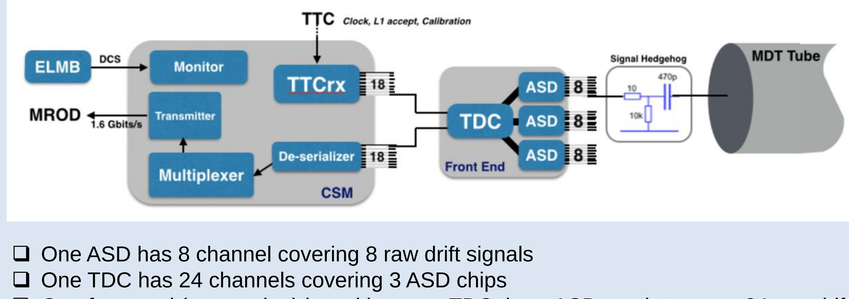
MDT detector





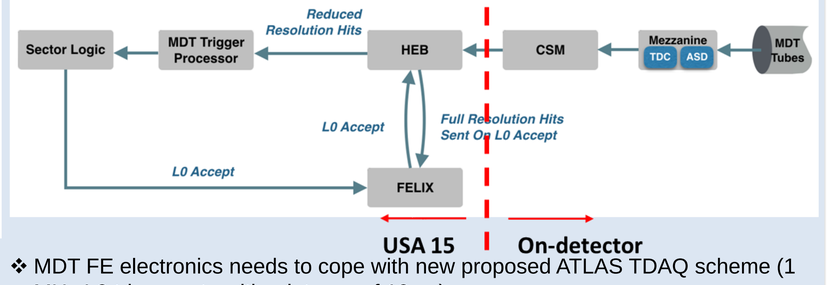
- ATLAS muon spectrometer is mainly used for muon triggering, identification and momentum measurement
- Provide a standalone momentum measurement (10% at 1 TeV), mainly by the monitored drift tube (MDT) chambers
- 1150 chambers with 354k tubes covering an area of 5500 m2
- Each tube has an inside diameter of 29.97 mm and is filled with a mixture of Ar/CO_2 (93/7) at 3 bar.
- A 50 μm gold-plated tungsten wire is positioned at the center of each tube.
- A high voltage of 3.08 kV is imposed across the tube wall and the central wire.
- Ionization created by the passage of a muon track can take up to 750 ns to reach the anode wire.

Present MDT Frontend Electronics



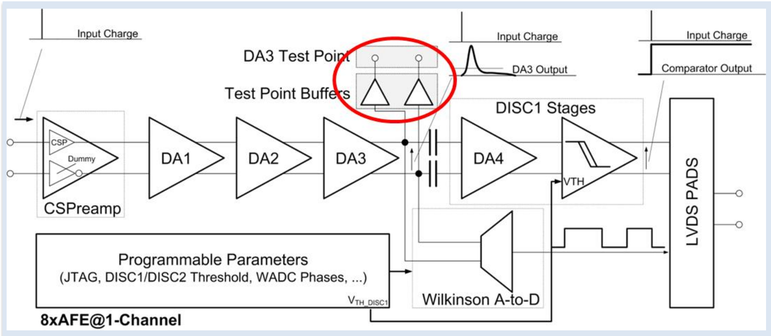
- One ASD has 8 channel covering 8 raw drift signals
- One TDC has 24 channels covering 3 ASD chips
- One front-end (mezzanine) board has one TDC three ASDs on it to cover 24 raw drift signals
- One Chamber Service Module (CSM) can cover up to 18 mezzanine boards
- CSM broadcasts the Timing, Trigger and Control(TTC) signals to the TDCs
- In CSM, the data are formatted, stored in a large de-randomizing buffer, and sent via an optical link to the MDT readout driver modules (MROD).

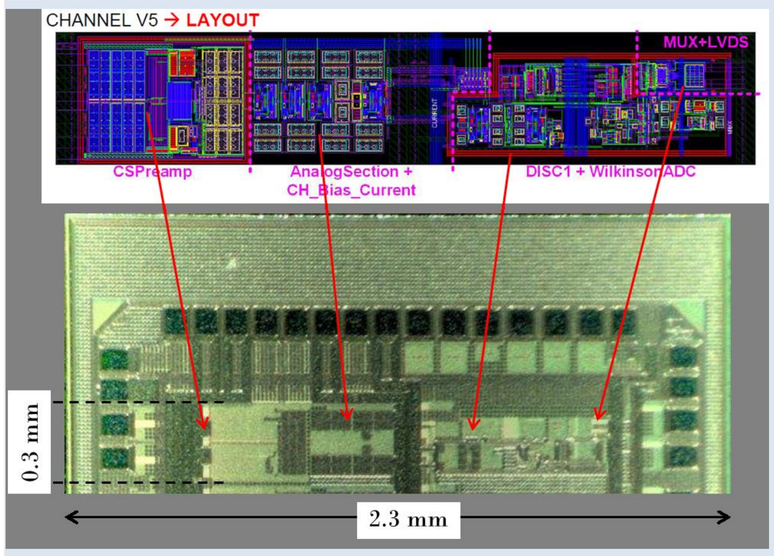
Consideration of MDT Frontend Electronics in Phase II



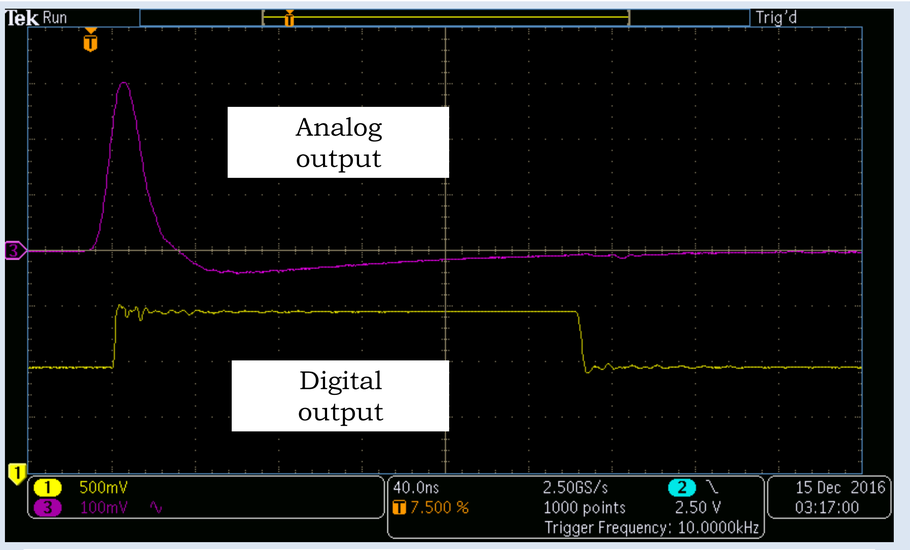
- MDT FE electronics needs to cope with new proposed ATLAS TDAQ scheme (1 MHz L0 trigger rate with a latency of 10 μs)
- The max rate current MDT readout electronics can handle : 46 kHz/tube
- Hit buffers in the current TDC chips are too small to store all hits for such a long latency time.
- MDT will be used at L0 to further sharpen the L0 trigger turn-on curve
- Radiation tolerant
- Proposed MDT electronics system:
  - Triggerless at FE and trigger matching performed at USA 15

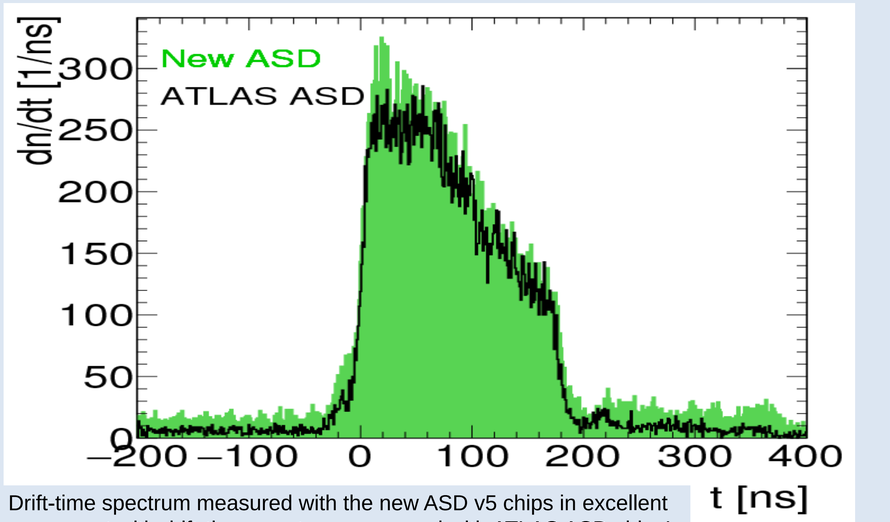
Amplifier-Shaper-Discriminator(ASD)





- Similar schematic as the present ASD (500 nm Agilent technology) but using using the GF 130 nm CMOS process
- Charge Sensing Preamplifier (CSP)->DA1->DA2->DA3(three shaping stages) -> discriminator
- The silicon area is $2.26 \times 3.38 = 7.6\ mm^2$





Drift-time spectrum measured with the new ASD v5 chips in excellent agreement with drift-time spectrum measured with ATLAS ASD chips!

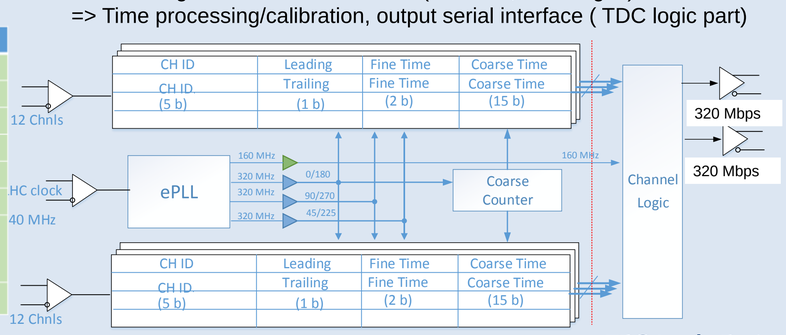
A New TDC Design

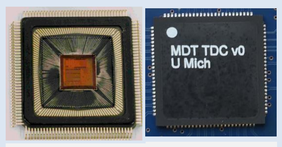
Motivation for a new TDC:
- Previous AMT is no longer available for production
- Out data band width not enough for high rate
- Issues found with the AMT chip

Develop a new TDC ASIC for the MDT phase II upgrade
- Comparable timing performance (Tubes unchanged)
- Additional features: Triggerless mode + Trigger mode

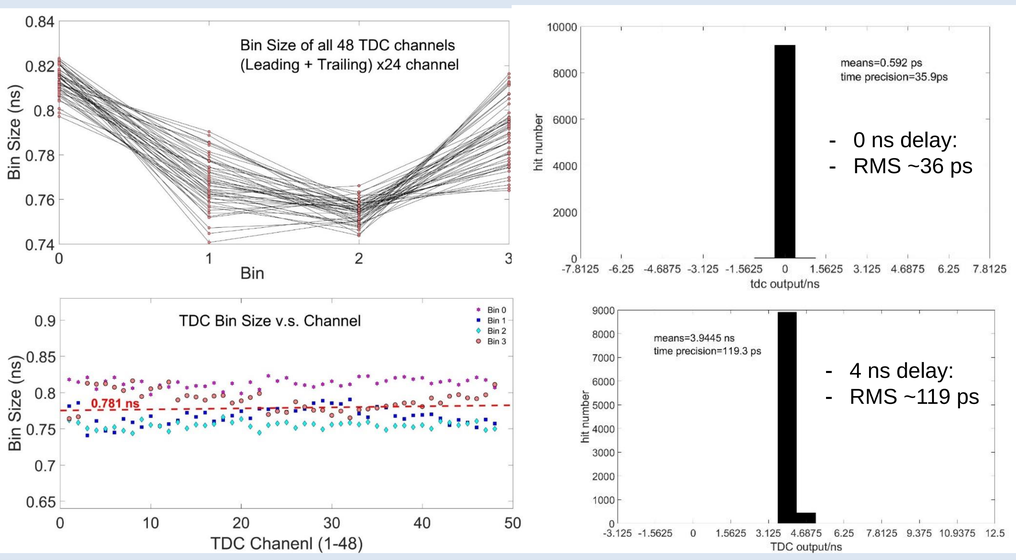
Comparison	AMT	UM-TDC
Technology	0.3 μm CMOS Toshbia	0.13 μm CMOS GF
# of channels	24	24
Resolution	0.78 ns	0.78 ns (~200 ps)
Dynamic Range	102.4 us	102.4 us
Measurement	Rising/falling/TOT	Rising/falling/TOT
Double-hit Resolution	<10 ns	~10 ns
Trigger Mode	Trigger buffer	Triggerless mode + Trigger buffer (early installation)
Output bandwidth	One 80 Mbps line	Two 320 Mbps line

- It is a demonstration prototype, with only triggerless mode.
- TDC architecture is optimized w.s.t. the timing resolustion:
  Multiple clock phases interpolator @ 320 MHz:
  4 phases of 320 MHz => 3.125 ns /4 = 0.78 ns LSB
- Main components:
  => Generation of multiple clock phases: ePLL (CERN)
  => Time Digitization: TDC channels (x24 chnl; dual edges)
  => Time processing/calibration, output serial interface (TDC logic part)





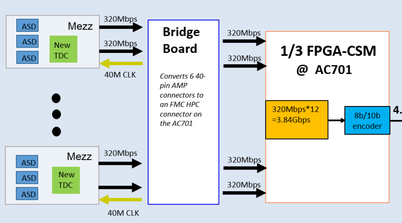
AMT3 UM-TDC v0



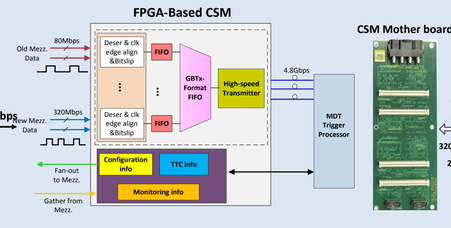
- Bin sizes for all $24 \times 2 = 48$ channels are within (0.78 ± 0.04) ns
- Integrated and differential non-linearity are less than 5% of the bin size
- Time precision: 0 ns delay, RMS ~36 ps;
- The power consumption: ~310 mW (TDC fully working).

Chamber Service Module (CSM)

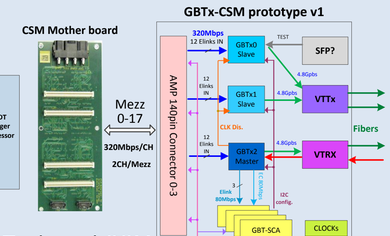
- One Chamber Service Module (CSM) must cover up to 18 new mezzanine boards
- Each new mezzanine boards have two 320Mhz data line
- CSM sends out data to USA-15 using 3 X 4.8Gbps fibers
- CSM get clock, configuration information using a fiber
- CSM sends out the mezzanine boards status like temperature, power supply using a fiber



FPGA–based CSM (a)



FPGA–based CSM (b)



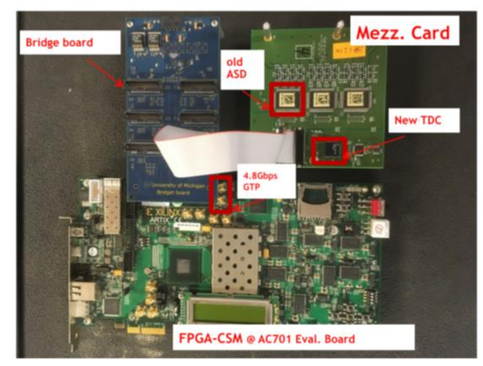
GBTx–based CSM

FPGA-based Advantages
- Flexibility
- Uniform hardware design
- Can easily handle migration from Phase I triggered mode to phase II trigger-less
- Talk with old mezzanine that cannot be replaced in Phase II

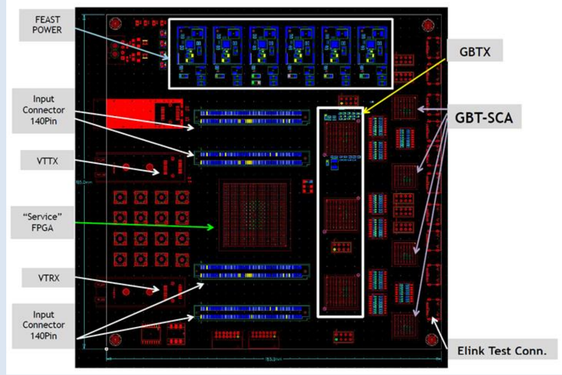
Design Complications
- Uncertainty about FPGA SEU performance in Phase II
- Maintenance needed for firmware

GBTx-based Advantages
- Low cost, low power
- radiation hard ASIC's from CERN
- No firmware design/maintenance

Design Complications
- Functionality fixed by GBTx chipset
- Small additional chip needed for JTAG distribution



FPGA-CSM in a Xilinx AC701 evaluation board



1/3 demonstrator of the GBTx-based CSM

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