A 4 x 8-Gbps VCSEL Array Driver ASIC and Integration with a Custom Array Transmitter Module for the LHC Front-end Transmission

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Abstract

This paper describes the design, fabrication and experiment results of a 4 x 8-Gbps Vertical-Cavity Surface-Emitting Laser (VCSEL) array driver ASIC with the adjustable active-shunt peaking technique and the novel balanced output structure under the Silicon-on-Sapphire (SOS) process, and a custom array optical transmitter module, featuring a compact size of 10 mm x 15 mm x 5.3 mm. Both the array driver ASIC and the module have been fully tested after integration as a complete parallel transmitter. Optical eye diagram of each channel passes the eye mask at 8 Gbps/ch with adjacent channel working simultaneously with a power consumption of 150 mW/ch. The optical transmission of Bit-Error Rate (BER) less than 10E-12 is achieved at an aggregated date rate of 4 x 8-Gbps.

Keywords: Optical detector readout concepts; Front-end electronics for detector readout; Lasers Driver ASIC; Array optical transmission

1. Introduction

VCSEL-based parallel optical data links have recently seen rapid and wide-spread deployment in high performance computing labs, data centers and Ethernet networks. The benefits include highly aggregated bandwidth, compact footprint and low power consumption. To apply the parallel optical links to the LHC upgrades as well as in other collider detector developments [1], these devices have to meet rigid environmental demands of radiation, electro-magnetic field, temperature and volume size. The high luminosity running of the LHC (HL-LHC), with instantaneous luminosities of 5×10^{34} cm^{-2} s^{-1} and an integrated luminosity of 3000 fb^{-1}, for example, will request that the opto-electronics devices are close to the beam pipe to withstand integrated radiation dose of 100KGy and 10^{15} neutrons/cm^2 [2, 3].

Two critical developments, the array driver ASIC and the array optical coupling, are indispensable towards a dedicated array optical transmitter for on-detector deployment. Prior developments on single channel optical transceivers, such as CERN's versatile link project [4], have successfully qualified commercial components, custom developed OE circuitry and assembly packages. In advancing to array-based parallel modules, limited by the channel-to-channel pitch of extremely tight industrial standard, both the array ASICs and the array optical module face new customization challenges.

A family of data link ASICs has been developed by SMU using a commercial 0.25-μm Silicon-on-Sapphire (SOS) CMOS technology [5]. The LOCld4 ASIC is a four channel, 8-Gbps/ch laser array driver designed for the array optical transmitter module. Each channel receives the low-swing Current-Mode Logic (CML) signal (200 mV differential peak-to-peak), outputs a modulation-current signal of 7.5 mA with an average current of 6.25 mA with a power consumption of 150 mW/ch at 8 Gbps/ch. This is the first VSCEL array driver ever fabricated at this aggregated bandwidth targeting high-energy physics experiments. Programmable active-shunt peaking technique is used to extend the bandwidth in pre-driving stages [6]. A novel structure of the output stage removes the ordinary extra bias-circuit, and delivers both bias and modulation current with balanced branches to effectively minimize the noise and crosstalk from the power supply.

After integrated within a custom array optical transmitter (ATx), the LOCld4 is able to be fully tested. The ATx module, while utilizing generic commercial array-optical-coupling components [7], is assembled via a custom low-cost reliable active-alignment procedure. Radiation tolerance has been tested at individual component level. The commercial VCSEL arrays (12-channel GaAs quantum well surface emitter) are being surveyed continuously with quantitative Non-Ionizing Energy Loss (NIEL) up to 10^{15} cm^{-2} 1-MeV neutrons equivalents by CERN [8]. The commercial array optical elements have been exposed to x-ray up to 96 Mrad(SiO_2) at a dose rate of 6668 Krad(SiO_2)/hr, no radiation-induced attenuation is observed [9]. The radiation tolerant performance of the SOS process has been evaluated [10], and verified on a single channel VCSEL driver with x-ray and high-energy neutron beam test [11].

The structure and design of the four-channel VCSEL Array driver LOCld4 are discussed in Section 2. The array transmitter module development and optical alignment procedures are described in Section 3. In Section 4, we discuss the full-channel optical test of the LOCld4 after integration with the ATx module. And the conclusions are presented in Section 5.

2. Four-channel VCSEL Array driver: LOCld4

The block diagram of LOCld4 is shown in Fig. 1. A common voltage (vcom) of 1.9 V is provided internally with impedance match as the input interface, followed by the pre-drivers with the 3.3 V (Vdd) power supply and the last output driver with the 3.8 V (Vvcsel) power supply. The pre-drivers are five-stage differential amplifiers with the adjustable active-shunt peaking technique for the consideration of amplification and bandwidth. The peaking strength and the tail current of pre-drivers, which mainly controls the modulation amplitude, are both adjustable through the Peaking_Adj and the Iref_pre respectively, as shown in the Fig. 1.

The last driver, receiving the differential outputs of pre-drivers, adopts the single-end, open-drain

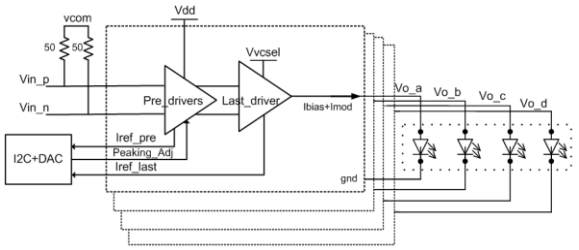


Fig. 1. Block diagram of the 4-channel array driver LOCld4

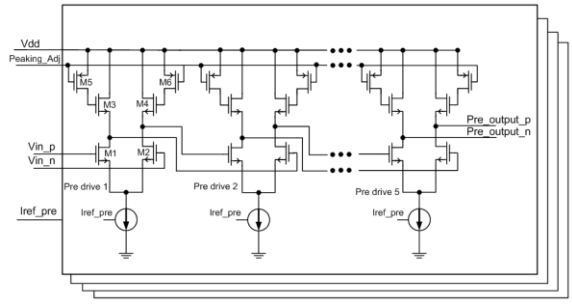


Fig. 2. Schematic of the pre-drivers in the LOCld4

structure to enable the DC coupling between the VCSEL and the driver for the array application. It combines the supply of bias and modulation current without the conventional extra bias-current circuit, and deliberately designs the load of internal branch to match with the external branch (VCSEL load). This novel "balanced" structure effectively weakens switching components on the power supply of the last driver, which minimize the ground bounce noise and crosstalk accordingly when compared to the conventional single-end output stage.

2.1. Adjustable active-shunt peaking technique in pre-driver designs

For the radiation-tolerant purpose and as a member of the data link ASIC series, the LOCld4 adopts the Silicon-on-Sapphire process. However, the bandwidth is significantly restricted by the transit frequency of this 0.25-μm CMOS process. To offset the bandwidth disadvantage, multi-stage amplification and an adjustable active-shunt peaking technique based on the regular inductance peaking are used in pre-drivers, as shown in Fig. 2. The pre-

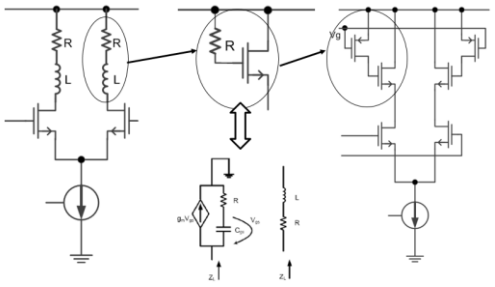


Fig. 3. (a) Passive inductance peaking, (b) Active shunt peaking (c) Adjustable active-shunt peaking used in the LOCld4

drivers of each channel consist of five DC-coupled stages with active loads. All these differential stages between different channels share the same 1.2 V (Vdd) power source within the chip.

The inductive load added to the drain, the so-called shunt peaking technique, is a conventional and widely-used way to boost the bandwidth [12]. It creates one more pole in the transmission equation of the common-source amplifier to broaden the bandwidth, as shown in Fig. 3(a). But the passive inductance generally costs a large chip area. Moreover, for the array driver application, the area of the single channel is rigidly restricted by the VCSEL Array, which has a fixed channel-to-channel interval of 250 μm. It makes the passive inductance completely unaffordable under the SOS process. The active-shunt peaking [13], as shown in Fig. 3(b), is an alternative method for the area-saving consideration. The resistor R, the capacitance between source and gate, and the V_{gs}-controlled I_{ds} consist of an active inductance with both equivalent conductive and resistive loads. Further, the resistor R in Fig. 3(b) can be substituted by a PMOS, which acts as a voltage-controlled resistor. The final structure is shown in Fig. 3(c). The PMOS gate voltage controls the value of the resistance, changes the equivalent value of the inductance, and makes the peaking strength adjustable consequently. The programmable structure enables the bandwidth optimization for each chip under applications of different bit rates, and also solves the instability problems of practical resistance value in the process.

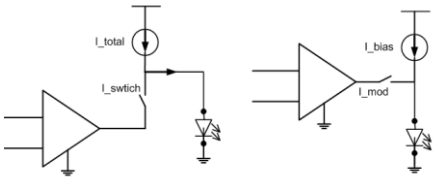


Fig. 4. Two regular structures of the last output driver in array driver design

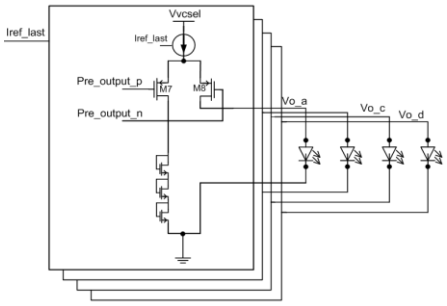


Fig. 5. Schematic of the last driver in the LOCld4

2.2. Balanced output structure in the last driver

To fit the high-density VCSEL Array, the outputs of array driver need to be directly bonded to the anode and cathode pads, and to deliver the bias and modulation current without any peripheral circuits. Fig. 4 shows two regular designs of the last output stage in an anode-driving array driver.

Fig. 5 shows the schematic of the last output driver in the LOCld4. It removes the regular extra bias current circuits, and combines the delivery of the bias and modulation current in one single branch. The PMOS M8 in Fig. 5 does not go deep into the cutoff region. Instead, it will be partially turned on to provide the bias current Ibias for the VCSEL, and completely turned on to drive the VCSEL with the current of $I_{bias} + I_{modulation}$. Besides, the load of the left branch (internal branch) is specifically designed to be balanced with the VCSEL load at the right branch: three diode-connected NMOS are used to simulate the forward voltage and serial resistance of the VCSEL. The optimum value of the left-branch load can be decided by a maximum common-mode rejection ratio (CMRR) of the last driver stage and a minimum fluctuation on the power supply (Vvcsel). The power supplies Vvcsel of four channels are separated within the chip, and connected as one with

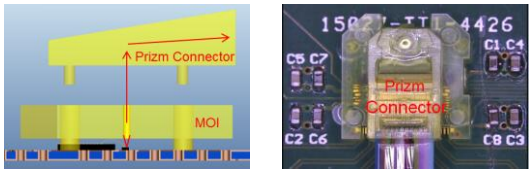


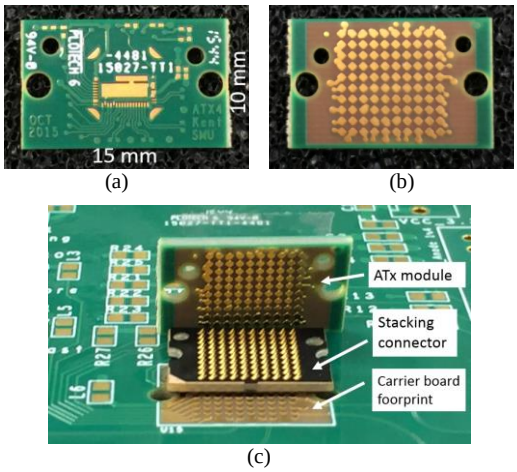
Fig. 6. Optical path diagram and photograph of assembled optical components

respective decoupling capacitors outside the chip to further suppress the crosstalk from the power.

3. Custom array optical transmitter module: ATx

Besides the array driver ASIC, the array optical transmitter module is another key component for the parallel optical data transmission, and also for the full-channel optical evaluation of the array driver. The high-density, high-precision form factor of the VCSEL array compounds the difficulty in coupling out parallel lights.

A custom array optical transmitter module (ATx) [14], utilizing commercial array optical components, i.e., mechanical optical interface (MOI) and Prizm LightTurn Connector [7], is a versatile module that can integrate different array drivers. PRIZM and LightTurn are trademarks of US Conec Ltd. The parallel lights of the VCSEL Array are focused by the MOI, redirected by 90 degrees within the Prizm Connector, and then coupled into the fiber ribbon. Fig. 6 shows the optical path through the two optical components. The Prizm Connector is pluggable over the MOI, while the MOI needs to be epoxied onto the substrate, across both the driver and VCSEL dies. The focus lens of the MOI needs to be aligned to the VCSEL apertures with a tolerance less than 10 µm. This critical process is performed by a low-cost reliable active-alignment method [9]. The main idea is to turn on the VCSEL during the alignment, and to use the coupled optical power as the guide line of the aligning. A three-dimensional micro-positioner and a horizontal rotation stage are deployed for the movement control. Under this alignment method, the coupling insertion loss of each channel, the channel-to-channel variation and the light crosstalk within the adjacent channel can be stably controlled under 3 dB,



(a) (b) (c)

Fig. 7. Electrical interface of the ATx module: (a) ATx substrate top, (b) ATx substrate bottom, (c) stacking structure

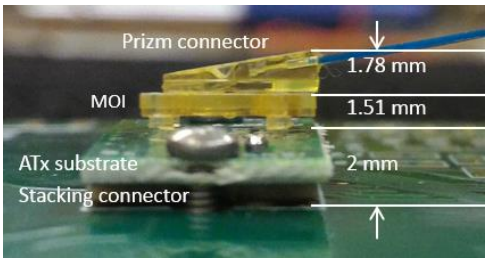


Fig. 8. Fully assembled ATx module on the carrier board

under 1 dB, and below -50 dBm respectively [9].

3.1. Electrical interface

A number of electrical interface variants have been designed for different optimization purposes. The first ATx prototype utilizes peripheral half-via structures that can be directly soldered onto carrier board. Both FR4 Print Circuited Board (PCB) and Alumina ceramic substrates have been used and both demonstrated sufficient transmission signal integrity [14]. With the latest high-speed ultra-low profile stacking connector [15], the electrical interface is updated to a pluggable version with the footprint further reduced from 19 mm x 22 mm to 10 mm x 15 mm.

Fig. 7(a) (b) shows the top and bottom sides of the

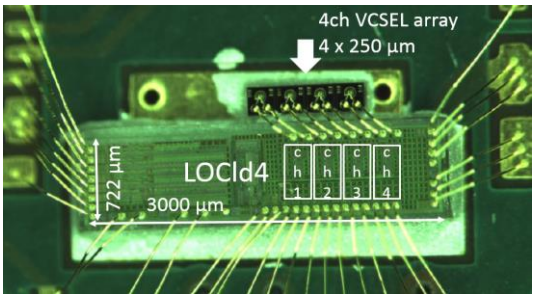


Fig. 9. LOCld4 and VCSEL array die attached and bonded

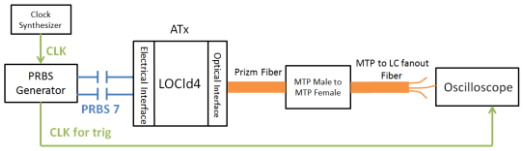
ATx substrate. The VCSEL array die and the driver die will be mounted on the top side of the substrate with the MOI assembled above. The bottom of the substrate adopts a footprint similar to the ball grid array (BGA) package with a pitch of 0.8 mm. The stacking connector, shown in Fig. 7(c), serves as a spacer between the ATx and the carrier board. Metal compression contacts are arranged at both sides of the connector to offer the top-to-bottom electrical connection. These contacts are corresponding to both the substrate footprint and the carrier board footprint. Fig. 7(c) shows the overall structure of the electrical interface.

The ATx module will be finally fixed onto the carrier board together with the stacking connector using two guide pins for positioning and two precise screws for mechanical reinforce. Fig. 8 shows a complete ATx module assembled on the carrier board. The total height of the ATx module in application is less than 5.3 mm.

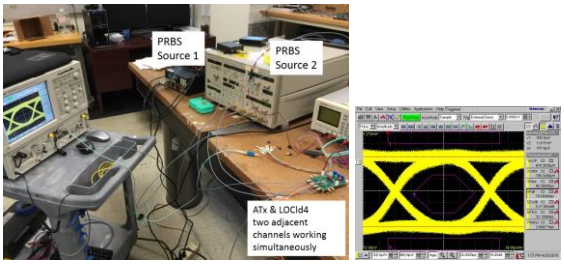
4. Full-channel optical test of the LOCld4 after integration with the ATx module

With the custom array module ATx and the active-alignment method, the array driver LOCld4 is able to be integrated within the module and fully evaluated. Fig. 9 is a photo of the LOCld4 and the 4-ch ULM 14G VCSEL array [16] dies attached and wire-bonded on the ATx substrate.

Fig. 10(a) (b) shows the block diagram and the setup picture of the optical eye diagram test. During the test, two pseudo random binary sequence (PRBS)

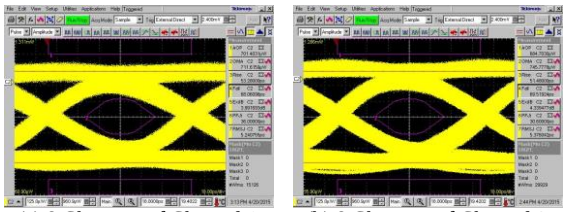


(a) Block diagram of the optical eye test

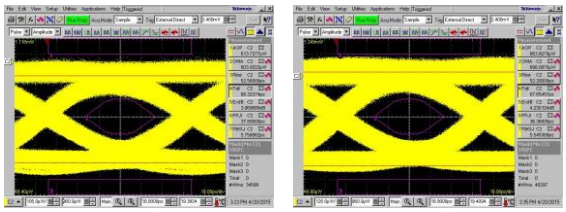


(a) Picture of the test setup (b) 5 Gbps eye diagram

Fig. 10. Optical eye diagram test setup and a 5 Gbps optical eye



(a) 8 Gbps eye of Channel 1 (b) 8 Gbps eye of Channel 2



(c) 8 Gbps eye of Channel 3 (d) 8 Gbps eye of Channel 4

Fig. 11. Optical eye diagrams of all four channels at 8 Gbps

generators were used with independent data patterns and clock sources to take into account the multi-channel crosstalk. The amplitude of the PRBS signals was set to differential peak-to-peak 200 mV. At the peaking strength of 2.2 V, an optimum 5 Gbps optical eye diagram was captured as shown in the Fig. 10(c), when adjacent channel working simultaneously at 5 Gbps.

Fig. 11 shows the optimum 8 Gpbs optical eye diagrams at a peaking strength of 2.4 V. All four channels were recorded when adjacent channel working simultaneously at 8 Gbps, and passed the eye mask test without a single violation.

Another BER link test was also conducted. The commercial SFP+ module was used as the receiver, and the LOCld4+ATx worked as the transmitter. The optical output of each channel was received by the SFP+ and verified with the PRBS 7 pattern. Every channel was tested at 5 Gbps and 8 Gbps with a total bits up to 5E12, and not a single error was found. BER less than 10E-12 was achieved at each channel at the rate of 5 Gbps and 8 Gbps when adjacent channel working at the same bit rate.

5. Conclusion

We have reported the development of a fabricated VCSEL array driver ASIC and a parallel optical transmitter module using commercial array optical components. The array driver has been integrated within the array module, and optically tested as a complete parallel optical transmitter that supports 4 x 8-Gbps data transmission. All four channels pass the optical eye-diagram mask test at the rate of 8-Gbps/ch when adjacent channel working simultaneously with a power consumption of 150 mW per channel (VCSEL power included). The BER less than 10E-12 transmission is achieved.

Acknowledgments

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