Development of Trigger and Readout Electronics for the ATLAS New Small Wheel Detector Upgrade

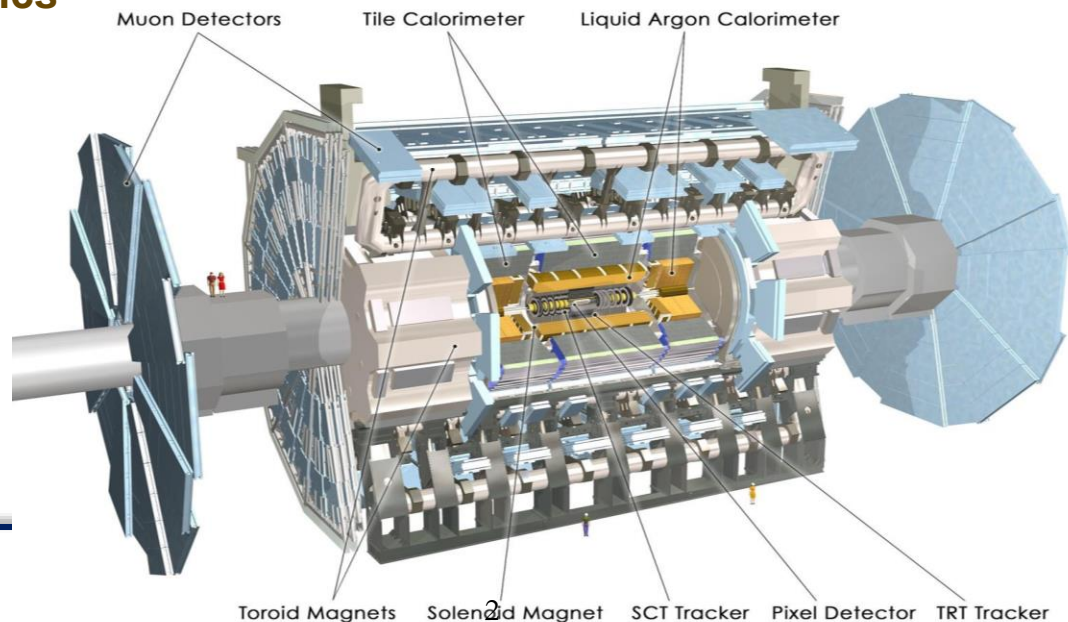**Xueye Hu**

University of Michgan

on behalf of the ATLAS Muon Collaboration

General Picture: Muon Upgrades

- **ATLAS has the world's biggest muon spectrometer and can measure muon pT with a resolution of 10% at 1 TeV**

- **Upgrades to the muon spectrometer are required to handle increased rates and fakes associated with HL-LHC luminosities (~ 7x1034 cm-2s-1)**

  - **Phase-1 Upgrade (LS2 ~ 2018): New Small Wheel**

  - **Phase-2 Upgrade (LS3 ~ 2023): Replace Tracking and Trigger Readout Electronics**

Muon Detectors   Tile Calorimeter   Liquid Argon Calorimeter

Toroid Magnets   Solenoid Magnet   SCT Tracker   Pixel Detector   TRT Tracker

Small Wheel

CSC: Cathode Strip Chambers

- *Multi-wire proportional chamber and segmented cathode strips ⊥ to wires*
- *Plane resolution ~ 60 μm ➔ Used for tracking*

MDT: Monitored Drift Tubes

- *Tube resolution < 80 μm ➔ Used for tracking*

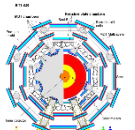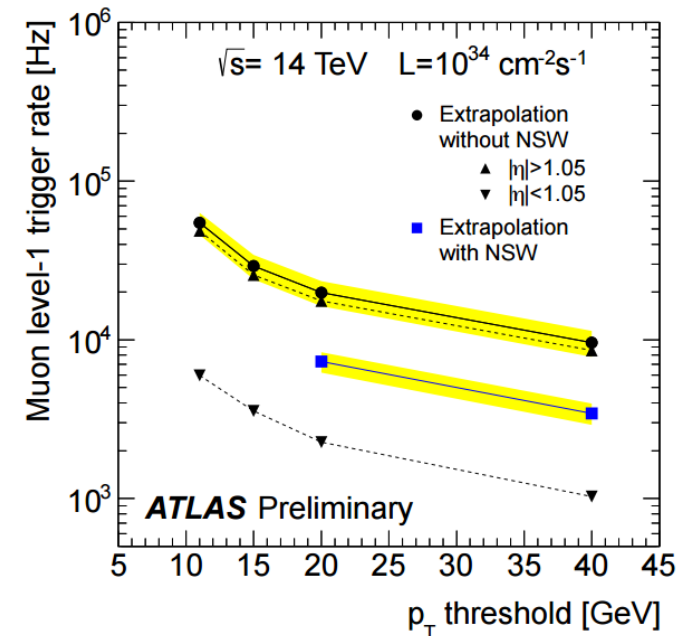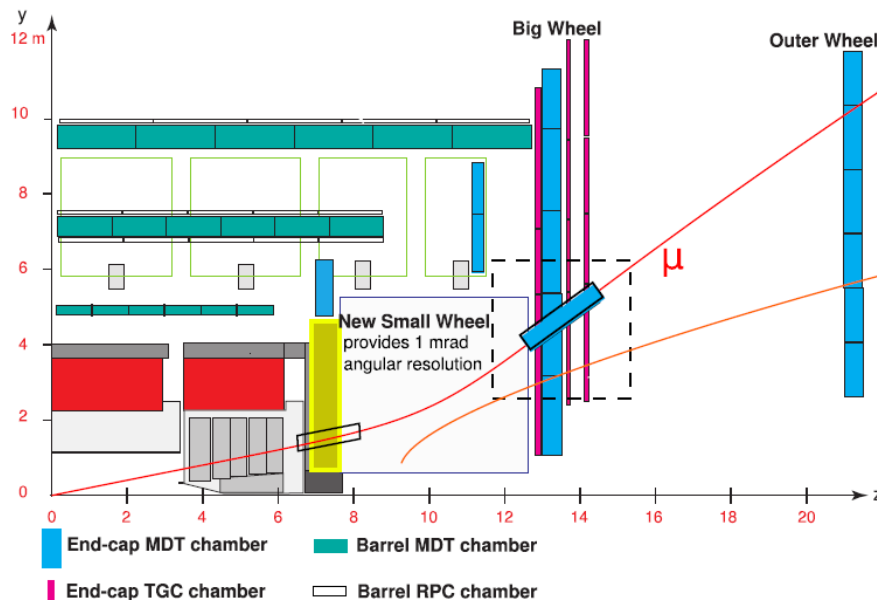## TGC: Thin Gap Chambers

- *Fast Readout ➔ Used for triggering*

- **Problems with the current spectrometer @ endcap**
  - **LV1 muon triggers rely on the BW TGC → most muons found at LV1 are fake (~90%)**
  - **Large hit rate expected at the HL-LHC → low MDT hit and track segment efficiencies**
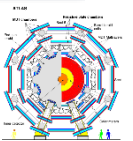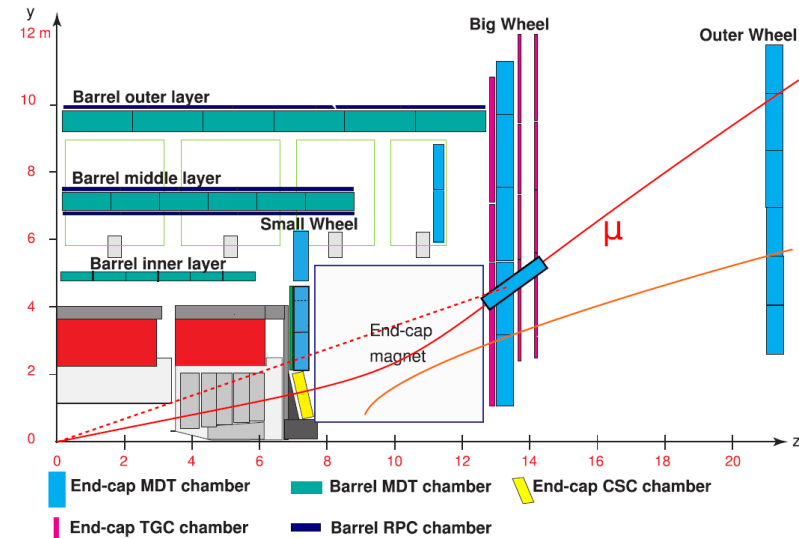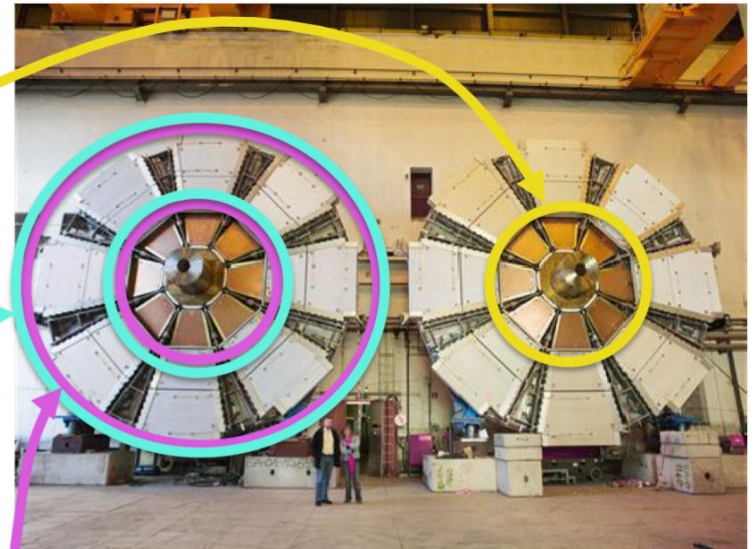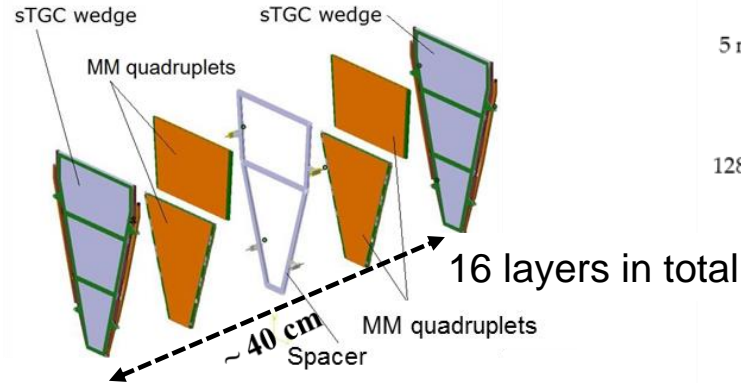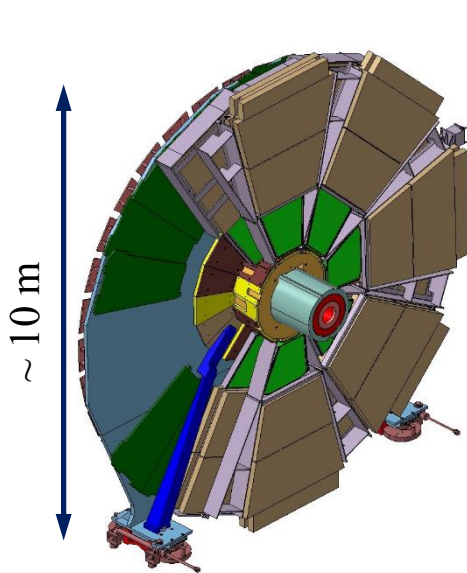
New Small Wheel

- **Replace the present SW detector with a NSW detector for the Phase-I upgrade**

  - Filter out fake tracks by reconstructing track vectors in the small wheel and match to vectors in the Big Wheel
  - Provide a segment measurement at NSW with an angular resolution of 1 mrad
  - Phase-2 Replace MDT+TGC with MM+sTGC that can work at 15 kHz/cm^2
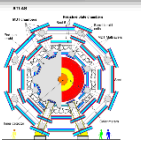
New Small Wheel Technologies

- **Micromesh Gaseous Detector, Micromegas (MM)**
- **Small-strip Thin Gap Chamber**

MM

sTGC wedge | sTGC wedge

MM quadruplets

16 layers in total

~ 40 cm

MM quadruplets

Spacer

~ 10 m

5 mm

Mesh support pillar | Resistive Strip 0.5–5 MΩ/cm

128 µm

PCB

Insulator

μ

Readout strip (0.4 mm pitch)

t

Readout channels:
- MM: ~ 2.1 M
- sTGC: 280k (strip) + 46k (pads) + 28k (wires) = 354k

~50 kW for frontend electronics

sTGC

Pad (~8 cm×8 cm)

1.4 mm

1.8 mm

1.4 mm

Resistive Cathode

Insulator (0.1 mm)

z

y

x

μ

Strip (pitch 3.2 mm)

- **Both detectors will be used for trigger and precision tracking**
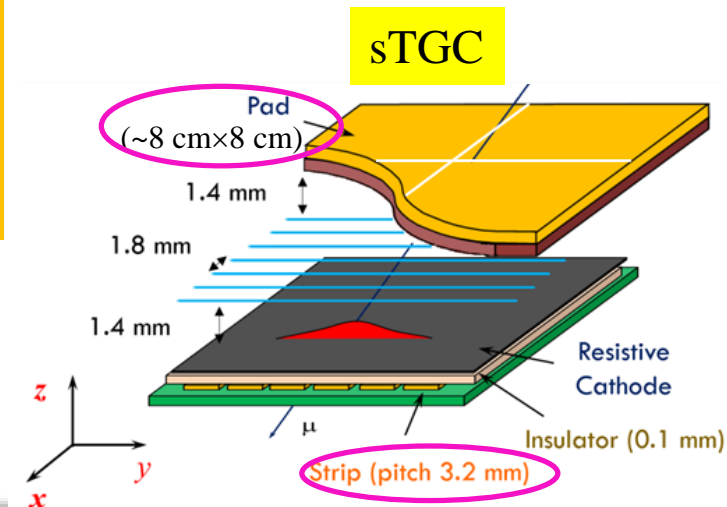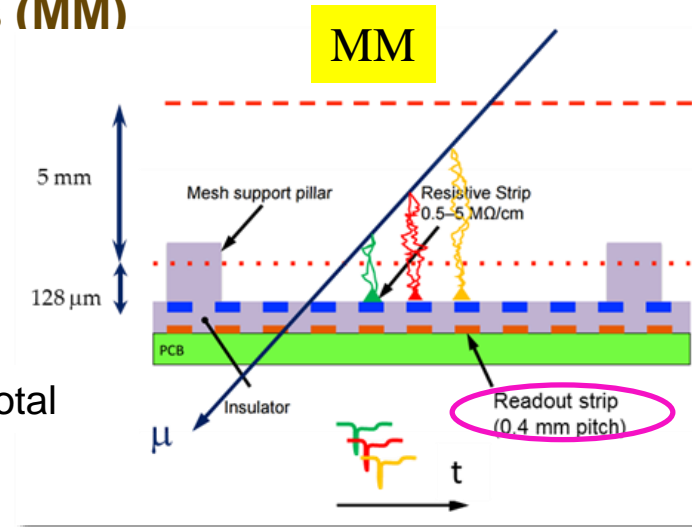
NSW Trigger and Readout Electronics

NSW Electronics Trigger & DAQ dataflow
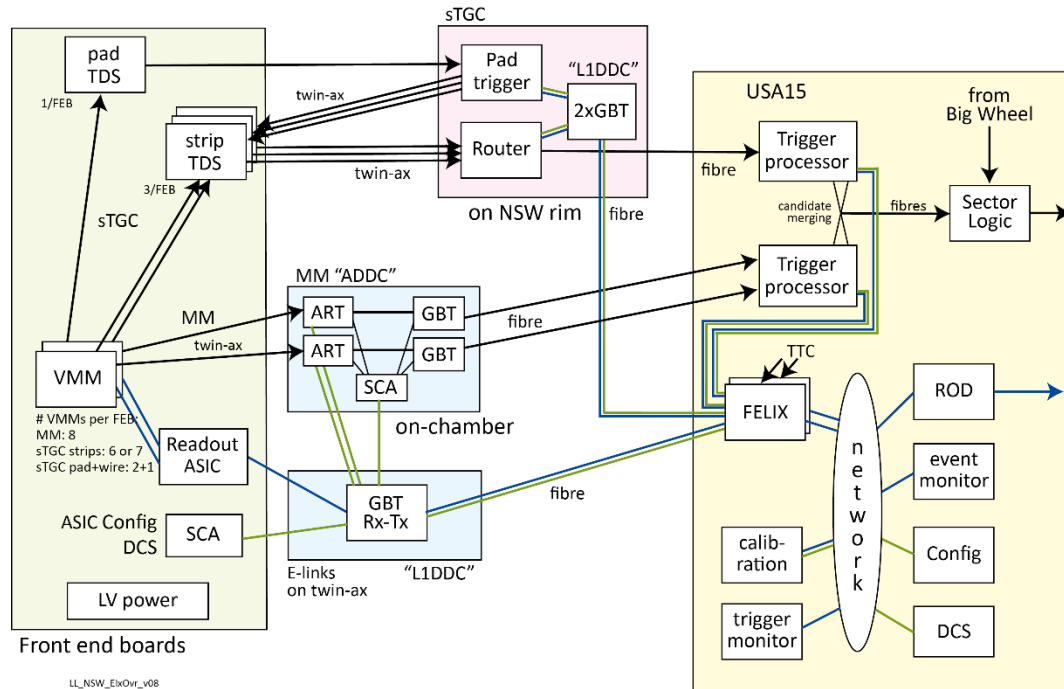
- **4 custom ASICs: VMM, ROC, TDS, ART**
- **4 custom on-detector boards: L1DDC, ADDC, MM FEB, sTGC FEB,**
- **2 custom on-rim boards: Pad Trigger, Router, Rim-L1DDC**
- **2 custom on-USA15 boards: sTGC trigger processor, MM trigger processor**

Ia. ASICs VMM

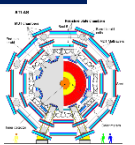**VMM provides amplification, shaping, peak height measurement and timing functionality**

- ❑ VMM2 (2014): 115mm^2, >5M MOSFETs (>80k/ch.)
- ❑ VMM3 (2015-16): 130mm^2, ~10M MOSFETs (>160k/ch.)

Channels	64
Polarity	positive/negative
Zin	50-75 ohm
Gain	0.5-16mV/Fc
Peaking Time	25-200ns
Shaper	Unipolar bipolar
TAC	60-650ns
Time Resolution	<1ns
Power	10mW/channel

Ic. ASICs TDS

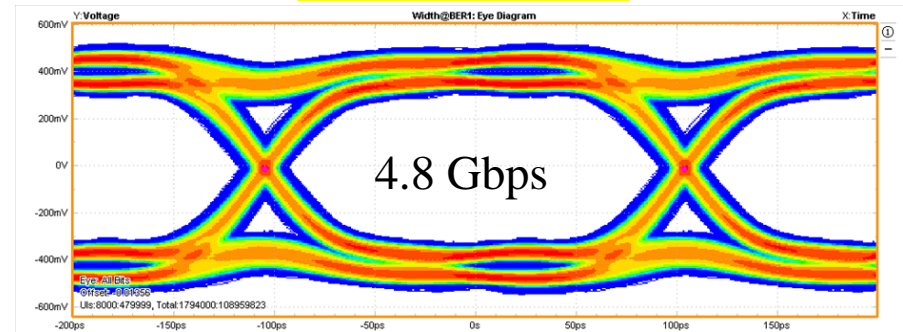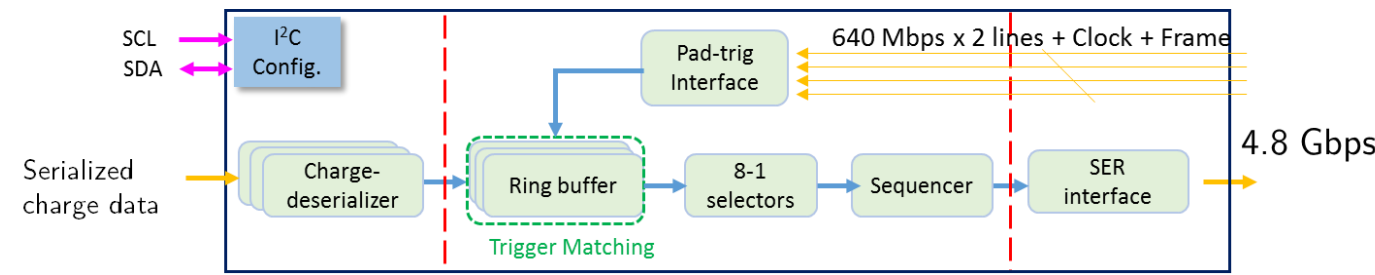- **Trigger Data Serializer**

    - **Pad-TDS: send each pad firing status to pad trigger board**
    - **Strip-TDS: prepare strip trigger data, perform pad-strip matching and serialize the charge for strips in the ROI**

TDS eye diagram

4.8 Gbps

- **Low and fixed latency needed (40 ns for pad-TDS and 75 ns for strip-TDS)**
- **Radiation tolerant**
- **128 channels with individual programmable delay (pad-mode only)**

Strip-TDS block diagram

SCL
SDA

I²C Config.

Serialized charge data

Charge-deserializer

Ring buffer

Trigger Matching

8-1 selectors

Sequencer

Pad-trig Interface

640 Mbps x 2 lines + Clock + Frame

SER interface

4.8 Gbps
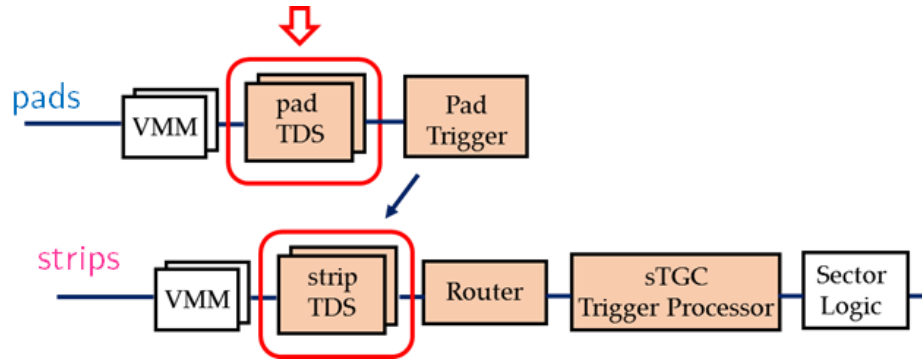
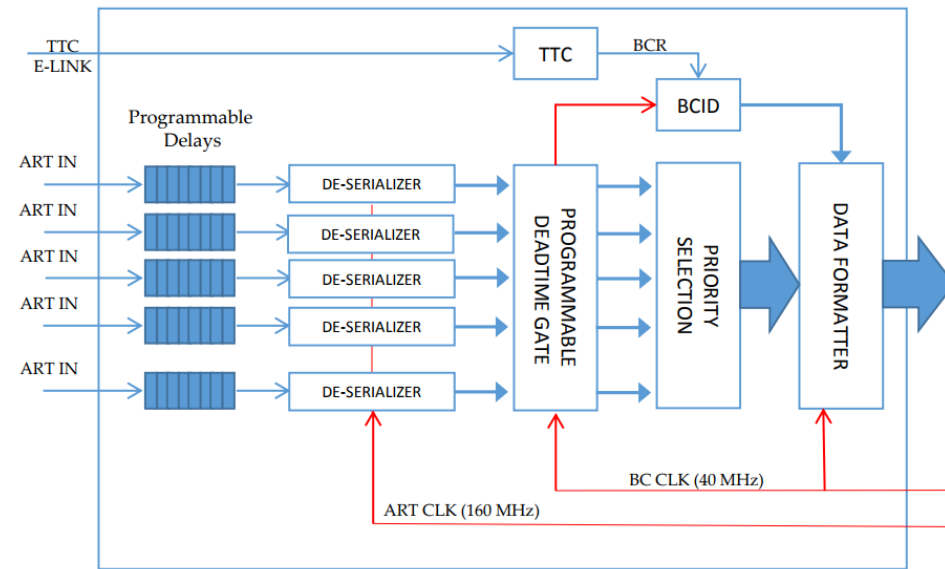1: Input interface   2: Pre-processing   3: Serialization*
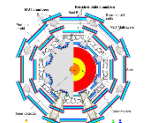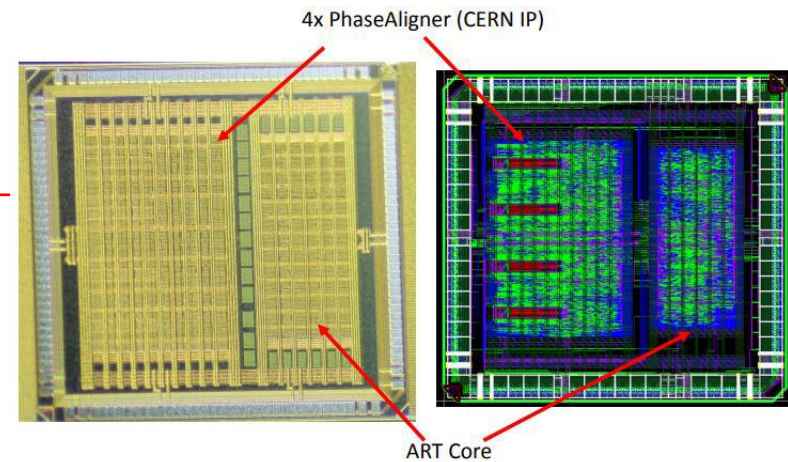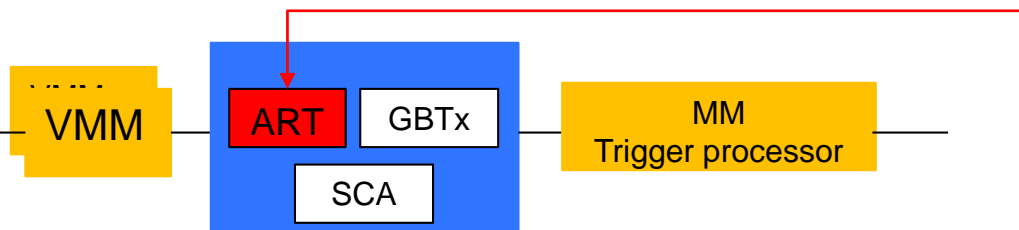
Id. ASICs ART

- **ART (Address in Real Time)**

  - Aggregates address from 32 VMMs and choses up to 8 hits to transmit
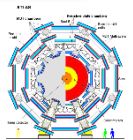 - VMM provides the address of first

- **Main Specifications:**

  - Programmable delay
  - TTC/BCID counting
  - Priority-based hit selection and data formatting

ART block diagram

ART Silicon Die

Ib. ASICs ROC

- **ROC(readout controller) responsible for the precision readout after L1A**

    - **Provide BC CLK to VMM, TDS, ART; RO CLK to VMM**
    - **Distribute control signals: L0A/VMMEN, TestPulse, BCRs**
    - **Decode 8 VMM inputs (10b/8b)**
    - **Assemble and buffer VMM packets**
    - **L1 trigger processing**
    - **Encoder new packets**
    - **Serial output: 640/320/160/80Mpbs**
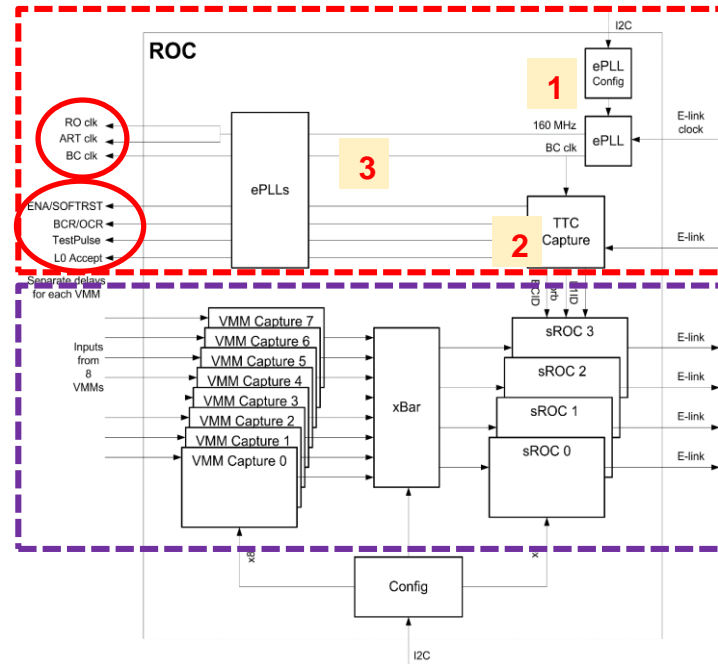
"Analog" part:
- Clocks
- Control signals

"Digital" part:
- 8 VMM inputs
- Packets processing
- 4 ROC outputs

BGA pkg. ROC

8
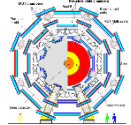
IIa. On-detector Board: FEBs

- **Front-End board will be populated with VMM, TDS, ROC ASICs. Power will be provided by FEAST, slow control will be done by GBT-SCA (CERN developed ASICs)**
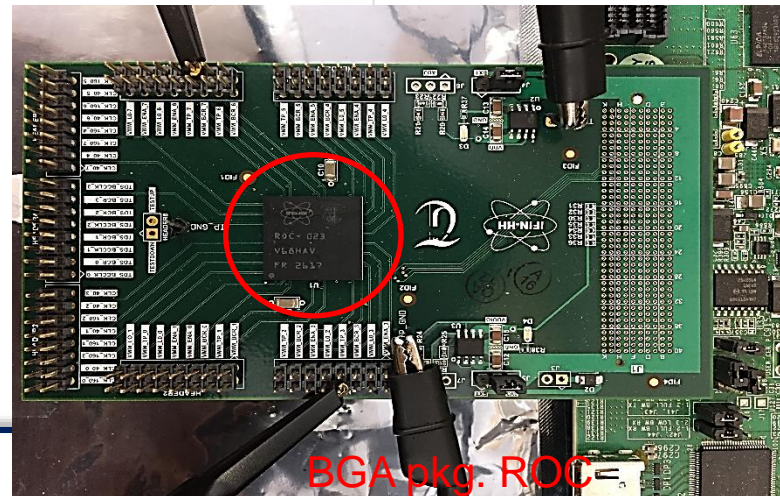
- **Two types of FEBs (pFEBs, sFEBs) for sTGC to readout wires, pads and strips. One unique type for Micromegas**

- **More than 5000 boards on NSW**

- **Layout is very challenging: need to handle large number of readout channels and deal with mixed signals (analog and fast digital up to 4.8Gbps)**

pFEB with 3* VMM3

sFEB with 8x VMM2

MMFE with 8x VMM2

IIb. On-detector Board: ADDC

- **ADDC: ART Data Driver Card**
    - Input from MMFE8
    - Two ART ASICs with 2 GBTx, 1 VTTx
    - Configuration is done by L1DDC

ADDC and Standalone Test Scheme
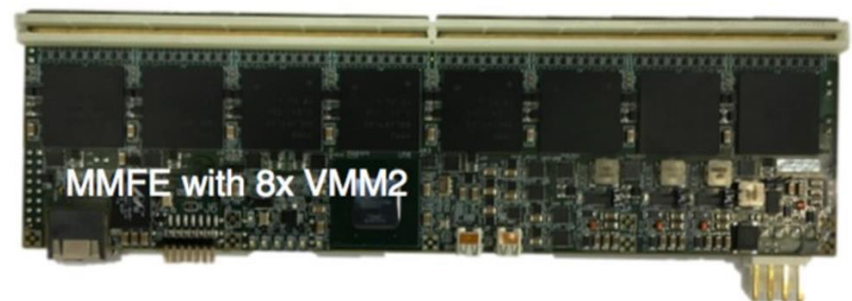
IIc. On-detector Board: L1DDC

- **L1DDC: L1 Data Driver Card**
  - **Common readout for both sTGC and MM**
  - **Aggregates and transmits L1 read from FEBs to FELIX**
  - **MM-L1DDC configuration: Using a VTTX GBTX2 and GBTX3 cannot be configured via an RX fiber. A GBT-SCA must be added-can monitor power and temperature on MM-L1DDC**
  - **sTGC-L1DDC configuration: Both GBTX can be configured by the IC channel of the GBT frame through VTRX. No GBT-SCA is needed – no monitoring**
  - **A type of L1DDC on rim: configuration and clock distribution for FEBs, sTGC Router and Pad Trigger board**
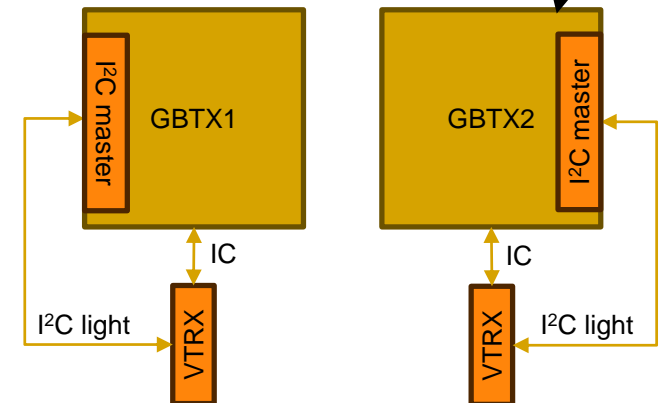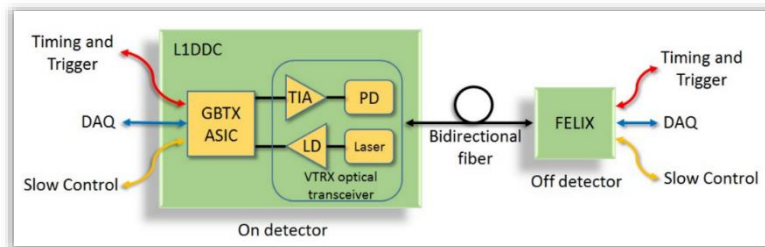
sTGC-L1DDC
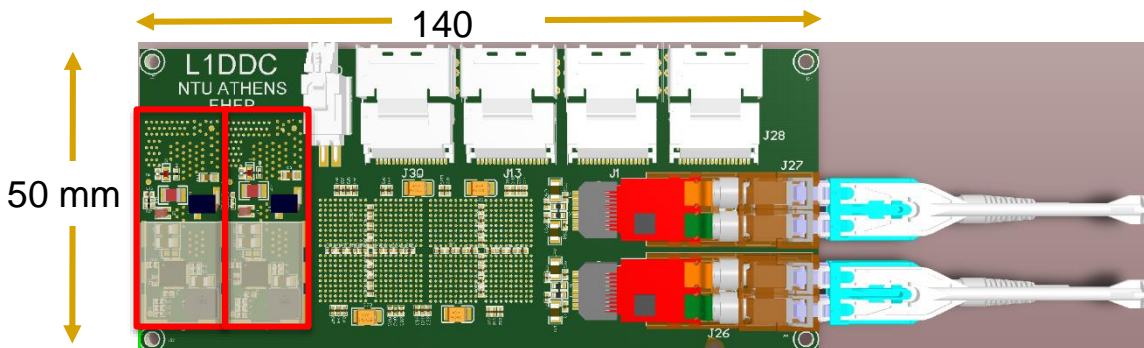
IIIa. On-rim Board: Pad Trigger

- **Pad Trigger**

    - **Receive pad firing information from all eight layers**
    - **Perform two 3-out-of-4 pad coincidences per BC to form pad trigger road (tag BCID and define strip band to be read out)**
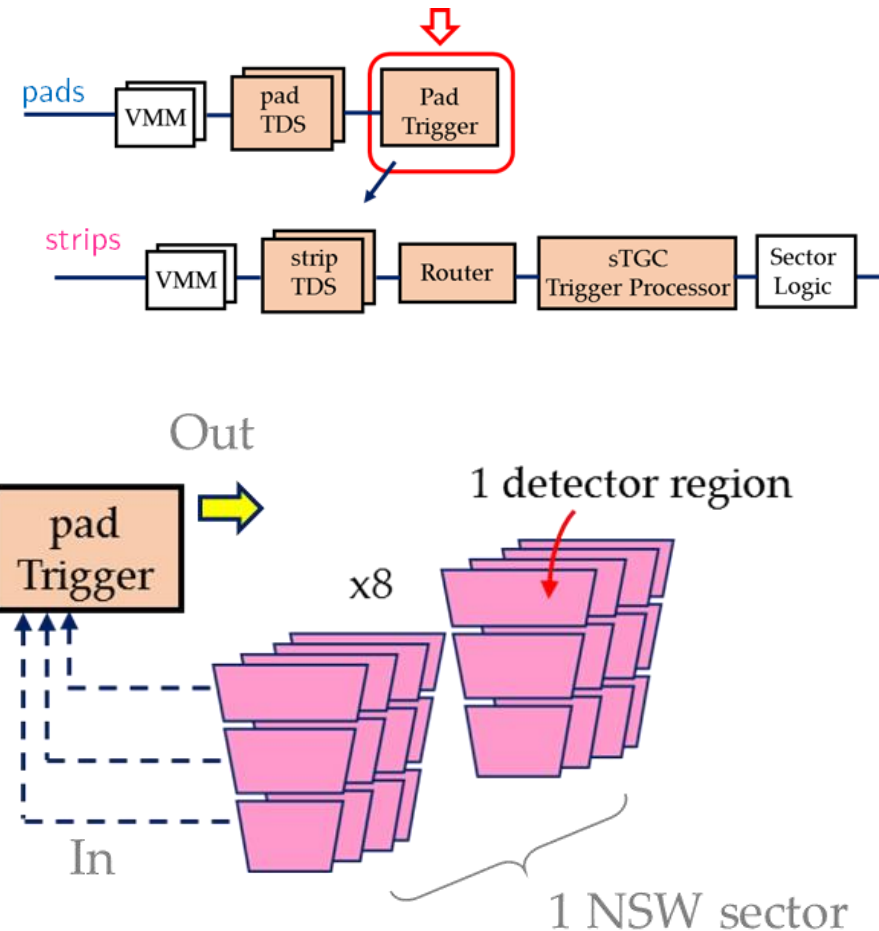   - **Send up to 3 trigger candidates (RoI) per sector per BC to strip-TDS**
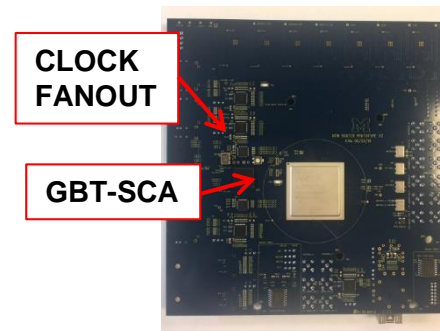   - **Send pad firing information after L1A for monitoring**

IIIb. On-rim Board: Router

- **Router**
  - Route active strip signals to trigger processor at USA15 and drop NULL packets
  - Input: 12 channels of TDS signals @4.8Gpbs
  - Output: 4 channels of optical signal to sTGC Trigger Processor
  - Low and fixed latency
  - Radiation tolerant
  - 256 routers/detector

Baseline: Artix-7

Giga-bit Input Signal conditioning

Slow control

Xilinx Artix-7 FPGA

POL DC-DC Converters

Switching Regulator

Repeater

Clock Conditioner

Back up for Data Link

Opto-TX/RX for TTC Link

JTAG   SPI Flash   Optical Mezzanine Slot for Data Link

Establish of links between TDS and router

TDS serializer chip

4m Twinax cable

MiniSAS-SMA adapter card

Router prototype

CLOCK FANOUT

GBT-SCA

FEAST

IVa. USA15 Boards: Trigger Processor

- ## Trigger Processor

  - Implement Deserializing/decoding/distribution function, BC alignment
  - Need robust, fast, FPGA-based algorithms for converting hits into high-level objects (clusters & tracks)
  - Ancillary functions: readout@L1A, monitoring, configuration…
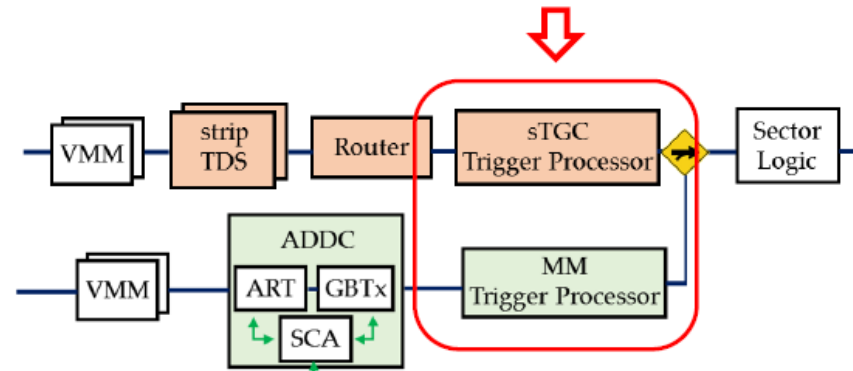
- ## sTGC Trigger Processor

  - Receive strip data from Router (32 fibers * 4.8Gbps)
  - Perform cluster centroid finding for both quadruplets and determine the segmentpointing direction
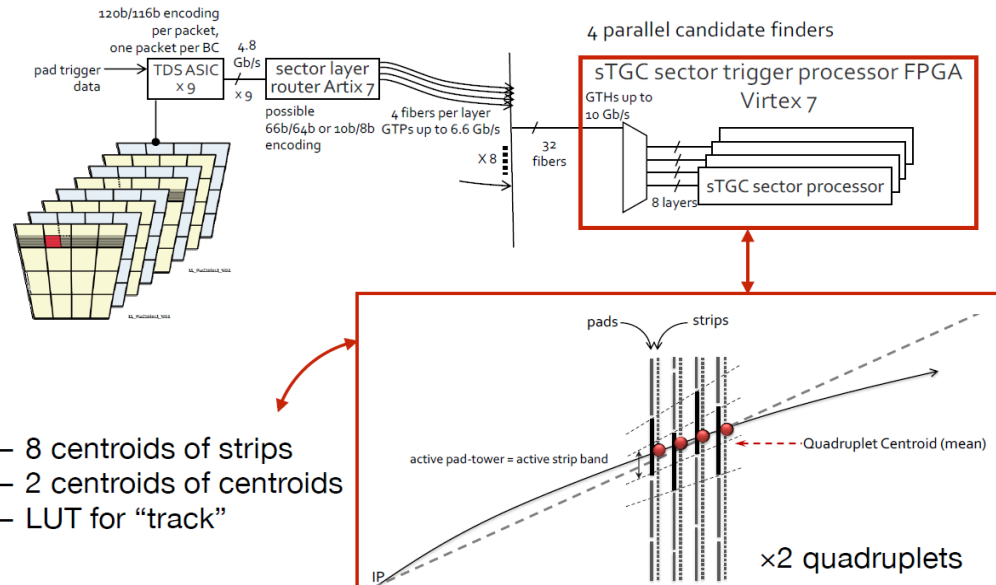
— 8 centroids of strips
— 2 centroids of centroids
— LUT for "track"

IVb. USA15 Boards: Trigger Processor

- ## MM Trigger Processor

  - **Projective roads to IP (hit→slope)**
  - **X-roads narrower, u-v (stereo) wider**
  - **A segment is multi-layer coincidence within a slope road**
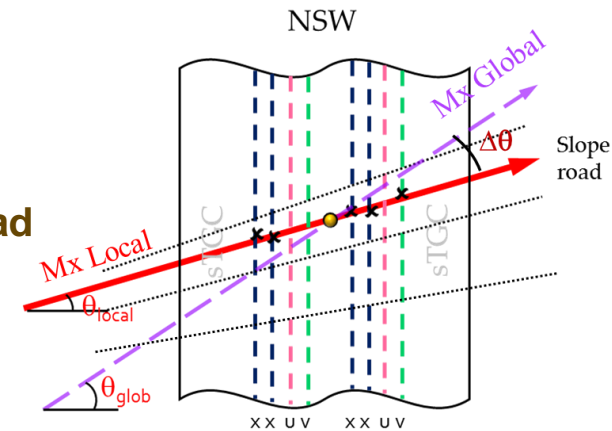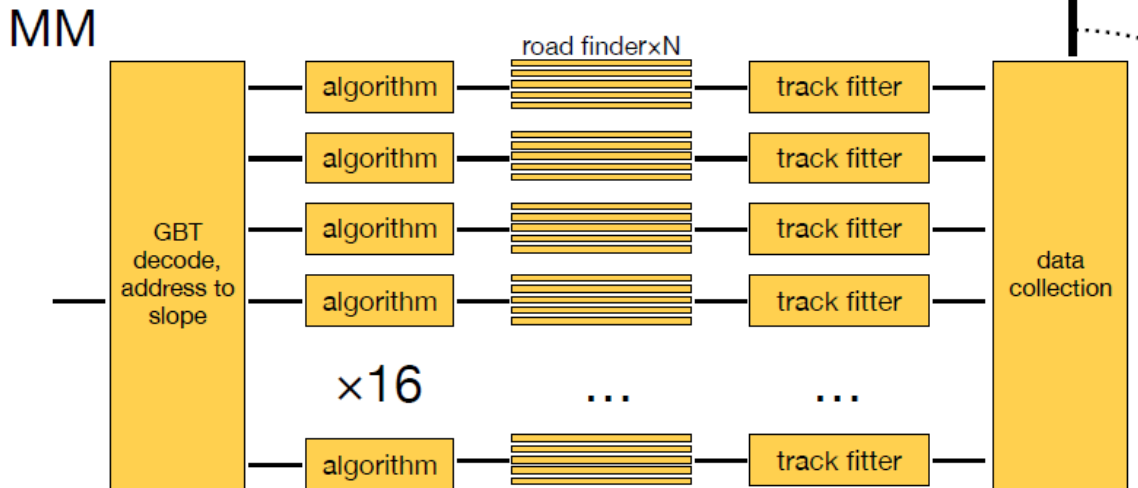
ATCA Mezzanine Card on SRS Platform
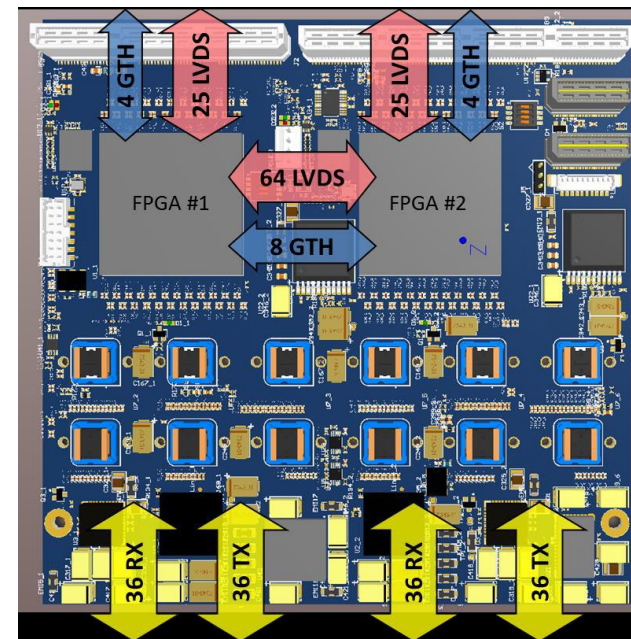
- ## MM & sTGC Trigger Processor board

  - **Implemented on FPGA-based ATCA Mezzanine Card**
  - **32 input fibers (MM/sTGC) @ 4.8Gbps**
  - **12 output fibers @ 6.4Gbps with 8b/10b encoder**
  - **1 ATCA carrier card hosts 2 Mezzanine cards (NSW sector)**

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NSW Collaboration

sTGC chambers:
Canada   Chile
China   Israel
Russia

Alignment:
Germany   Saclay
US

MM chambers:
CERN
Germany
Greece
INFN Italy
Saclay France
Dubna
Japan

Electronics:
China
Greece
Hongkong
INFN Italy
Israel
Netherlands
Rumania
Taiwan
US

Mechanics, Integration:
South Africa
….

Vertical Slice Integration Test

Project was initiated
The place was chosen

Integration Week #1
First integration week was held in August and in fact was split into two weeks, one dedicated to MM and another to sTGC. Difficult startup.
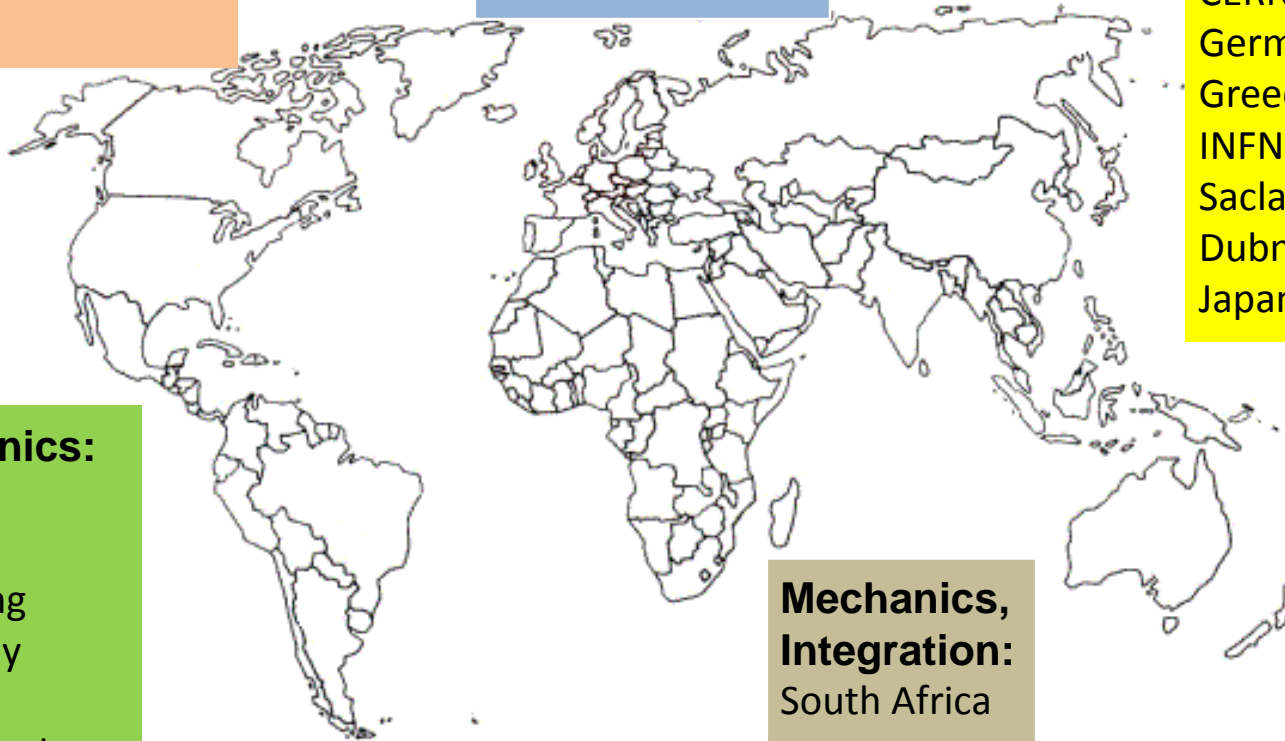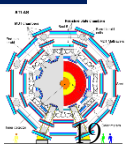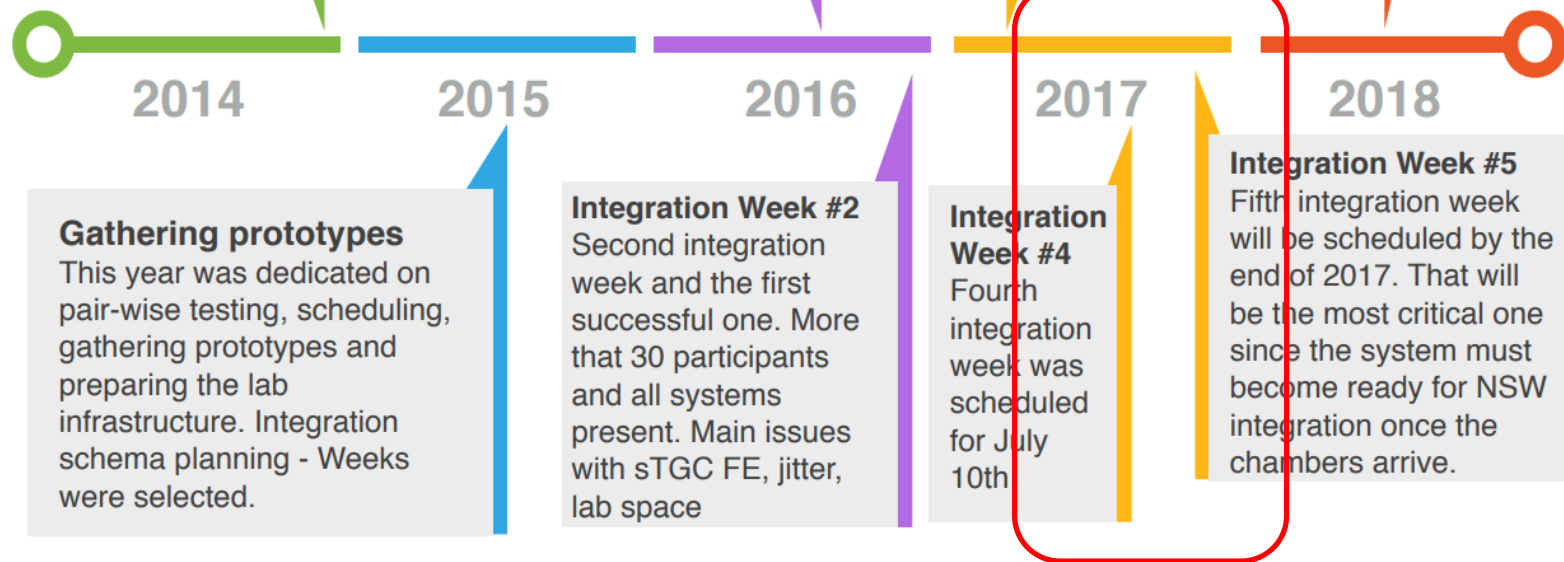
Integration Week #3
Third integration week was held in March, 30 people present and successful integration. Main issues found, jitter, SCA e-link (FELIX), sTGC FE availability, pinout

Final Integration
The last integration week will be done with final prototypes. If more weeks are needed will be scheduled.

2014   2015   2016   2017   2018

Gathering prototypes
This year was dedicated on pair-wise testing, scheduling, gathering prototypes and preparing the lab infrastructure. Integration schema planning - Weeks were selected.

Integration Week #2
Second integration week and the first successful one. More that 30 participants and all systems present. Main issues with sTGC FE, jitter, lab space

Integration Week #4
Fourth integration week was scheduled for July 10th

Integration Week #5
Fifth integration week will be scheduled by the end of 2017. That will be the most critical one since the system must become ready for NSW integration once the chambers arrive.

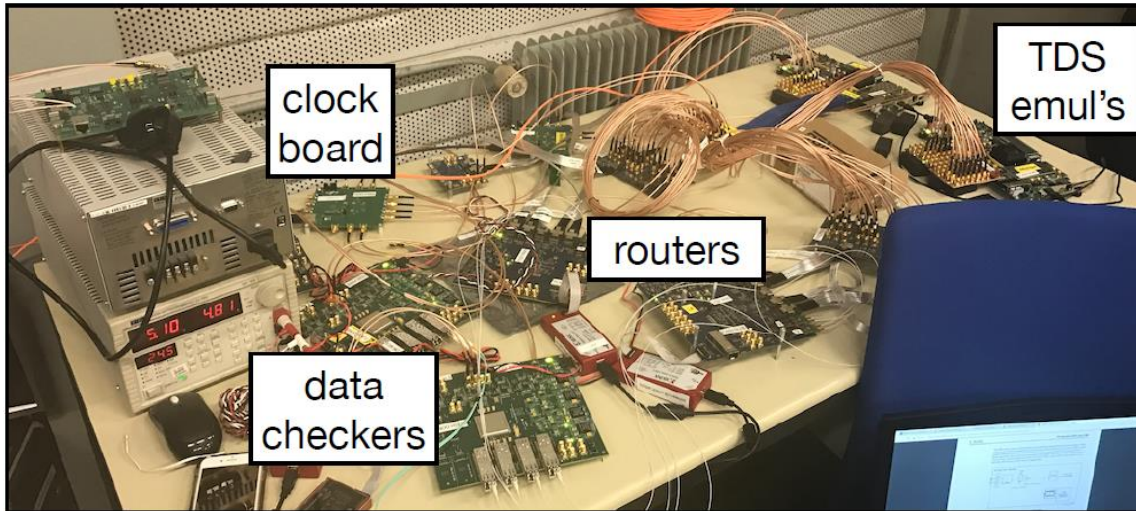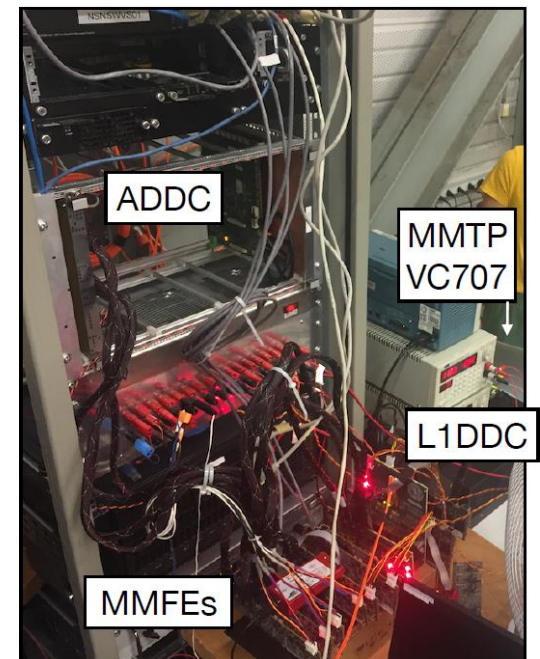# VS WEEK Test @ CERN 188

sTGC Trigger

- **SCA board with VMM & TDS chips**
- **12 CHs TDS emulator *2 setups**
- **Routers V2 prototypes *2**
- **Router-TP communication**
- **UDP output for TP diagnostics**

MM Trigger

- **Complete MM trigger path connected 8 MMFE→2 ADDC→ MMTP (Eval. board) with fake tracks "fitted" by TP**

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VS WEEK Test @ CERN 188

VMM data "decoder" Monitor
ROUTER
SI5338
VMM Test Pulse
"sFEB"
MTx fiber
Fake "TP" Checker
3m MiniSAS cable
SMA-MiniSAS Adapter
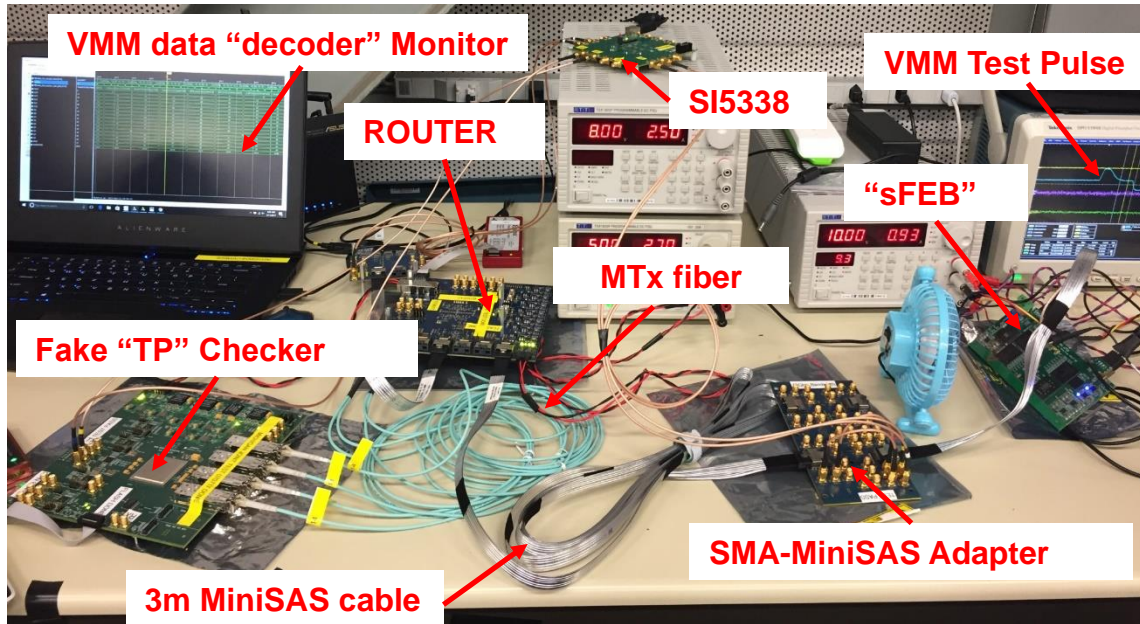
- ❑ **pFEB/sFEB tested with Router**
- ❑ **VMM test pulse as signal source**
- ❑ **Charge, strip info was checked by router "decoder"**

- ❑ **Router tested with rim-L1DDC to check reference clock jitter performance**

Fake "TP" Checker
Router
Bullseye cable
Rim-L1DDC
VC7215 TDS emul's
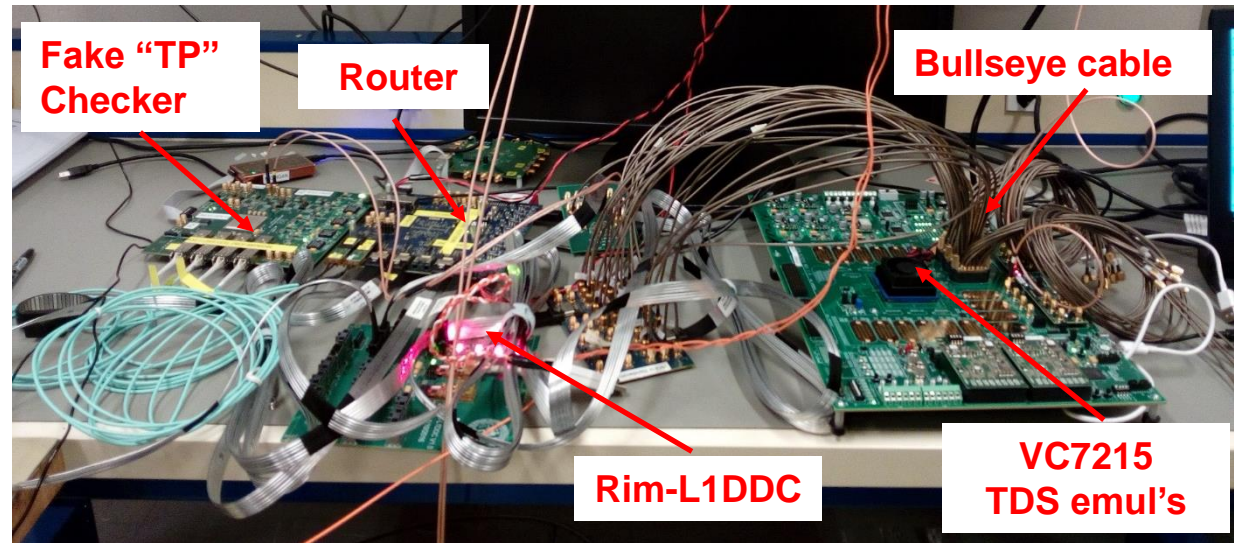
Radiation Tests for NSW Detector

- **NSW simulated radiation level**

New Small Wheel Simulated Radiation Loads and Magnetic Fields

		Inner Rim ($R = 1\,\mathrm{m}$)	Outer Rim ($R = 5\,\mathrm{m}$)
TID	(γ)	$460\,\mathrm{Gy}$	$16\,\mathrm{Gy}$
NIEL	(fast neutrons)	$2.3 \times 10^{13}\,\mathrm{n/cm^2}$	$7.3 \times 10^{11}\,\mathrm{n/cm^2}$
SEE[1]	(protons)	$4.2 \times 10^{12}\,\mathrm{p/cm^2}$	$1.3 \times 10^{11}\,\mathrm{p/cm^2}$
B field		$\leq 1\,\mathrm{kG}$	$5\,\mathrm{kG}$

- **Safety factors**

  - SF(TID) = 1.5*5*4=30.0
  - SF(NIEL) = 2.0*1*4=8.0
  - SF(SEE) = 2.0*1*4=8.0

e.g. unknown COTS batches

Radiation safety factors for New Small Wheel electronics.

Safety Factor	Type	Value	Notes
SF_{sim}	TID	1.5	Updated from [1] as per [2]
	NIEL	2.0	Updated from [1] as per [2]
	SEE	2.0	Updated from [1] as per [2]
SF_{ldr}	TID	5.0	COTS, no control for low-dose-rate effects.
	TID	1.5	ASIC, no control for low-dose-rate effects.
	TID	1.0	COTS/ASIC, accelerated aging or low-rate tests.
	NIEL	1.0	
	SEE	1.0	
SF_{lot}	all	4.0	Unknown COTS batches.
	all	2.0	Preselection; homogenous COTS or ASIC batches.
	all	1.0	Qualification; homogenous COTS or ASIC batches.

- **ATLAS required RTC**

RTC = SRL * Sfsim * SFldr * SFbatch

  - TID: ~48kRad
  - NIEL: 5.8*10^12 n/cm^2
 - SEE: 1.1*10^12 p/cm^2

e.g. NSW rim
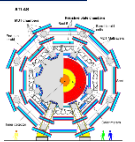
Radiation Tests for NSW Detector

- **NSW ASICs, Rim electronics has done several radiation tests**

- **Router as an example**

  - **Repeater TID test**
    - Time: 05/26/15 -- 05/30/15 @BNL
    - Source: Co-60 γ
    - Total dose: up to 1Mrad

  - **Artix-7 FPGA TID test**
    - Time: 08/23/15 -- 08/29/15 @BNL
    - Source: Co-60 γ
    - Total dose: up to ~500krad

  - **Artix-7 FPGA SEE test**
    - Time: 10/27/15 -- 10/31/15 @LANSCE
    - Time: 05/08/17 -- 05/12/17 @Demokritos

- **LANSCE 2017 Sep. joint neutron beam test**

  - **Clock fanout chip**
  - **Router with fully function**
 - **Flash chip**
  - **TDS ASIC**

Repeater board @ Co-60 source location
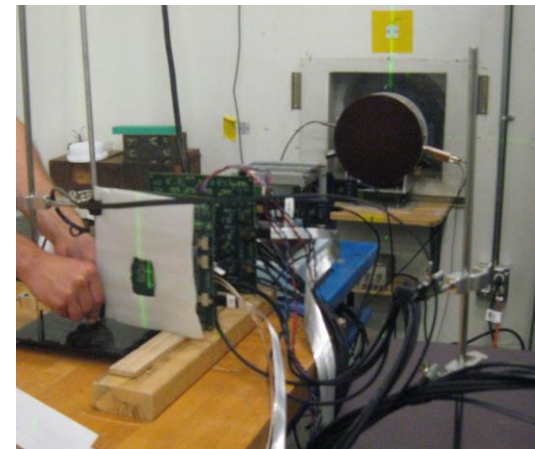
Router board @ LANSCE, 2015
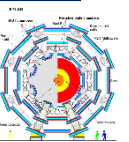
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Summary and Outlook

- **The NSW upgrade is necessary for ATLAS to improve the LV1 muon trigger and maintain precision tracking capability at high luminosity**

- **Separate trigger strategies for two sub-detector systems have been developed, taking into account substantial readout and geometry differences**

- **Advance development of trigger/readout electronics to achieve precise muon measurement requirement and Phase-I latency budget**

- **Vertical slice integration tests and radiation tests are ongoing to qualify NSW electronics system can survive in ATALS in next ten years**

- **System mass production will be lunch soon!**
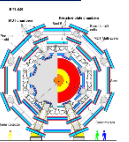
Thanks!
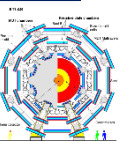
BACK UP

Radiation Tests at Demokritos