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# Commissioning of the Phase-1 upgrade of the CMS pixel detector

Benedikt Vormwald for the CMS Tracker Group

# Abstract

The Phase-1 upgrade of the CMS pixel detector is built out of four barrel layers (BPIX) and three forward disks in each endcap (FPIX). It comprises a total of 124M pixel channels in 1856 modules and it is designed to withstand instantaneous luminosities of up to  $2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ . The different parts of the detector have been assembled over the last year and later brought to CERN for installation inside the CMS tracker. At various stages during the assembly tests have been performed to ensure that the readout and power electronics and the cooling system meet the design specifications. After tests of the individual components, system tests have been performed before the installation inside CMS. In addition to reviewing these tests, we also present results from the final commissioning of the detector in-situ using the central CMS DAQ system, as well as results from cosmic ray data, preparation for the data taking with pp collisions.

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# Commissioning of the Phase-1 upgrade of the CMS pixel detector

Benedikt Vormwald for the CMS Tracker Group

University of Hamburg, 22761 Hamburg, Germany, benedikt.vormwald@cern.ch

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Keywords: pixel detector, silicon detectors, commissioning, detector system

# 1 CMS Pixel Phase-1 Upgrade

During the extended year-end technical stop of the LHC 2016/2017, CMS has replace its vertex detector. The new system is designed to withstand the harsh conditions of the LHC, with instantaneous luminosities of up to  $2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ , until the end of LHC run 3.

The detector maintains a four-hit coverage of up to  $\eta < 2.5$ , with the first layer placed closer to the interaction point (r = 29 mm) and the new additional fourth layer further outside (r = 160 mm) compared to the original pixel detector. It further features a new digital module readout, CO<sub>2</sub> cooling, as well as a  $\mu$ TCA based DAQ back-end system. The detector itself is subdivided into three forward disks on both sides (FPIX) as well as four concentric layers in the barrel region (BPIX). In total 1856 pixel modules have been installed, accounting for 124 million pixel channels. All the on-detector service electronics is housed on dedicated supply tubes (BPIX) and service cylinders (FPIX) which fulfill the requirement to match the mechanical envelope of the initial CMS pixel detector.

Details on the general design and the detector construction can be found in [1, 2]. This contribution focuses on the commissioning of the individual detector components.

# 2 Component Tests during Production

The pixel module is the smallest building block of the final detector system. The production of these modules has been shared among different groups within the CMS collaboration. In order to ensure the quality a set of standardized tests has been developed and applied following very closely every single production step of a module. These tests embrace very basic checks of the sensor and sensor connection (current-voltage characterization, bump-bond tests), but also functionality checks of the readout chip (ROC) and the readout periphery. The functionality of the full modules was tested before and after thermal cycles. In an X-ray setup, the rate capability as well as an absolute pulse-height calibration was determined. The calibration results acquired during the pre-installation tests have been used as starting point for the detector commissioning.

The components on the service cylinder and supply tubes have also been tested extensively during the production process. The detector modules are powered via DC-DC converters, which is necessary in order to allow to use the same power cables despite the fact of having 1.9 times the number of channels compared to the initial pixel detector. The design of the powering scheme and the component production is detailed in [3]. In total 1184 DC-DC converters have been installed.

The checkout of the full on-detector electronics followed closely the procedure of the full system checkout and, thus, will be described in Section 4.1.

# 3 Commissioning of Off-Detector Infrastructure

#### 3.1 CO<sub>2</sub> Cooling System

Two-phase CO<sub>2</sub> cooling is a very light-weight and efficient way of cooling a detector [4] due to the usage of tiny cooling pipes with diameters of 1.6 mm and a wall thicknesses of only 50  $\mu$ m. Thus, two-phase CO<sub>2</sub> cooling is the technology of choice for the CMS Phase-1 pixel detector.

The cooling plant has already been installed and commissioned successfully during the LHC long-shutdown 1. Thanks to the detailed planning and 3D computer modelling of the routing of signal fibers, power cables, and cooling pipes, the detector connection to the cooling system has been achieved without problems in spite of the very limited space at the detector bulkhead. The system has been pressurized with 100 bar of  $CO_2$ , which is five times larger than the operational pressure, and no leaks have been detected.

A flow reduction in the BPIX manifold has further increased the cooling efficiency, which is due to the fact that the vapor quality could be further improved by this action. Since then the cooling system is operating very stably at a pressure in the accumulator of about 20 bar and a corresponding outlet  $CO_2$  temperature of -20 °C. The effective temperature at the position of the pixel modules amounts to about -10 °C.

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#### 3.2 $\mu$ TCA DAQ System

In the context of the CMS Phase-1 pixel upgrade also the entire back-end DAQ electronics in the service cavern has been replaced, switching to the new CMS-wide crate standard  $\mu$ TCA [5].

In total there are 19 Front-End Controllers (FEC), which control the detector hardware, and 108 Front-End Drivers (FED), which read out the pixel modules. All of these components are based on a generic AMC card built around a Xilinx Kintex 7 FPGA and 4GB of DDR3 RAM. The different flavors are realized using different FPGA mezzanine cards and different firmware. The hardware is able to drive and receive links of up to 10 Gbit/s.

In order to be able to exercise, validate, and test the FEDs, an emulator of the optical pixel module output has been developed. Using this FED tester, the data throughput of a FED could be measured. In this test, 100 kHz of random triggers (level-1 trigger rate at CMS) are sent to the FED and the FED is loaded with a varying number of emulated hits per channel. The FED transmits the data via a 10 Gbit/s readout link to the central CMS DAQ infrastructure. If the load gets too high, the FED throttles the trigger rate. In the test no trigger throttling has been observed up to three emulated hits per ROC and channel, which is well above the expected rate in 2017.

The full DAQ chain has been tested including all 108 FEDs. Each FED can emulate data on-board. The DAQ chain has been loaded with three emulated hits per ROC and channel in each FED, which corresponds to the rate in the first barrel layer for 105 pile-up events. No problems in the downstream DAQ chain have been encountered.

## 4 Detector Checkout and Commissioning

#### 4.1 Procedure

For the system checkout the signal path from the back-end electronics upstream to the detector is established. Therefore, the different parts in the upstream DAQ chain need to be adjusted. In a first step, the light level of the opto-links are varied in order to check the physical connection between the detector and the counting room. After that, global signal and trigger delays are adjusted until a communication with the transmitter chip on each module (Token-Bit-Manager, TBM) is achieved. The TBM orchestrates the readout of the individual ROCs in two independent streams with a rate of 160 Mbit/s. The two streams are multiplexed in a 4-to-5 coding scheme such that the outbound data rate accounts to 400 Mbit/s. In the checkout, both the 160 Mbit/s and 400 Mbit/s phases have been adjusted until a complete data word consisting of TBM header, a number of ROC headers, and TBM trailer could be decoded in the FED. Finally, test pulses have been injected in individual pixels and read out in order to test the signal path down to the level of the readout chip.

#### 4.2 Detector Status

Once the full signal path has been established down to the hit level, ROC parameters have been adjusted. The threshold of the ROCs for layer 2–4 and the forward disks have been optimized to about 1750 electrons, while for layer 1 in a first round of optimization the threshold was set to about 3000 electrons. This is a first conservative setting which might be further optimized in the coming months. The measured noise is well in agreement with the results from the pre-installation tests in the module production centers.

After the installation and during commissioning a few malfunctions have been detected which affect full readout or power groups such that in total 95.1% of the channels are active after the commissioning.

#### 4.3 Cosmic Runs

During the commissioning phase, the CMS Phase-1 pixel detector participated also in cosmic runs. This low-occupancy data provides very valuable input to the detector alignment. Clean, low-rate muon tracks offer the chance to adjust readout delays with respect to the level-1 trigger decision and to optimize the detector geometry used for simulation and reconstruction by inspecting the hit-on-track efficiency of the different subsystems. Improvements of the hit residuals from the order of 1 - 2 mm to the order of 0.1 mm have been achieved. These studies mark a very good starting point for the final detector alignment using collision data.

# 5 Conclusions

Thanks to many tests during the production and system integration, CMS went through a successfull commissioning of its new vertex detector. All the service facilities have shown to work without problems. Around 95% of the detector channels are active and in a good condition. Further work is ongoing to fully optimize the settings for layer 1. All in all, the detector is ready for data taking in 2017.

### References

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