GEFÖRDERT VOM
Bundesministerium für Bildung und Forschung
PRISMA DETECTOR LAB
JOHANNES GUTENBERG UNIVERSITÄT MAINZ
ATLAS EXPERIMENT

Challenges and performance of the frontier technology applied to an ATLAS Phase-I calorimeter trigger board dedicated to the jet identification

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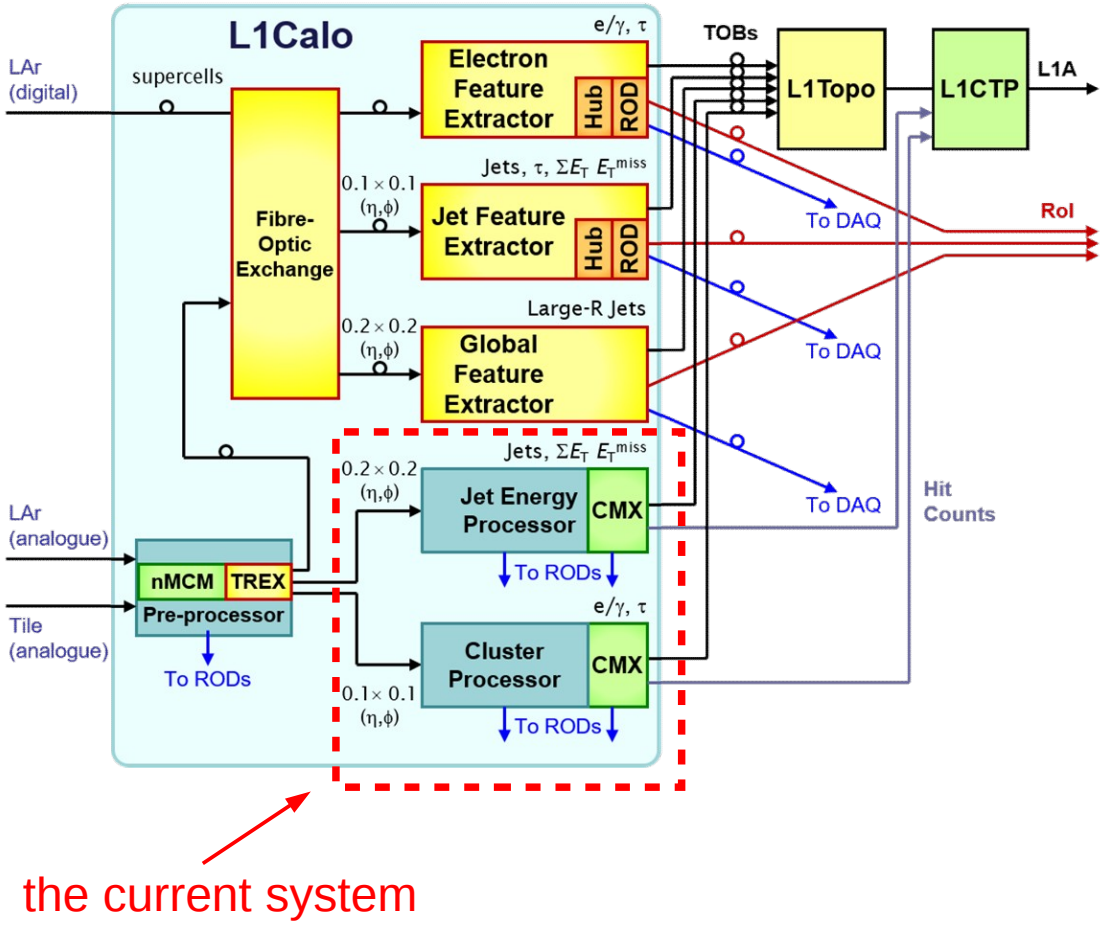
Outline

- Introduction
- jFEX Requirements
- Features and Challenges
- jFEX Prototype
- Signal Integrity
  - Data duplication using PMA Loopback
  - PCB Simulations: Signal Integrity Simulations
  - jFEX Prototype – Link speed tests
- Power Delivery
  - FPGA power consumption
  - PCB Simulations: Power / Thermal Simulations
  - jFEX Prototype: Temperature and Power Measurement
- Conclusions and Perspectives

Introduction

- Conditions
  - LHC luminosity: 2.5 x 10^{34} cm^{-2} s^{-1}
  - L1trigger rate ≤ 100 kHz
- Physics Motivations
  - Physics sensitivity to electroweak process
    - → low trigger thresholds (see TDR*)
- ➔ New L1 trigger system based on higher granularity
  - ➔ jet Feature EXtractor (**jFEX)** required



* Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System: CERN-LHCC-2013-018

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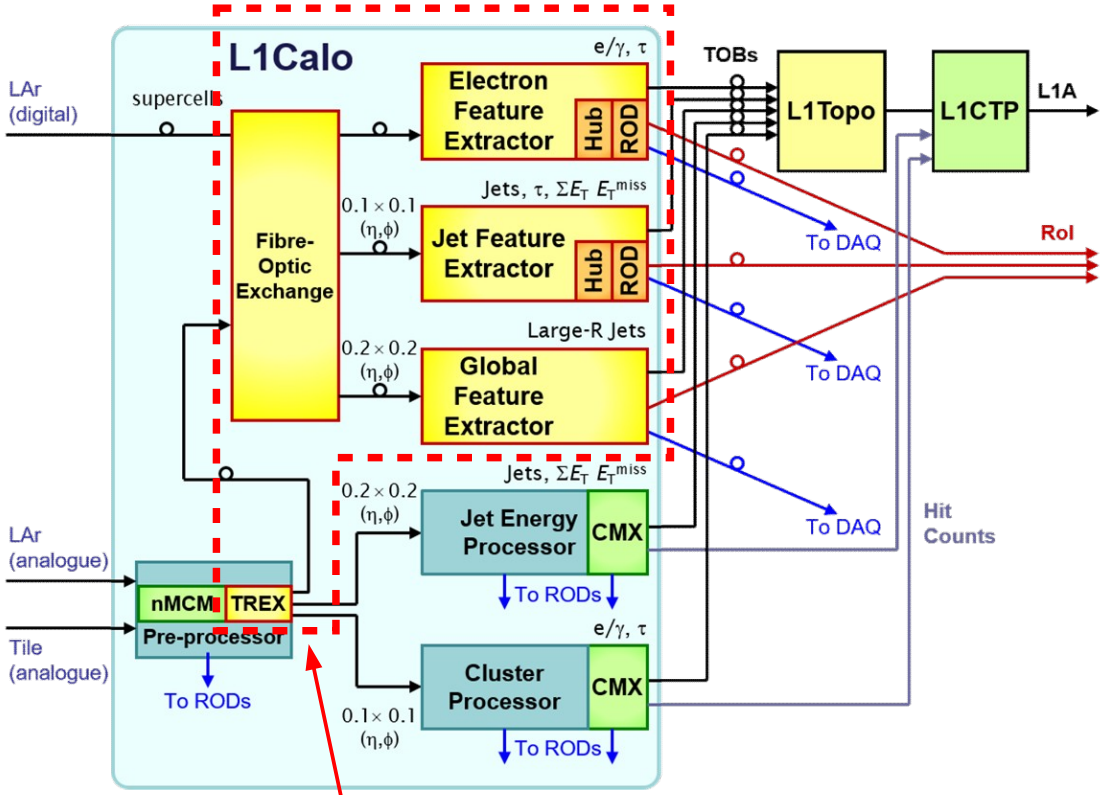

the Phase-I Upgrade
(Presented earlier today by Victor Andrei)

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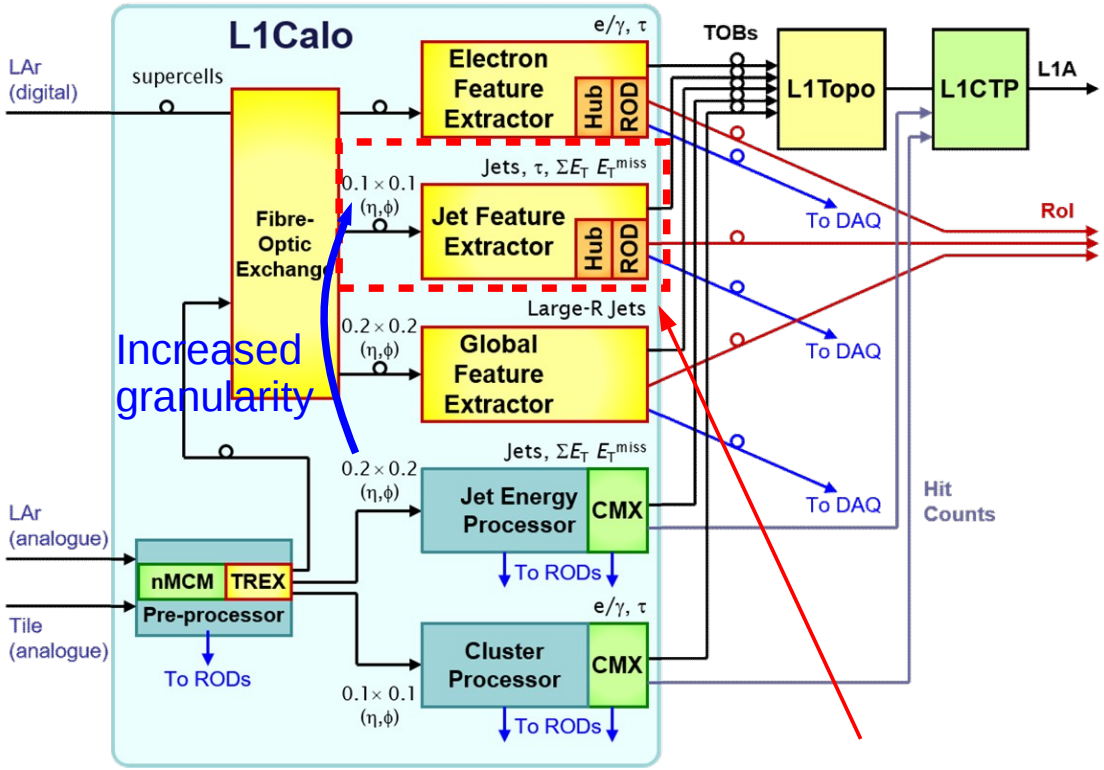
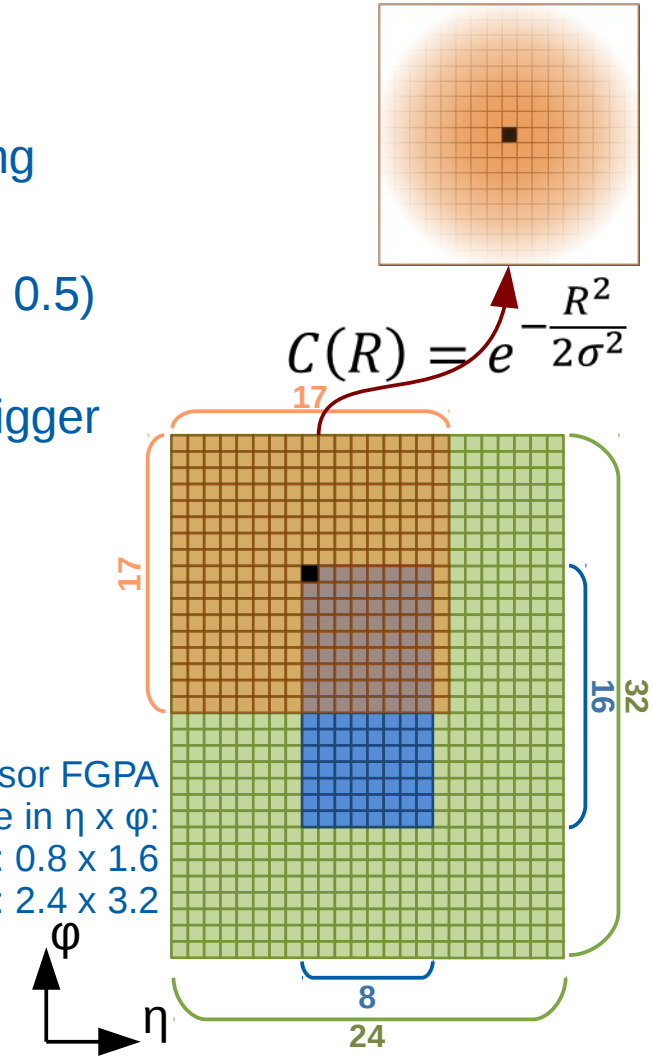


jFEX: topic of this presentation

* Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System: CERN-LHCC-2013-018

jFEX Requirements

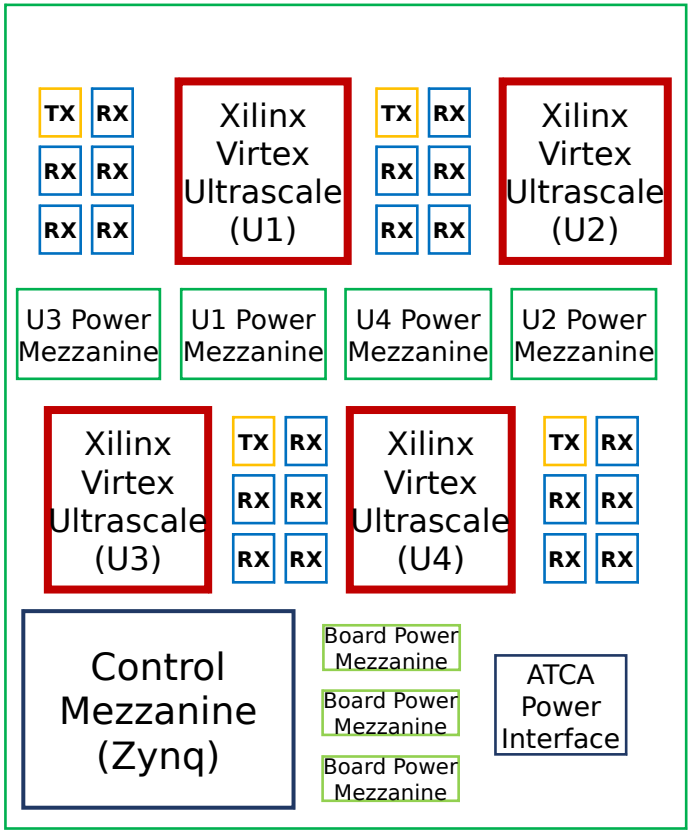
- Receive data from central and forward calorimeters
- Identification in real-time of Jet and Large-area tau candidates
  - capability for fat jets (up to 1.7 x 1.7 in η x φ)
  - Baseline algorithm: Sliding window with Gaussian weighting
    - Parallelized identification of local maxima
      - Comparing energy sums of jet core regions (0.5 x 0.5) of all possible jet positions
    - Calculation of jet energy sum by weighting adjacent trigger towers with Gaussian weights
- Calculation of Σ E_T and E_T^{miss}
  - Fully exploit calorimeter information (best E_T resolution) at highest possible granularity (up to 0.1 x 0.1)
- ➔ Large overlap region necessary for every processor
  - ➔ High factor of data duplication
- Latency budget: 387.5 ns (15.5 bunch crossings)
- ➔ **High input bandwidth and large processing power required**



Single Processor FGPA coverage in η x φ:
Core area: 0.8 x 1.6
Overlap: 2.4 x 3.2

Features and Challenges

- Features:
  - ATCA board
  - 4 Processor FPGAs (Xilinx Ultrascale XCVU190FLGA2577)
    - Each processor 120 Multi-Gigabit transceiver
  - Data duplication via PMA loopback
    - Each processor covers ¼ of φ range
    - Each module covers full φ range of eta ring
    - 7 modules to cover η range
  - 24 Avago MiniPOD: 5 RX + 1 TX per processor
    - Each MiniPOD: 12 channels
    - ➔ Incoming data per module: ~3.1 Tbps (@12.8 Gbps per channel)
  - Module control (mezzanine board)
    - Carrier board for Avnet PicoZed (Xilinx Zynq)
  - Power mezzanine boards



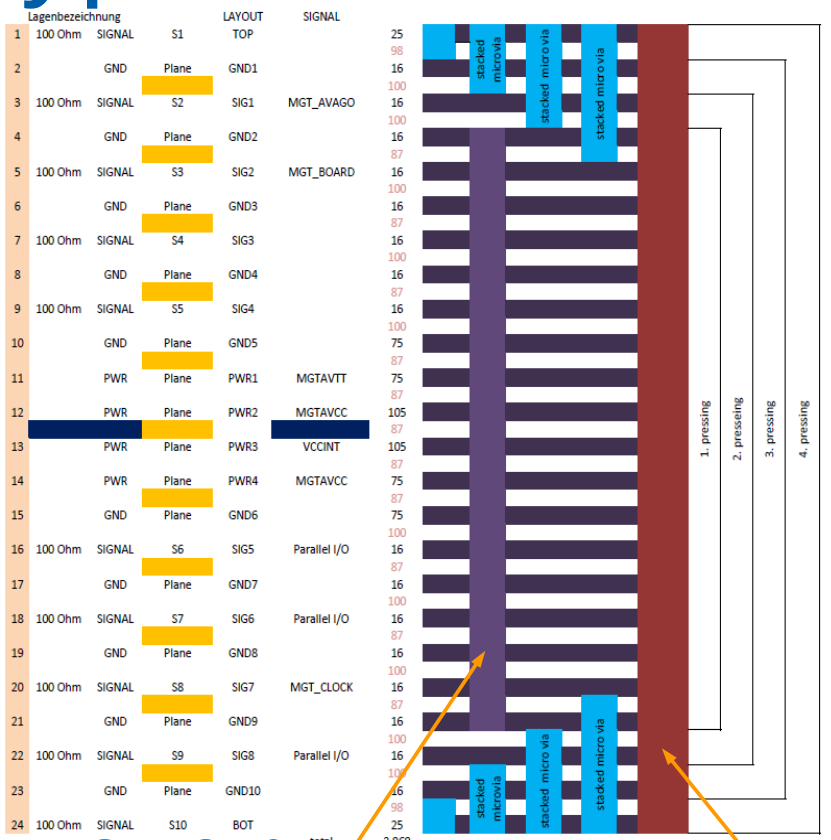
Features and Challenges (2)

- Challenges:
  - Tight routing space (breakout of 51x51 BGA)
    - Conflicting constraints:
      - Impedance of tightly-coupled differential signal pairs
      - Voltage drop on power planes
      - Drilling aspect ratio and via clearance
      - Number of PCB layers
      - Manufacturing costs
  - Signal integrity
    - Potential problems: attenuation, reflection, differential skew
    - Matched impedance for differential signal pairs routed on several layers
    - High density → possible cross-talk
  - FPGA power consumption
    - Uncertainty on required FPGA resources and toggling rate by the final algorithms
    - Cooling

jFEX Prototype

Signal layers alternating with ground planes

4 Power planes 105 µm and 70 µm copper



24 layers MEGTRON6

	pad / drill
Micro Via	350 / 100 um
Via50-25-75	500 / 250 um
Burried Via	450 / 200 um

Buried Via

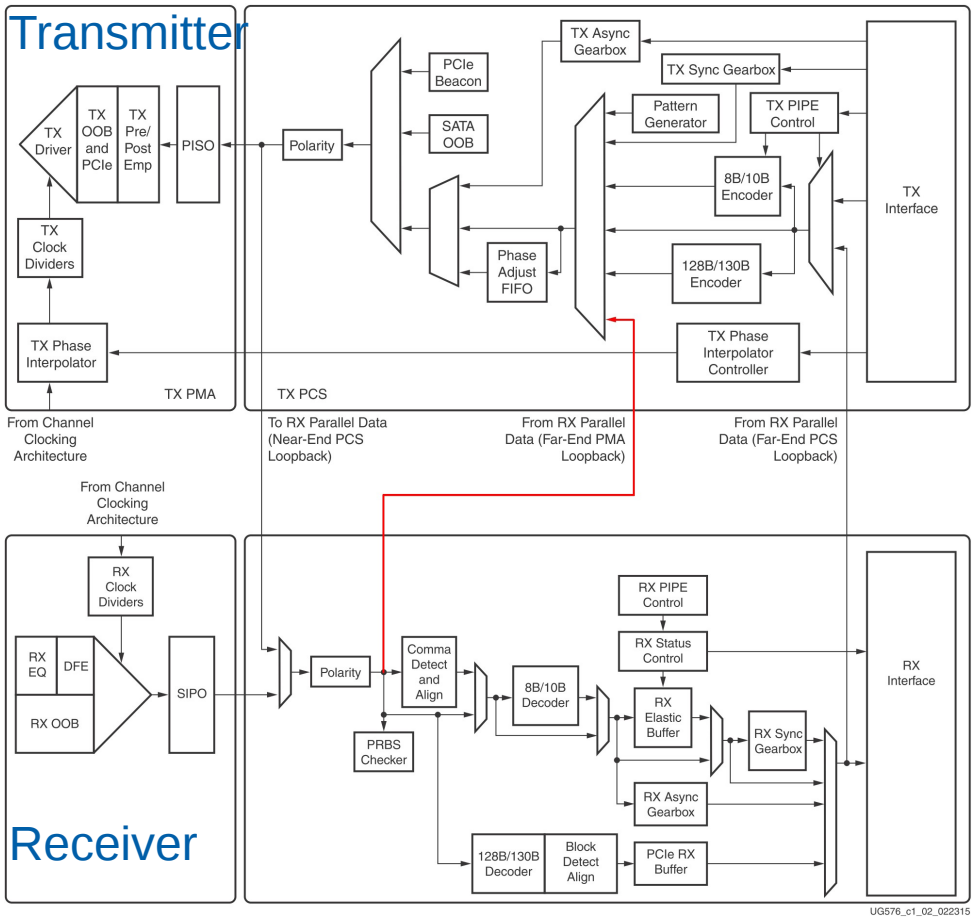
Through-Hole Via

Stacked Micro Vias

- Prototype received December '16
- Few months delay
  - One of two manufacturer gave up during production
- Assembled with one FPGA

Data duplication using PMA Loopback

Measurement of bit error rate on Ultrascale evaluation board VCU110

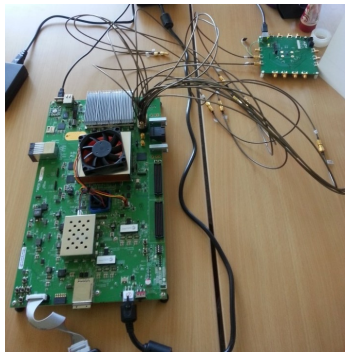


Data duplicated inside MGT Transceivers

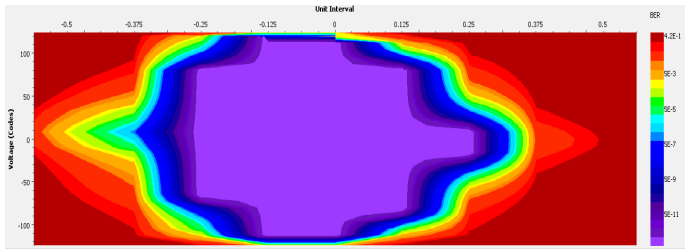
- Receiver gets data from original data source
- Branch-off in digital domain
- Data available in FPGA fabric AND injected in transmitter

Measurement:

- Electrical transmission on coax cables via Bullseye and SMA connectors
- Xilinx IBERT running at 28 Gbps



BER < 2.15 x 10e-16



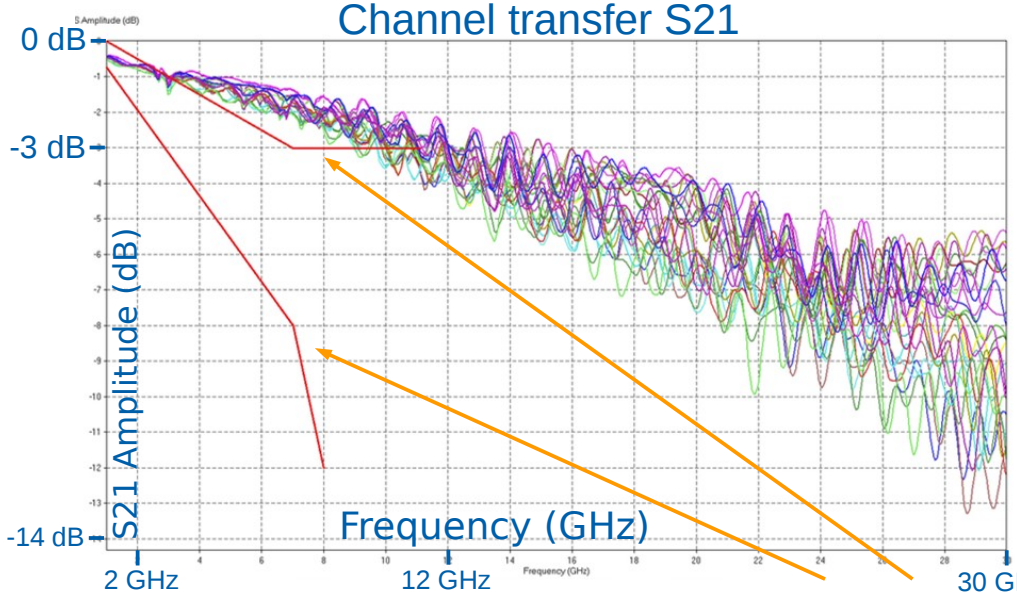
Xilinx: Ultrascale Architecture GTH Transceiver User Guide
https://www.xilinx.com/support/documentation/user_guides/ug576-ultrascale-gth-transceivers.pdf

PCB Simulations: Signal Integrity Simulations

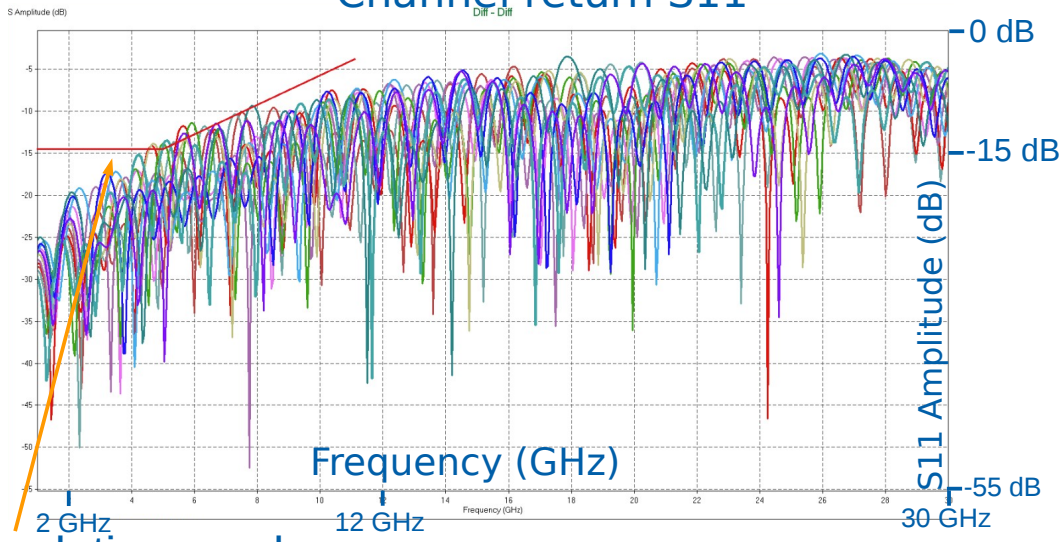
Post layout simulation of PCB traces for multi-gigabit links

- using Cadence Sigrity PowerSI
- PCB traces only simulated (without transmitter pre-emphasis and receiver equalization)
- Simulation results compared with SFP+ specifications (industrial standard with similar data rates)
  - Only few traces exceed recommendation for max. channel return by < 2 dB between 4-6 GHz
  - Specification recommends minimum attenuation for channel transfer to damp reflections
    - Prototype layout ~ 5 dB “too good”

Channel transfer S21



Channel return S11



SFP+ recommendation mask

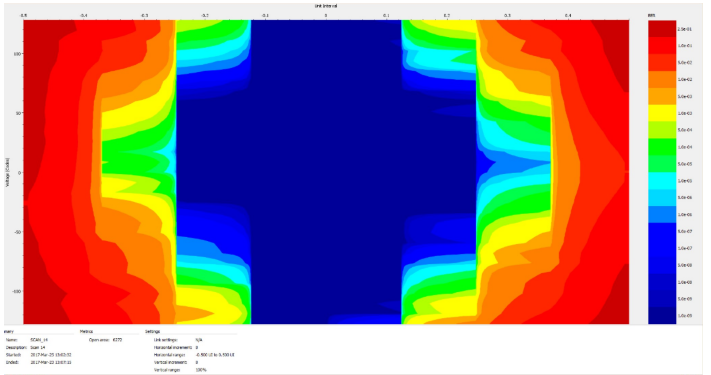
jFEX Prototype: Link speed tests

Tests at CERN with other modules

- LAr Trigger prOcessing MEzzanine (LATOME)
  - 48 links @ 11.2 Gbps
  - IBERT PRBS31
  - Formatted data (8B10B encoded)
- FEX Test Module (FTM)
  - 60 links @ 11.2 Gbps and 12.8 Gbps
  - IBERT PRBS31
  - Formatted data (8B10B encoded)

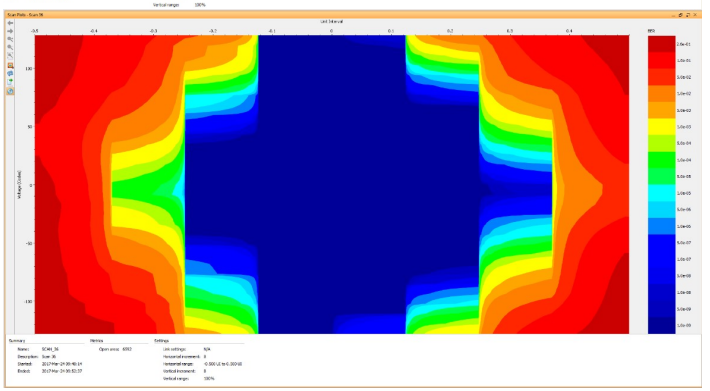
11.2 Gbps

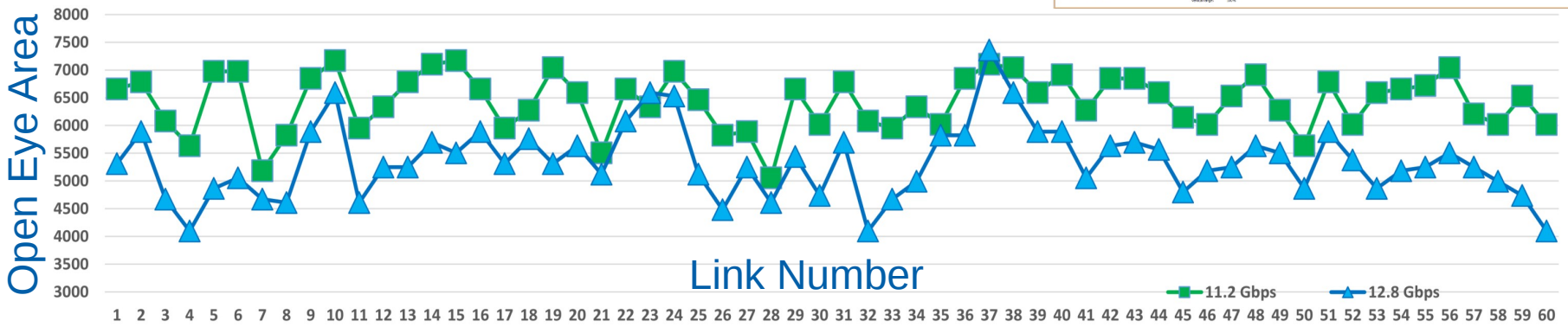
BER < 9.9 x 10e-16



12.8 Gbps

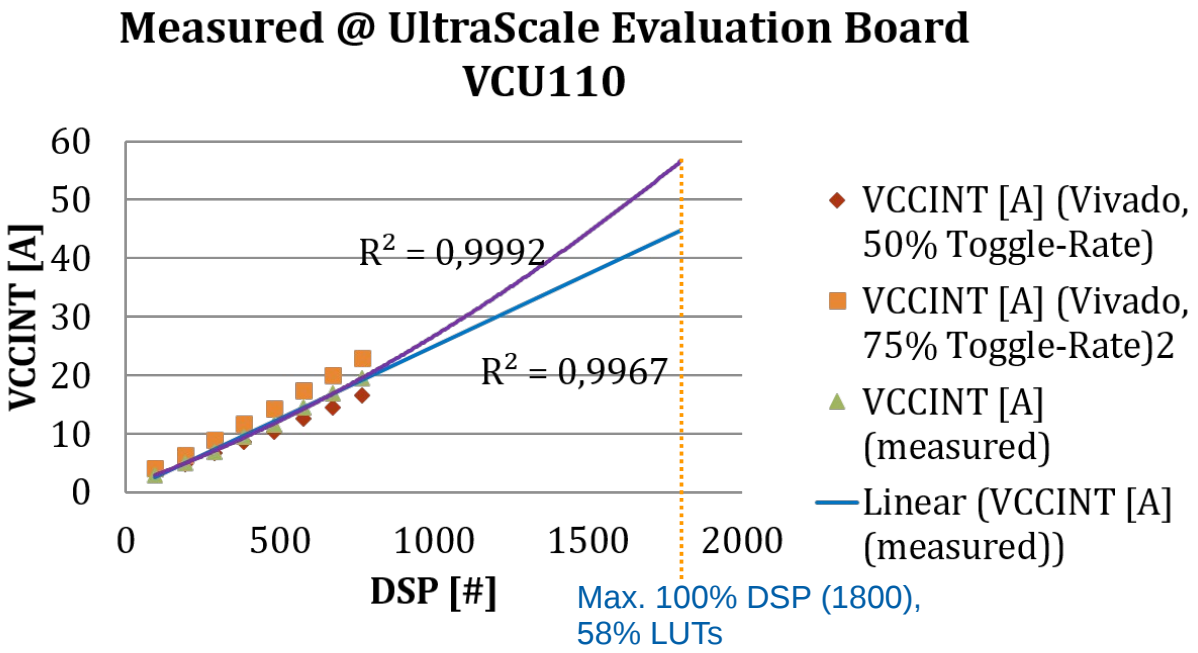
BER < 1.1 x 10e-15





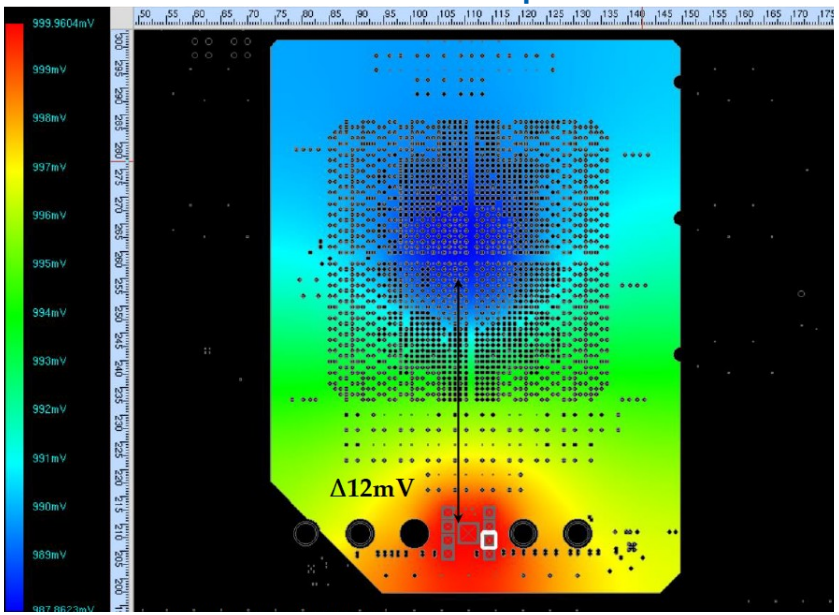
FPGA power consumption

- Xilinx Power Estimator used for initial estimates of power requirement
- Validated with measurements on Xilinx evaluation board XCU110
  - Measurement of FPGA power consumption depending on usage of FPGA resources (DSP)
  - Estimation of DSP usage for final algorithm version ~ 43 %
  - Expected max. current for VCCINT is ~ 35 A



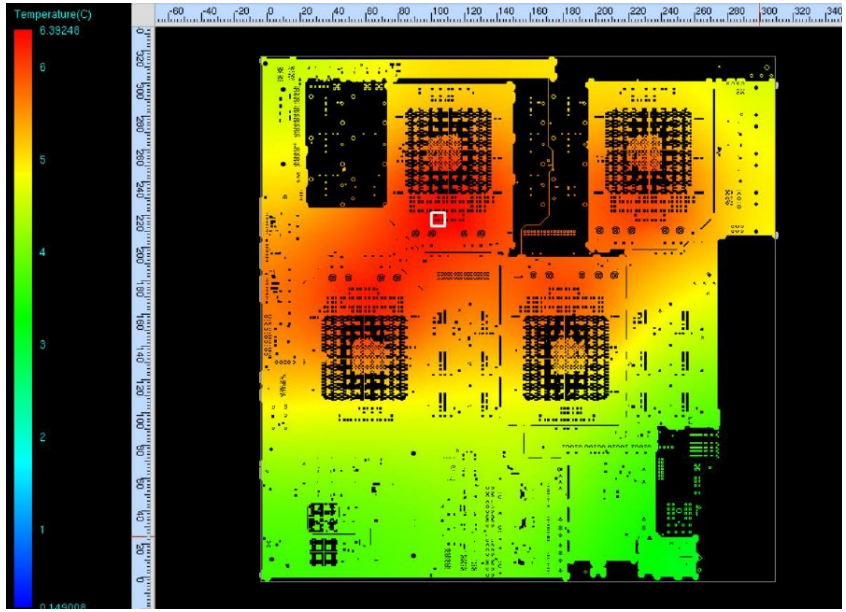
PCB Simulations: Power / Thermal Simulations

- PCB simulated for VCCINT current up to 60 A per processor
- Design challenge: ± 3% (=30 mV) VCCINT tolerance
  - **solved** with increased plane size and copper thickness



Voltage drop

- Max voltage drop 12 mV less than half of Xilinx specs
- Effective voltage drop further reduced by power supply sense lines



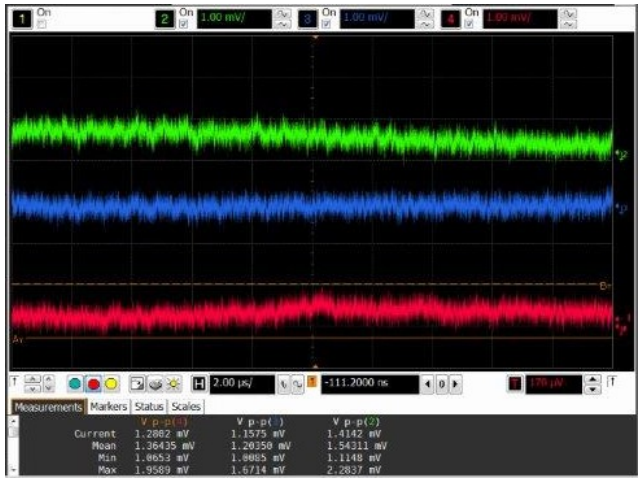
Temperature

- PCB stack-up has high thermal conductivity → no thermal hot spots
- Worst case: 6.4 °C temperature rise due to power loss on power planes

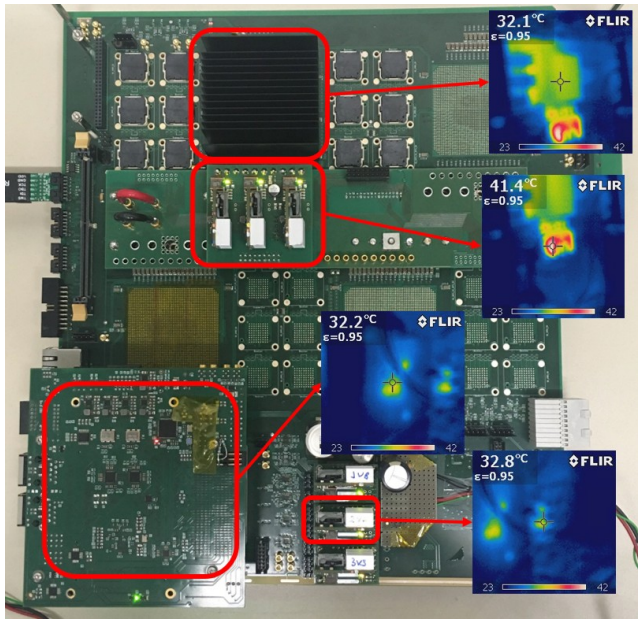
→ safe operational condition

Power and Temperature Measurements

- Ripple on Supply Voltages
  - Critical ripple requirement for MGTAVCC and MGTAVTT: Ripple < 10 mVpp
- Power Supply:
  - Artesyn SIL20C
    - Successfully tested
    - Measured max. ripple: MGTAVTT 2.0 mV, MGTAVCC 1.7 mV, VCCINT 2.3 mV
  - Next Step: TDK-Lambda iJX-Series
    - PMbus functionality



	11.2 Gbps 48 links	11.2 Gbps 60 links	12.8 Gbps 60 links
MGTAVCC (1.0V)	9.4	11.8	12.4
MGTAVTT (1.2V)	4.2	4.2	4.2
VCCINT (0.95 V)	8.2	10	11.4
12 V	5.8	6.6	6.9
FPGA Core Temperature	57	62	65



Conclusions and Perspectives

- Challenging luminosity conditions after Long Shutdown 2 (LS2)
- Upgrade of Level-1 Calorimeter trigger system required
- jFEX is one of the three new feature extractors
  - Working on higher data granularity than before
- 4 Processor FGPAs (Xilinx Ultrascale) per jFEX board (ATCA form factor)
  - Board input bandwidth: ~3.1 Tbps
- PCB layout was accompanied and checked by power, thermal and signal integrity simulation
  - Post-layout simulations suggest data transmission possible up to very high line rates
- First prototype produced with one processor assembled
  - Link speed tests with other modules as data source
  - Tests very successful so far
- Final production by July 2018
  - Installation and commissioning in ATLAS up to LHC restart in 2021