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Silicon Technologies for the CLIC Vertex Detector

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Abstract

CLIC is a proposed linear e^+e^- collider designed to provide particle collisions at center-of-mass energies of up to 3 TeV. Precise measurements of the properties of the top quark and the Higgs boson, as well as searches for Beyond the Standard Model physics require a highly performant CLIC detector. In particular the vertex detector must provide a single point resolution of only a few micrometers while not exceeding the envisaged material budget of around 0.2% X_0 per layer. Beam-beam interactions and beamstrahlung processes impose an additional requirement on the timestamping capabilities of the vertex detector of about 10 ns. These goals can only be met by using novel techniques in the sensor and ASIC design as well as in the detector construction.

The R&D program for the CLIC vertex detector explores various technologies in order to meet these demands. The feasibility of planar sensors with a thickness of 50–150 μm , including different active edge designs, are evaluated using Timepix3 ASICs. First prototypes of the CLICpix readout ASIC, implemented in 65 nm CMOS technology and with a pixel size of $25 \times 25 \mu\text{m}^2$, have been produced and tested in particle beams. An updated version of the ASIC with a larger pixel matrix and improved precision of the time-over-threshold and time-of-arrival measurements has been submitted. Different hybridization concepts have been developed for the interconnection between the sensor and readout ASIC, ranging from small-pitch bump bonding of planar sensors to capacitive coupling of active HV-CMOS sensors. Detector simulations based on Geant 4 and TCAD are compared with experimental results to assess and optimize the performance of the various designs.

This contribution gives an overview of the R&D program undertaken for the CLIC vertex detector and presents performance measurements of the prototype detectors currently under investigation.

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ABSTRACT: CLIC is a proposed linear e^+e^- collider designed to provide particle collisions at center-of-mass energies of up to 3 TeV. Precise measurements of the properties of the top quark and the Higgs boson, as well as searches for Beyond the Standard Model physics require a highly performant CLIC detector. In particular the vertex detector must provide a single point resolution of only a few micrometers while not exceeding the envisaged material budget of around 0.2% X_0 per layer. Beam-beam interactions and beamstrahlung processes impose an additional requirement on the timestamping capabilities of the vertex detector of about 10 ns. These goals can only be met by using novel techniques in the sensor and ASIC design as well as in the detector construction.

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1 Introduction

The Compact Linear Collider (CLIC) [1] is a proposed linear e^+e^- collider based at CERN in Geneva, Switzerland. Its construction is foreseen in three stages [2] as indicated in Figure 1, with collision energies between 380 GeV and 3 TeV. CLIC employs a novel two-beam acceleration concept in which a high-current, low-energy drive beam produces the RF for the acceleration of the main beams. The bunches of the drive beam are accelerated by klystrons at low frequency and a series of delay loops and combiner rings is used to increase the bunch frequency. High frequency RF power is produced and transferred to the main beams by decelerating the drive beam in normal conducting cavities. This approach enables RF field gradients of more than 100 MV/m to be attained and thus allows a compact collider design.

Owing to this acceleration scheme, the time structure of the CLIC beams has some features which directly impact the design parameters of the detector. The colliding bunches are arranged in bunch trains with a total length of 156 ns and a repetition rate of 50 Hz. One train consists of 312 bunches that are spaced by 0.5 ns. The low train repetition rate allows parts of the front-end electronics to be switched off between the bunch trains, the so-called *power pulsing* scheme, which significantly reduces the average power consumption of the detector and hence the required cooling infrastructure.

In order to reach the anticipated luminosity of about $\mathcal{L} = 6 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, each bunch of 1×10^9 particles is compressed to a size of about $\sigma_x \times \sigma_y \times \sigma_z \approx 40 \text{ nm} \times 1 \text{ nm} \times 44 \text{ }\mu\text{m}$. The high particle density in the bunch and the very small extent lead to strong electromagnetic interactions between the colliding bunches and particles within the bunch. The resulting beamstrahlung [3] reduces the total collision energy of the particles and produces a large amount of background particles, especially in the forward regions of the experiment. The impact of this beam-induced background can be reduced by applying timing cuts on the detector signals to select the hard interaction of interest. For most sub-detectors, a time resolution of about 10 ns is foreseen; a

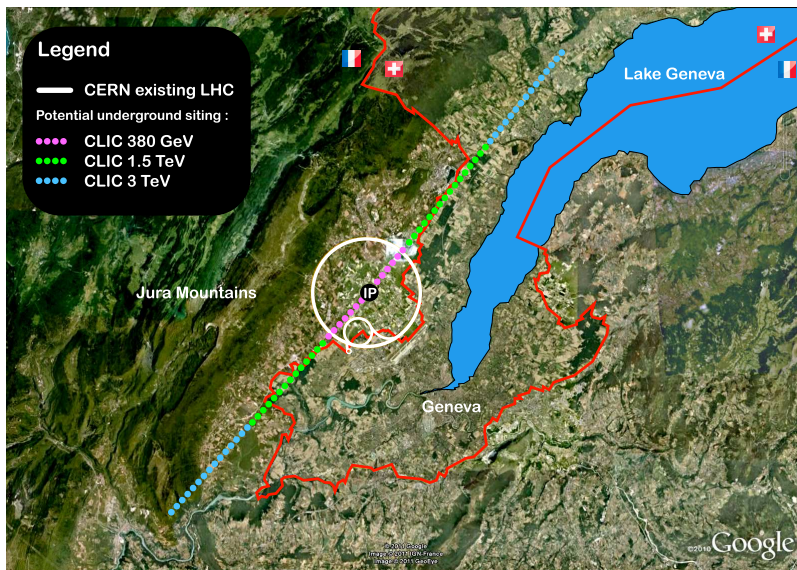


Figure 1. Proposed layout of the CLIC accelerator at CERN. The LHC and SPS rings are indicated and the three CLIC construction stages are shown in different colors.

correspondingly precise time stamping capability is required for the tracking systems of the CLIC detector. The CLIC vertex detector is the innermost component and provides crucial information for the identification of secondary decay vertices as well as for the reconstruction of particle trajectories.

The current proposal for the vertex detector comprises six barrel layers of silicon pixel detectors, arranged in three double layers with modules on both sides of the mechanical support structure. This approach allows the material budget, which is currently envisaged to be around $0.4\% X_0$ per double layer, to be minimized. The forward regions are also covered by three double layers, which are mounted in a spiral geometry to allow air cooling as described below. The current detector design foresees a hybrid pixel detector with a thin readout ASIC and silicon sensor, each having a thickness of about $50\ \mu\text{m}$. The pixel size is $25 \times 25\ \mu\text{m}^2$ and both planar sensors and capacitively coupled active sensors are considered. A single hit resolution of about $3\ \mu\text{m}$ is required to reach the desired impact parameter resolution for flavor tagging.

By power pulsing the front-end ASICs, the mean power consumption of the vertex detector is limited to below $50\ \text{mW cm}^{-2}$. The low power consumption and the detector geometry allow cooling using forced air flow which further reduces the overall material budget by not requiring cooling pipes and coolant. The spiral geometry of the forward regions acts as an airflow guide and ensures a proper distribution of the air in the detector. This approach has been shown to perform well in previous experiments featuring a barrel detector only [4] as well as in a mechanical mockup of the CLIC vertex detector [5].

2 The CLICpix Readout Chip Prototypes

First prototype readout ASICs following the requirements of the CLIC vertex detector have been developed. The CLICpix ASIC design [6] is derived from the Timepix/Medipix chip family [7–9] and is implemented in a commercial 65 nm CMOS process with an active pixel array of 64×64

pixels and a pitch of 25 μm . Each pixel features a charge sensitive amplifier (CSA), a discriminator as well as digital logic for the simultaneous measurement of a 4-bit time-of-arrival (ToA) and a 4-bit time-over-threshold (ToT) for every hit. The chip is operated in a shutter-based readout mode which is well-suited for the CLIC beam structure. Furthermore, it supports power pulsing of the analog circuitry and features an optional on-chip data compression. The chip has been extensively tested both in laboratory measurements and test beam campaigns and has shown to perform well as will be discussed later.

The CLICpix2 ASIC represents an advancement of the CLICpix design and is produced in the same 65 nm CMOS process. The chip features a larger active matrix with 128×128 pixels, which corresponds to a total active area of about $3.2 \times 3.2 \text{ mm}^2$. The pixel circuitry provides measurements of the ToA and ToT with 8-bit and 5-bit precision, respectively. Relative to the first prototype, the new ASIC has an improved noise isolation and a source of cross talk observed in CLICpix has been identified and removed. Furthermore, the new chip contains an integrated circuit for test pulses as well as a band gap reference and the capability of power pulsing for both the analog and the digital parts. A first production of the CLICpix2 has been received and is currently being tested in the laboratory.

3 Planar Silicon Sensor Studies

Planar silicon sensors are one of the options considered for the CLIC vertex detector. The following sections provide a brief overview of the different designs and assemblies under investigation.

3.1 Sensor Studies using Timepix ASICs

Different thin planar sensors with slim-edge and active-edge design have been tested using the Timepix [7] and Timepix3 [8] ASICs for the readout. Assemblies with 50 μm to 500 μm thick sensors have been produced and tested. The thinnest full assembly tested is a 100 μm thin sensor bump bonded to a Timepix chip thinned down to 100 μm [10].

The active edge technology [11] is an interesting option to reduce the amount of passive sensor area and thus the overall material budget of the detector. For this, the backside implant is extended to the edge of the sensor. The deep reactive ion etching (DRIE) process is used in order to achieve a smooth edge which allows for the implantation. Extending the backside implant alters the electric field configuration and allows the distance between the last pixel implant and the physical edge of the sensor to be reduced substantially.

Different sensor edge designs are possible, including the use of guard rings to shape the electric field. Several sensor designs with different guard ring configurations have been produced by Advacam [12] and tested for their charge collection behavior and efficiency. All sensors feature a pitch of 55 μm in order to facilitate testing with the Timepix3 [8] readout chip.

The first design tested includes guard rings which are kept at ground potential by connecting them to the readout ASIC with an additional row of bump bonds. Figure 2 (left) shows the single hit efficiency for the sensor edge. Here, all edge pixels have been folded into two pixel cells in order to increase statistics. It can be seen that the grounded guard rings lead to a sizable inefficiency near the edge in the regions between pixel implants as they compete with the guard rings for charge

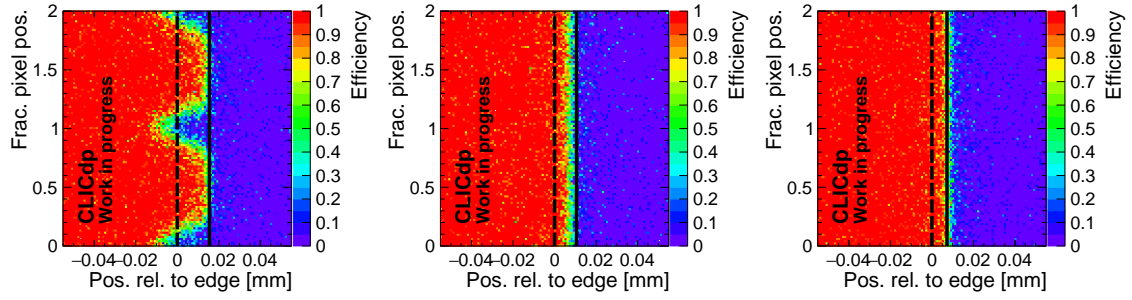


Figure 2. Single hit efficiency for active edge sensors with grounded guard rings (left), floating guard rings (center) and without guard rings (right). The distance from the pixel implant to the sensor edge is $28\ \mu\text{m}$, $23\ \mu\text{m}$ and $20\ \mu\text{m}$, respectively. The dashed lines indicate the implant end while the solid lines represent the physical edge of the sensor. Modified from [13].

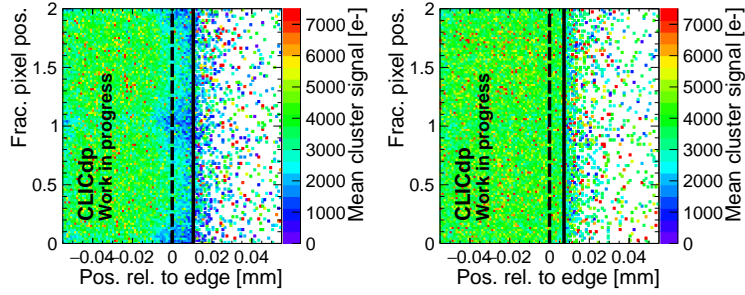


Figure 3. Mean cluster charge of active edge sensors with floating guard rings (left) and without guard rings (right). The distance from the pixel implant to the sensor edge is $23\ \mu\text{m}$ and $20\ \mu\text{m}$, respectively. The dashed lines indicate the implant end while the solid lines represent the physical edge of the sensor.

collection in particular between the pixels, where the distance to the guard ring might be smaller than to the adjacent pixels.

In the second design, the guard rings are left unconnected and thus floating. The impact of this change is demonstrated in Figure 2 (center), where only a marginal drop of the efficiency can be observed towards the physical cut edge of the sensor. Figure 3 (left) shows the mean cluster signal over a two-pixel region of the same sensor, and charge losses of tracks close to the sensor edge due to charge being collected on the floating guard ring are visible.

Full efficiency up to the physical edge of the sensor could only be achieved with the third design without guard rings. Figure 2 (right) shows that a uniform and very high single hit efficiency can be achieved. The previously discussed charge losses close to the edge are mitigated in this design as can be seen in Figure 3 (right).

These findings have also been studied in simulation using TCAD and good agreement is found. All sensors could be operated well above their depletion voltage without breakdown.

3.2 Sensor Studies with the CLICpix ASIC

Thin planar sensors with a pixel pitch of $25\ \mu\text{m}$ have been tested using the CLICpix ASIC. The ASICs have been produced on a multi-project wafer and the chips could thus not be post-processed

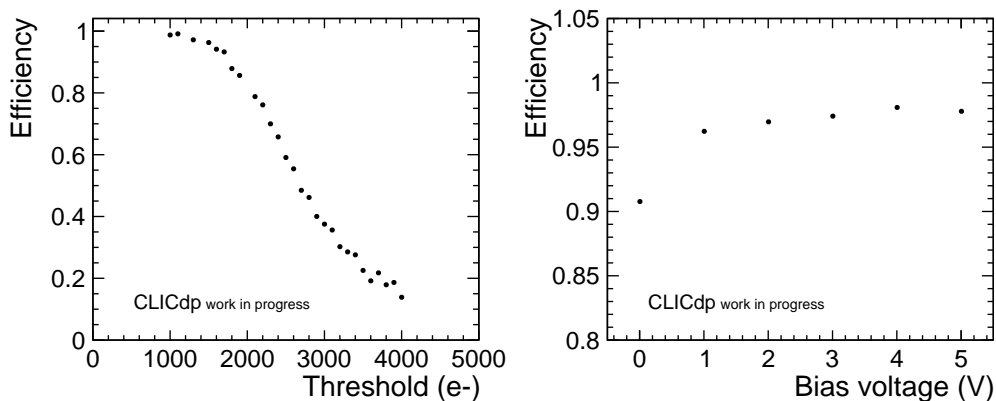


Figure 4. Efficiency of a 50 μm thick planar silicon sensor bump bonded to the CLICpix ASIC as a function of the applied charge threshold (left) and the bias voltage at a threshold of 1.2 ke (right).

at wafer level. While large-scale bump deposition on sensors with 25 μm pitch is established at wafer level [14], a custom process had to be developed at the Stanford Linear Accelerator laboratory (SLAC) [15] in order to allow bump bonding of single chips and sensors after dicing. For this, indium bumps were deposited on both ASIC and sensor prior to the flip chip process. Because of the small chip size and pitch, a large spread in quality between different assemblies has been observed. The optimization of the bump bonding process is ongoing and some of the observed issues have been understood in the meantime. Nonetheless, samples produced with several 200 μm -tick slim-edge planar sensor and a 50 μm active edge sensor allowed measurements and have been characterized.

Figure 4 (left) shows the efficiency of the 50 μm sensor assembly as a function of the charge threshold applied, with an efficiency of around 99% at a threshold of 1 ke. With lower charge thresholds, achievable with the design optimizations implemented in the CLICpix2 prototype, even higher efficiencies should be feasible. Figure 4 (right) shows the efficiency of the same assembly as a function of the applied bias voltage at a fixed charge threshold of 1.2 ke. While full depletion is reached at around 2 V, the detector is observed to be very efficient even in the absence of external biasing due to the built-in potential and an offset of the pixel ground level resulting from the biasing of the CMOS circuitry.

4 Capacitively Coupled Active Sensors

Active sensors implement some functionality for charge collection and amplification directly in the sensor. However, with standard CMOS processes, the charge is mostly collected by diffusion as the sensor cannot be fully depleted. High Voltage (HV) CMOS processes [16] allow transistors to be shielded by an additional deep n -well and thus enable a fast signal collection in the sensor by applying a moderate bias voltage. This removes the need for bump bonding as the sensor can be directly glued to the readout ASIC and the amplified signal transferred via capacitive coupling.

For the CLIC vertex detector, a Capacitively Coupled Pixel Detector (CCPDv3) [17] has been designed. It is produced in a commercial 180 nm HV-CMOS process and features the same footprint

as the CLICpix ASIC with an active pixel matrix of 64×64 pixels with a pitch of $25 \mu\text{m}$. Each pixel contains a CSA as well as a second inverting amplifier stage. The chip contains only limited standalone readout capabilities and is designed for being read out by the CLICpix ASIC. Although comprehensive test beam studies [18] have shown good performance of the sensor, some parameters, e.g., the amplifier peaking time of around 120 ns , do not yet meet the requirements for the CLIC vertex detector. Studies of the impact of misalignment of the two components during fabrication on the total coupling capacitance and the cross coupling between pixels have been performed [19].

A major redesign of this sensor has been developed and produced, called CLIC Capacitively Coupled Pixel Detector (C3PD), including power pulsing circuitry, an improved test pulse injection and a single amplifier stage. Standalone measurements in the laboratory show an improved amplifier rise time of about 20 ns and high average gain of 190 mV/ke . Some samples have been thinned down to $50 \mu\text{m}$ and no performance degradation has been observed. A full test of the sensor using the CLICpix2 ASIC is foreseen for the coming test beam campaigns.

5 Summary and Outlook

The CLIC accelerator technology and the resulting beam structure impose stringent requirements on the CLIC vertex detector. New readout ASICs and sensor technologies are being developed to meet the goals of a low mass detector with high spatial and temporal resolution.

The first readout chip prototype, CLICpix, performed well in several test beam campaigns. CLICpix2 represents an advancement of this design with several improvements and a larger active area, and is currently under investigation in the laboratory.

Several technologies are considered for planar silicon sensors. First samples of sensors thinned to $50 \mu\text{m}$ have been tested and perform well. Active edge technology would allow the reduction of passive material by extending the active region of the sensor to the physical cutting edge. Different guard ring designs have been investigated and sensors without guard rings have been found to provide the best efficiency up to the sensor edge. The small pitch of $25 \mu\text{m}$ poses a challenge for bump bonding but processes have been developed to allow bump bonding at single chip level.

The concept of capacitively coupling an active sensor to the readout ASIC is under investigation as a possible alternative to standard planar silicon sensors. Assemblies of the capacitively coupled active sensor CCPDv3 and the CLICpix ASIC have been produced and successfully operated. Based on this experience, an advancement of the active sensor, C3PD, has been designed. The chip has shown to perform well in laboratory measurements and will be tested in a particle beam using the CLICpix2 chip for the readout.

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