A NEW ORBIT SYSTEM FOR THE CERN ANTIPROTON DECELERATOR

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Abstract

This contribution will describe the new orbit system foreseen for the Antiproton Decelerator (AD) located at CERN. The AD decelerates antiprotons from 3.57 GeV/c down to 100 MeV/c, with an intensity ranging from 1×10^7 to 5×10^7 particles. The orbit system developed is based on 34 horizontal and 29 vertical electrostatic beam position monitors (BPMs) fitted with existing low noise front-end amplifiers. After amplification, the BPM signals will be digitized and down-mixed to baseband, decimated and filtered before computation to extract the position. The digital acquisition part of the orbit measurement system is based on the VME Switched Serial (VXS) enhancement of the VME64x standard and includes VITA57 standard FPGA Mezzanine Cards (FMC). The system is foreseen to measure complete orbits every 2.5 ms with a resolution of 0.1 mm.

INTRODUCTION

The AD ring [1] is a synchrotron where ~$3x10^7$ antiprotons produced from a production target are injected at 3.57 GeV/c. After RF manipulation and stochastic cooling, the beam is decelerated in several stages involving additional stochastic cooling, electron cooling and RF manipulation, before the antiprotons are extracted at 100 MeV/c. The AD revolution frequency varies from 1.59 MHz down to 174.5 kHz during the deceleration cycle. Fig. 1 shows a schematic view of the AD deceleration cycle and the essentials of its operation.

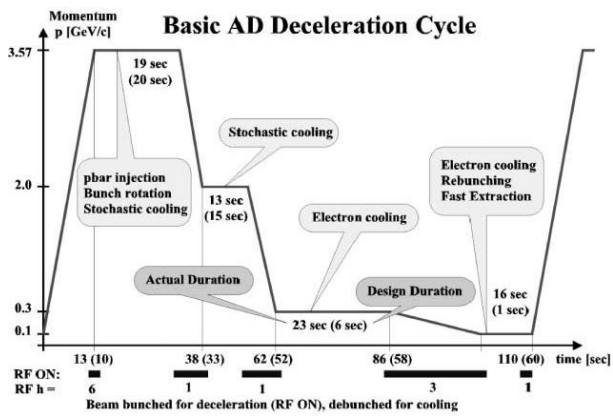

Figure 1: Basic AD deceleration cycle.

The present AD orbit system [2] has a limited performance in terms of time resolution since it is a multiplexed system acquiring signals from one BPM at a time. This allows for a complete orbit measurement only every 1.2 seconds. The new requirement of orbit measurements on the deceleration ramps involves moving to a parallel system where each BPM signal has its own analogue to digital converter (ADC) channel.

The new beam position system will use the same 63 BPMs as well as the head amplifiers of the present system, but with the reception amplifiers, the digital acquisition system as well as the front-end software totally updated.

The aim for the new system is to measure complete orbits every 2.5 ms with a resolution of 0.1 mm.

FRONT-END ELECTRONICS

Beam Position Monitors

The new orbit system acquires the signals from 34 horizonal and 29 vertical electrostatic BPMs. The sigma (Σ) signal is provided by a specific annular electrode while the delta (Δ) signals are derived from two semi-sinusoidal electrodes. The Δ signal level in the electrodes for $1x10^7$ particles is 4.2 μVp with a BPM differential sensitivity of 0.1 μVp/mm.

Head Amplifiers

The existing head amplifiers [2], placed close to the BPMs around the AD ring, will be also used in the AD new orbit system. These amplifiers have an equivalent input noise of 0.6 nV/√Hz for the Δ inputs, which is low enough to fulfil the 0.1 mm resolution requirement. In order to have this low input noise level, they feature a differential amplifier of 2 times 6 parallel Junction Field Effect Transistors (JFETs). The gain for the Δ outputs can be selected (47 dB or 20 dB) by means of a Transitor-Transistor Logic (TTL) digital control signal. The bandwidth for the high gain setting, which will be used in the new system, is 10 kHz – 20 MHz and the CMRR is better than 66 dB below 10 MHz. The head amplifiers have differential delta and sigma outputs which are transmitted from the AD ring to the AD control room. An analogue calibration input signal and two TTL digital control signals are implemented to simulate the maximum positive/negative beam displacement as well as a centred beam for calibration purposes.

Reception Amplifiers

New reception amplifiers, placed close to the digital acquisition system in the AD control room, have been designed to transform the differential signals coming from the head amplifiers to single ended signals and transmit them to the ADCs of the digital acquisition system. Two differential amplifiers with a 0 dB gain and a bandwidth of 560 Hz-80 MHz have been implemented for the sigma and delta signals.

ISBN 978-3-95450-176-2

ORBIT MEASUREMENTS

The analogue front-end electronics will deliver RF difference and sum signals for each BPM, i.e. 126 signals, which must be digitized and down converted to baseband for position calculations. The measurements will be carried out using the first harmonic of the f_{REV}, or the second harmonic in case of RF induced interference (EMI). Digital down conversion using the selected harmonic as local oscillator permits continuous position measurements during the whole deceleration cycle, whenever the beam is bunched. After low pass filtering and decimation of the complex I/Q data the positions are calculated (in mm) according to Eq.1.

$$Pos(t) = k \cdot \left(\frac{1}{\frac{\Delta}{\Sigma}_{cal}} \right) \cdot \left(\mathrm{Re}\left\{ \frac{I_\Delta(t) + jQ_\Delta(t)}{I_\Sigma(t) + jQ_\Sigma(t)} \right\} - \frac{\Delta}{\Sigma}_{zero} \right) + BPM_{off}. \quad (1)$$

k being the BPM sensitivity, BPM_{off} the total BPM offset Δ/Σ_{cal} the calibration slope calculated from calibration data and Δ/Σ_{zero} the offset obtained from calibration data.

The digital acquisition system includes a calibration procedure to obtain the calibration parameters required in equation (1). Three consecutive calibration acquisitions, simulating the maximum positive and negative beam displacements and a centred beam are performed to get three different values of the Δ over Σ signal for each BPM. In each calibration acquisition the system averages 522540 samples of the acquired Δ over Σ signal for each BPM. The calibration offset value (Δ/Σ_{zero}) for each BPM will be directly the averaged calibration value obtained for a centred beam (Δ/Σ_{zero}) while the calibration slope (Δ/Σ_{cal}) for each BPM will be given by Eq. 2.

$$\frac{\Delta}{\Sigma}_{cal} = \frac{\frac{\Delta}{\Sigma}_{pos} - \frac{\Delta}{\Sigma}_{neg}}{2}. \quad (2)$$

Being Δ/Σ_{pos} and Δ/Σ_{neg} the averaged calibration values obtained for the maximum positive and maximum negative beam displacements respectively.

DIGITAL ACQUISITION SYSTEM

System Layout

The new digital acquisition system is based on an in-house (CERN RF Group) developed hardware family [3]. This hardware family follows the VME Switched Serial (VXS) [4] enhancement of the VME64x standard, which supports switched serial transmission over a new high-speed P0 connector. For the daughter boards, the VITA57 standard FPGA Mezzanine Card (FMC) [5] is used.

Two different VXS-VME crates will be used to group the digitization of the horizontal and vertical BPM signals. In the horizontal crate, there will be nine VXS-DSP-FMC carriers, one holding a FMC-MDDS (FMC Master Direct Digital Synthesizer) and a FMC-ADC (FMC Analogue to Digital Converter) board and the rest holding two FMC-ADC boards. A timing module (CTRV) will provide all the triggers related to the AD cycle. The vertical crate will have a similar configuration. The digital acquisition system block diagram can be seen in Fig. 2.

The digitization of the BPM signals, at the FMC-ADC boards, and generation of the calibration analogue signals, at the FMC-SDDS board, as well as the associated low-level signal processing, at the FPGAs, is driven by a common RF clock which is a programmable higher harmonic of the AD revolution frequency (f_{REV}). A TAG pulsed signal marks the revolution frequency and synchronises all boards in the system. The RF clock and TAG signals will be generated from the revolution frequency by an FMC-MDDS board. The revolution frequency value will be calculated during the AD cycle by the Digital Signal Processor (DSP) of the VXS-DSP-FMC Carrier M1 from the value of the magnetic field of the main dipoles, the evolution of which is provided via a train of two pulsed signals (BUP and BDOWN).

VXS Switch Board

The VXS Switch board is used to interconnect the VXS-DSP-FMC Carrier boards via full-duplex Giga-bit serial links by means of the VXS transmission. Each VXS crate will contain two VXS Switch boards (positioned at a star-point) allowing the routing of a total of eight full-duplex links of up to 3.125 Gbit/s between any payload slot. In both crates, one VXS Switch boards will be used to distribute the RF clock and TAG signal through each VME-VXS crate and between crates. The other VXS Switch board will be used for the communication among VXS-DSP-FMC carriers by means of the VXS fabric through the VME-VXS crate and between crates. Optical fibres will connect the VXS switches of both crates.

VXS-DSP-FMC Carriers

The VXS-DSP-FMC carrier accommodates a Digital Signal Processor (DSP) ADSP-21368 and two Xilinx Virtex 5 Field Programmable Gate Arrays (FPGAs), known as the Main FPGA (XC5VLX110T) and FMC FPGA (XC5VSX95T). In order to distribute the RF clock and TAG signals, there are two dedicated full-duplex VXS channels from each VXS-DSP-FMC carrier routed to one of the VXS Switch boards. The other six full-duplex VXS channels, combined to form three 32 bit data paths, are used to transfer 10b8b-encoded data between VXS-DSP-FMC carriers at a raw link rate of 2 Gbit/s or 100 MSPS (32 bit). Each VXS-DSP-FMC carrier can host up to two FMC daughter boards with a high-pin count format. The VXS-DSP-FMC carrier also includes several memory banks for observation purposes. In particular, two, 4Mx18 bit banks that are clocked at 100 MHz and two 1Mx4x18 bit banks that are clocked at the RF frequency.

ISBN 978-3-95450-176-2

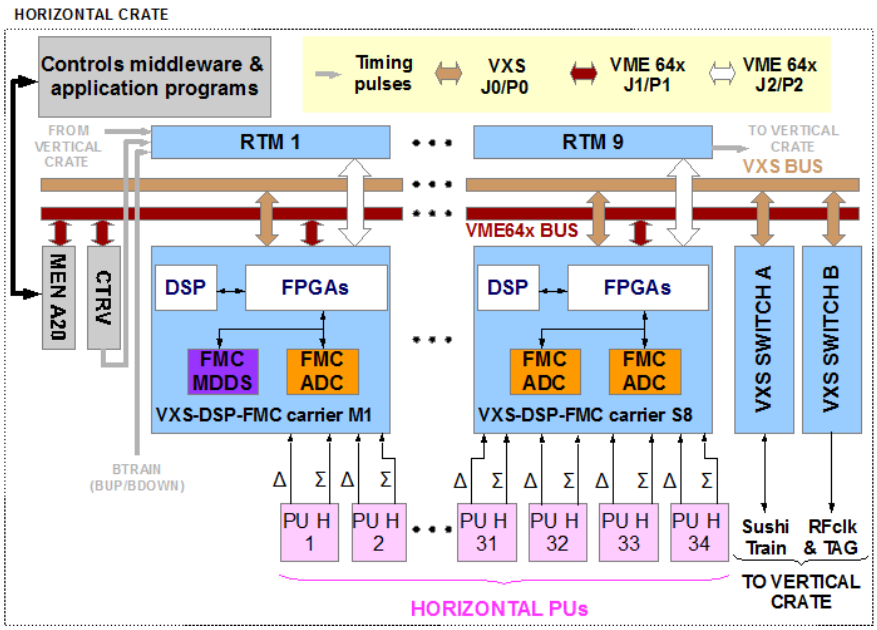

Figure 2: Digital acquisition system block diagram (horizontal crate). MDDS: Master DDS FMC board. ADC: Analogue-to-Digital FMC board. RTM: Rear Transition Module. CTRV: Timing Receiver Module. Men A20: master VME board. PU H: Horizontal transverse Pick-Up.

Rear Transition Modules (RTM)

There is a Rear Transition Module (RTM) connected to each VXS-DSP-FMC carrier through the J2/P2 connector. It carries all major secondary power supplies needed by the VXS-DSP-FMC carrier. The RTM front panel provides sixteen digital inputs and eight digital outputs, directly interfaced to the Main FPGA using stacked LEMO 00 connectors. The digital inputs can be configured as high impedance or TTL 50 Ohm. These digital inputs/outputs will be used to connect the trigger signals generated by the timing module, e.g. the start and end of the AD cycle, as well as to implement the timing and interlock wired daisy chains required by the system.

FMC-MDDS Daughter Board

The FMC-MDDS board generates the RF clock and the TAG synchronization signals. The RF clock can range from 62.5 MHz to 125 MHz at any revolution frequency harmonic from 1 to 1023. It needs a 10 MHz input reference clock to operate. Two independent channels are synchronized to the same input reference. The board includes a 32 bit direct digital synthesizer core (AD9858) with 232 mHz frequency resolution. It also features the possibility of distributing the RF clock and TAG signal either through VXS switch or a front panel eSATA connector.

FMC-SDDS Daughter Board

The FMC-SDDS is used to generate the analogue calibration signals required by the head amplifiers. This board is based on an AD9747 DAC and allows four independent digital-to-analogue conversion channels with 16 bits resolution and a programmable gain switching of 18 dB. The output is DC coupled, with a 40 MHz analogue bandwidth and a full scale, peak output voltage of 3.6 V. The sampling rate of the DAC mezzanine can go up to 250 MSPS.

FMC-ADC Daughter Board

The FMC-ADC board is used to digitize the BPM delta and sigma signals. It has four independent DC coupled channels, with an input signal range of ±1V over 50 ohms. Two dual, 16 bit ADCs (AD9286) with a sampling rate up to 125 MSPS are used for digitizing the input signals. The bandwidth of each channel is limited to 40 MHz. The gain of each input channel is selectable, 0 dB or 18 dB, with DC offset compensation performed automatically. The signal to noise ratio is better than 70 dB which is equivalent to 12.5 bits of resolution.

FPGA Firmware

The Main FPGA firmware implements the essential infrastructure for the system communication and data exchange. It includes the following communication channels:

- VME64x (A32/D32 + A32/D64 MBLT).
- DSP (A16/D32).
- VXS full-duplex dual 32 bit link with a transfer rate of 100 MHz (carrier-to-carrier).
- Communication and data exchange with the FMC FPGA (full-duplex 32 bit Gigabit links).
- Different I2C links to control the RTM or the VXS Switch boards.

The communication architecture is configured so that no arbitration is required on any of the link or bus interfaces in order to have a simpler and more reliable system. The

ISBN 978-3-95450-176-2

Main FPGA firmware also implements other useful blocks such as:

- a dual, 128 channel timing generator.
- 16 channel, 32 bit x 1024 vector function generators.
- 48 channel, 32-bit x 2048 programmable digital signal observation.

The Main FPGA firmware allows for remote updating of the FPGA and DSP software. Finally, numerous diagnostics functions are available. The main FPGA firmware will be the same for all boards and the capabilities will be enabled or disabled depending on the desired board functionality.

The FMC FPGA firmware implements the custom FMC hardware control and data treatment. Digital signal observation is also possible via configurable buffers clocked at the RF clock and located in the fast memory on the VXS-DSP-FMC Carrier board. The firmware code in the FMC FPGA is tailored to the specific FMC hardware via the instantiation of FMC IP cores, i.e. each daughter board is complemented by an FPGA IP core running on the FMC FPGA. These IP Cores are developed in independent version-controlled libraries through a collaborative design while the FMC FPGA common firmware is held in a separate library. The FMC FPGA firmware instantiates the corresponding IP cores in each slot.

The ensemble of FMC daughter board and corresponding IP core implements the functionality of a FMC-MDDS, FMC-DDC or a FMC-SDDS. The MDDS generates a clock that clocks all daughter boards at a high f_{REV} harmonic. The TAG signal phase synchronises all FMC-DDC and FMC-SDDS channels in the system.

The FMC-SDDS generates RF analogue signals of programmable f_{REV} harmonic and phase. Data acquisition and control are carried out in I/Q coordinates.

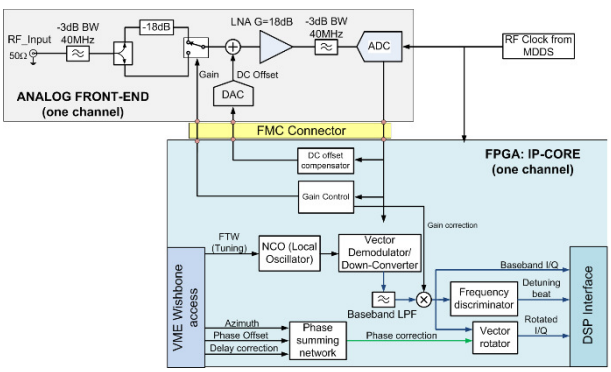

Figure 3: FMC-ADC board hardware and DDC firmware.

The FMC-DDC (Fig. 3) performs digitization, down-conversion, low-pass filtering and decimation. The digital down converter is a homodyne receiver that converts the selected beam revolution harmonic into a baseband I/Q signal. The ADC sampling clock and the local oscillator are locked to the RF clock, so the local oscillator frequency and phase is controlled to select the required beam revolution harmonic. A baseband low pass filtering and a decimation stage have been implemented by means of a first order Cascaded Integrator Comb (CIC) filter. The decimation factor and the differential delay of the CIC filter can be modified. The phase of the down-converted I/Q signal can be varied so as to compensate the beam time of flight and cable delay differences of each input channel.

DSP Firmware

The DSP firmware is developed in C code as an interrupt driven finite state machine. It implements the core data treatment and system control, such as the acquisition and data processing from the FMC-DDCs and the on-line control of all the FMC daughter boards. The DSP firmware will depend entirely on the functionality of the VXS-DSP-FMC carrier hosting the DSP itself and will allow full system customisation.

The DSP firmware of the M1 VXS-FMC-DSP carrier controls the FMC-MDDS operation and acquires data from two horizontal BPMs via the FMC-DDC daughter board. This DSP firmware also calculates the revolution frequency during the AD cycle from the value of the main dipoles magnetic field. The hand-shaking via VXS communication to synchronize all the FMC-DDC daughter boards is also controlled by the M1 DSP firmware.

The DSP firmware of the M2 VXS-FMC-DSP carrier controls the FMC-SDDS operation for the calibration and acquires data from two vertical BPMs by means of an FMC-DDC daughter board.

The DSP firmware of the other VXS-FMC-DSP carriers (S1 to S15) is configured to acquire data from 4 BPMs using two FMC-DDC daughter boards per carrier.

SOFTWARE

Specific real-time and communication software running in the dedicated VME crates is needed in order to perform data post-processing, calibration runs, real-time control following machine timing and to ensure a seamless integration of the measurement into the AD operational control system. The standard CERN software framework (FESA: Front End Software Architecture) [6] is used for running the new AD orbit system. This implementation will allow for easy porting to the ELENA (Extra Low ENergy Antiproton) machine, currently under construction and foreseen to use the same orbit system.

SYSTEM STATUS AND TESTS

Most of the hardware required for the system is already produced, tested and installed, with the exception of the FMC-ADC boards. The current version of the FMC-ADC daughter boards was found to be too noisy for the system. The noise density level of the FMC-ADC board must be lower than 20 nV/√Hz for the BPM Δ input signals while, in the current version of the FMC-ADC board, it was found to have noise peaks of up to 45 nV/√Hz in the bandwidth of interest (174.5 kHz - 1.59 MHz). These peaks were due to the switching frequency of the on-board DC-DC converters used to generate the ±5V and 1.8V power supply levels. It was therefore decided to redesign the FMC-ADC board to have AC coupling inputs in order to

ISBN 978-3-95450-176-2

require only positive power supply levels (10V and 1.8V) generated with linear regulators. Preliminary results measured with a prototype show that the maximum noise density level for the FMC-ADC AC coupled version is well below 10 nV/√Hz.

The DSP firmware for each VXS-DSP-FMC carrier is already developed. The FPGA firmware has been upgraded in order to allow communication of up to 32 VXS-DSP-FMC carriers via the VXS. Other minor changes have also been included to be able to read out the BPM position data continuously during the whole AD cycle.

The specifications for the software have been written and the final software is currently being developed. For the initial system tests, different scripts based on Python have been developed to mimic the final software.

An initial version of the system with only the M1 VXS-DSP-FMC carrier without VXS communication was tested in December of 2014 in AD as proof of concept of the system, with data from two BPMs acquired successfully.

A second version of the system is currently being tested in AD with beam. It consists of a VXS-VME crate holding the M1 VXS-DSP-FMC carrier, the M2 VXS-DSP-FMC carrier, another six (S1-S6) slave VXS-DSP-FMC carriers and a CTRV timing module. The aim is to acquire data from all vertical BPMs and test all the features of the final system (VXS communication, calibration procedure, etc.) in real conditions. For this test, the noisier DC-coupled version of the FMC-DDC boards will be used until the new AC-coupled FMC-DDC boards are available.

Fig. 4 shows the position measurement for a vertical BPM during the first flat top and deceleration ramp in the AD cycle (3.57-2 GeV/c). It can be seen that a position signal with a resolution better than 0.1 mm is obtained from 35 s onwards, corresponding to the time when the beam is bunched (it being debunched for stochastic cooling beforehand).

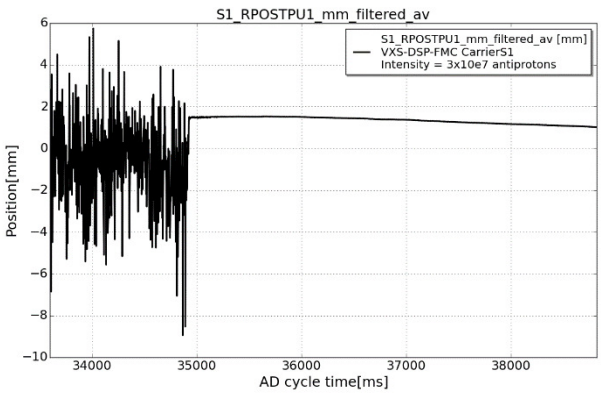

Figure 4: Position measurement for a vertical BPM acquired with the S1 VXS-DSP-FMC carrier during the first flat top and deceleration ramp in the AD cycle.

Fig. 5 shows the position measurement for the vertical plane of all BPMs during the first flat top. The green line corresponds to the current orbit system and the blue line to the prototype version of the new orbit system being tested. The discrepancies between both systems are currently being investigated.

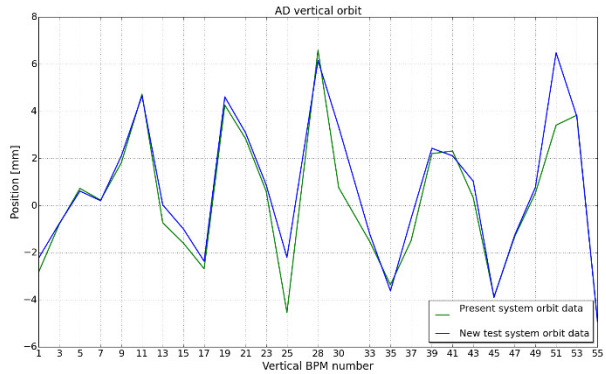

Figure 5: Position measurement all vertical BPMs acquired during the first AD flat top (at 35.77 s) with the current orbit system (green line) and the prototype version of new orbit system (blue line).

The final AD orbit measurement system is foreseen to be commissioned by the end of 2015.

CONCLUSION

The design of the new orbit system for AD has been presented. It will use the same 63 BPMs and the head amplifiers than the current orbit system. A new digital acquisition system based on in-house developed hardware will digitize and process the BPM signals to obtain an orbit measurement with a resolution of 0.1 mm every 2.55 ms. The 17 VXS-DSP-FMC carriers and the 34 FMC daughter boards used will be accommodated in two VME-VXS crates for acquiring the horizontal and the vertical BPM signals. The majority of the hardware is already produced and tested, with a new low noise FMC-ADC board under development. Tests with a prototype version of the final orbit system are currently being carried out with beam in the AD, with the final orbit system foreseen to be commissioned by the end of 2015.

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ISBN 978-3-95450-176-2