INSTR 17 - Novosibirsk
Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid Argon Calorimeters

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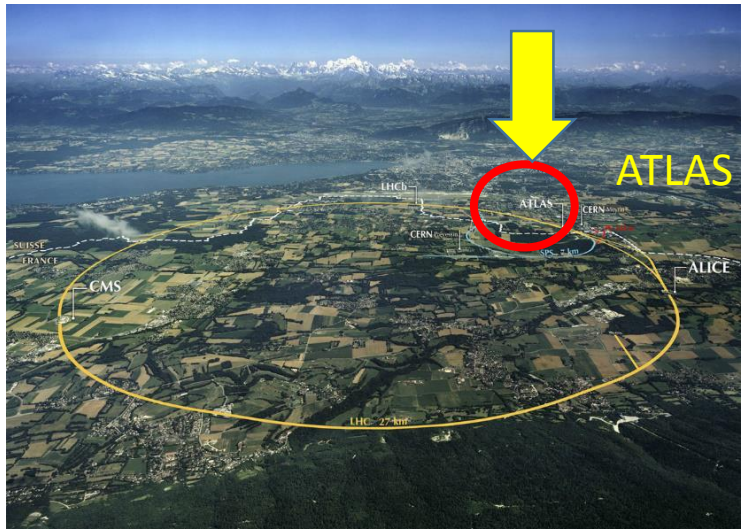
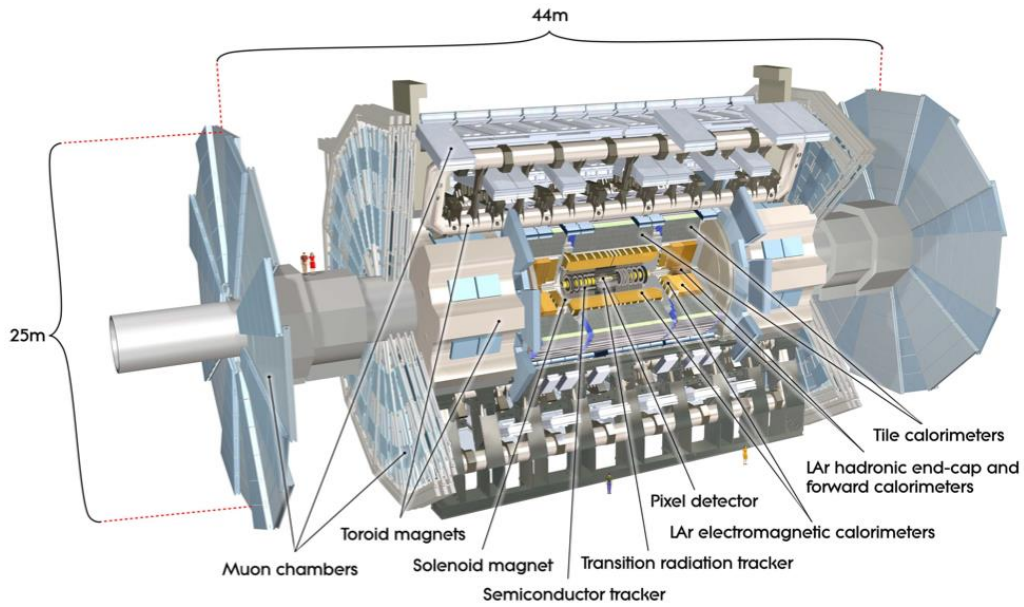
on behalf of the ATLAS Liquid Argon Calorimeter group

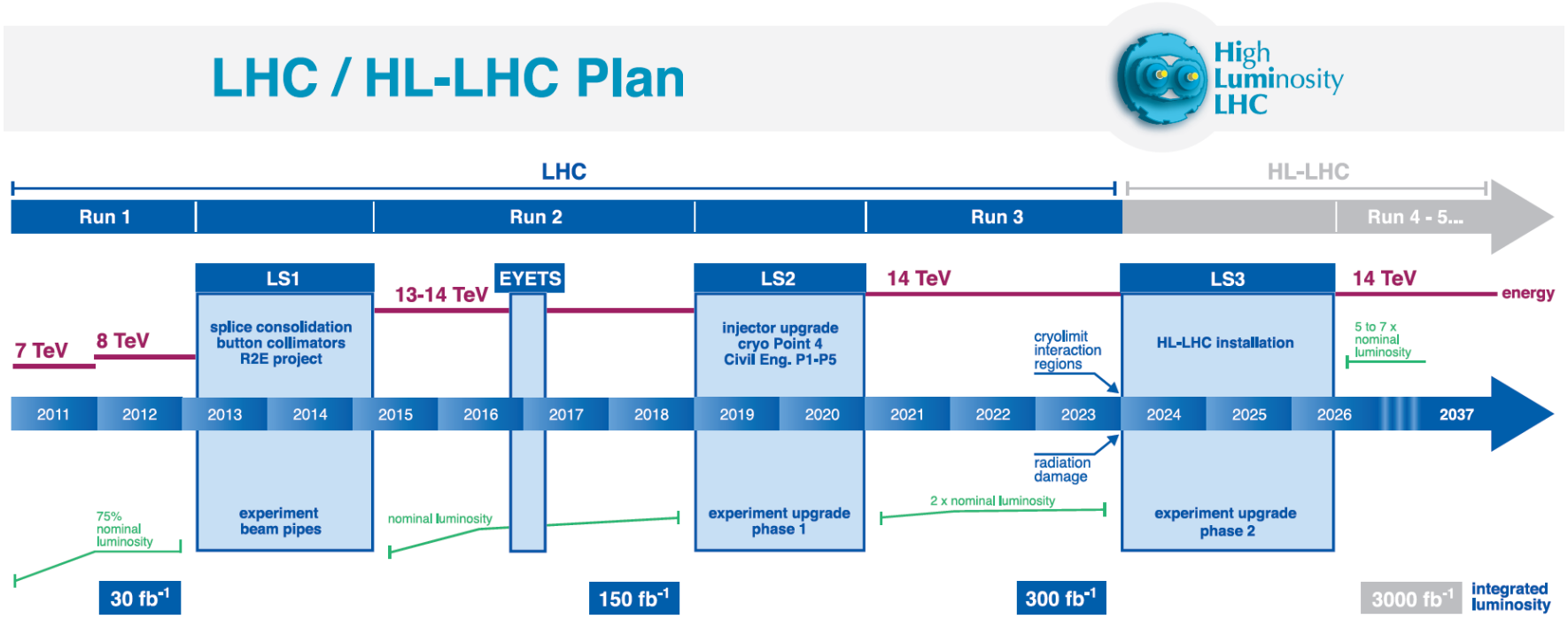
The ATLAS detector

- **Multi purpose detector**
- **Trigger based**
- **88 M readout channels**
  - ❖ **Pixels: 80.4 M**
  - ❖ **SCT: 6.3 M**
  - ❖ **Lar : 0.2 M**
  - ❖ **Muon : 1 M**
- **Dimensions**
  - ❖ **44 m x 25 m**
  - ❖ **7000 tons**





LHC schedule



Average number of vertices per bunch crossing

LS2: Phase-I Upgrade goals

- $\mathcal{L} \cong 3 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle\mu\rangle \cong 80$
- Keep trigger (max) 100 kHz; latency $\leq 3\ \mu s$

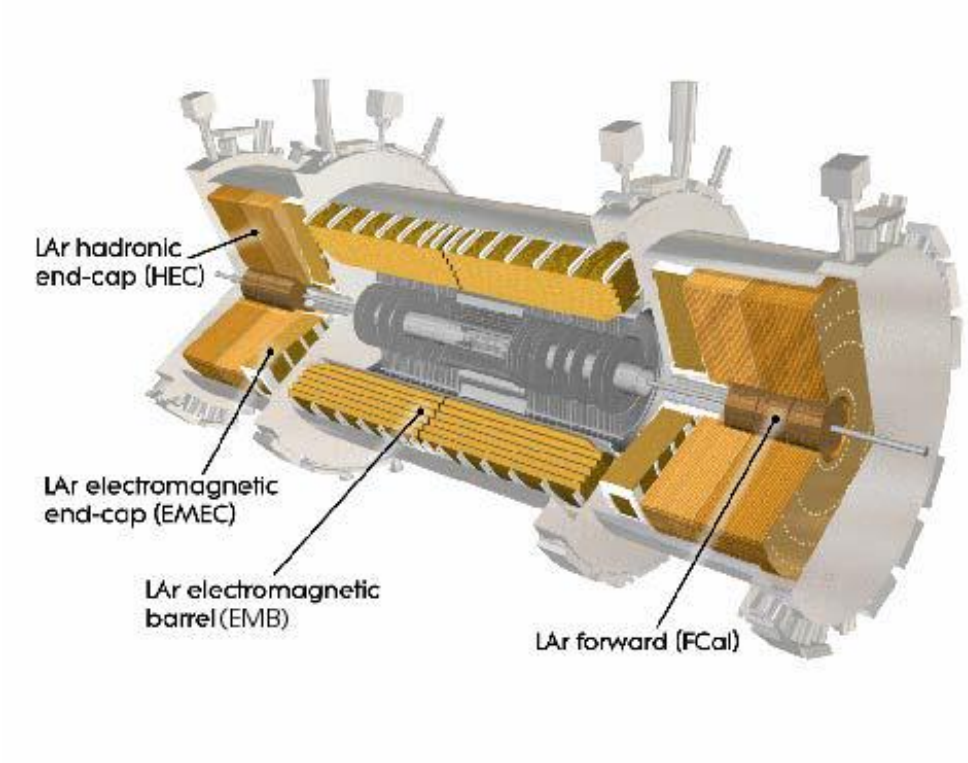
Upgrade of LAr trigger readout

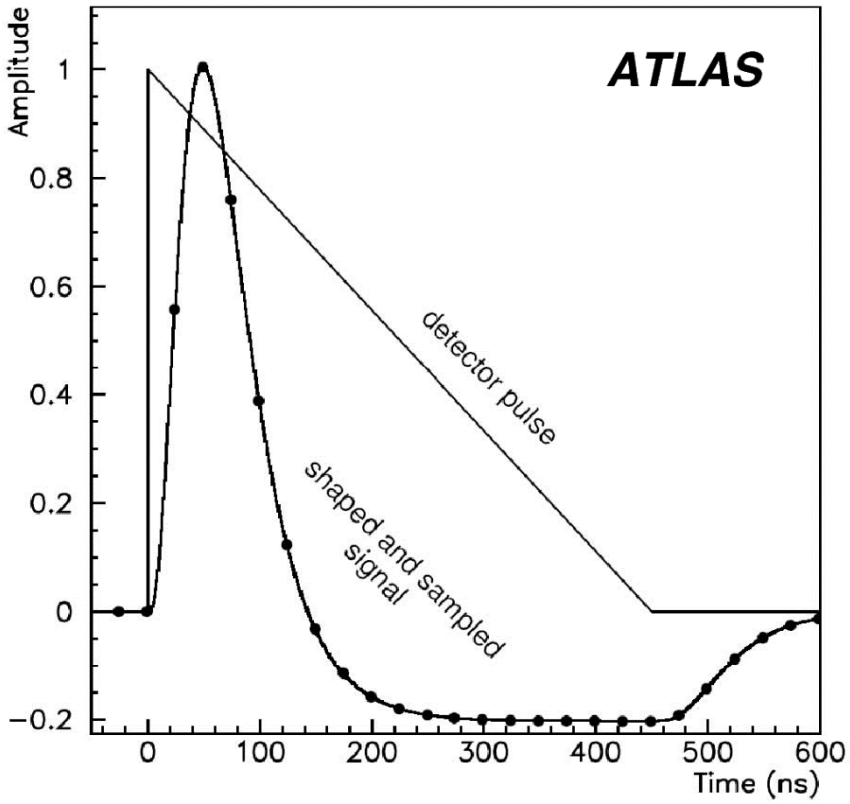
LS3: Phase-II Upgrade goals

- $\mathcal{L} \cong 7.5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle\mu\rangle \cong 200$
- Upgrade trigger to 1 MHz; latency $\leq 10\ \mu s$

Upgrade of LAr main readout*

The Liquid Argon Calorimeters





- ~ 200 k detector cells
- Energy reconstructed by pulse shaping and sampling
- Absorber : Lead/copper/tungsten Active: Liquid Ar

- 4 layers, different spatial resolution
- Connected to the Level-1 Trigger system
- 40 MHz sampling rate

The current electronics

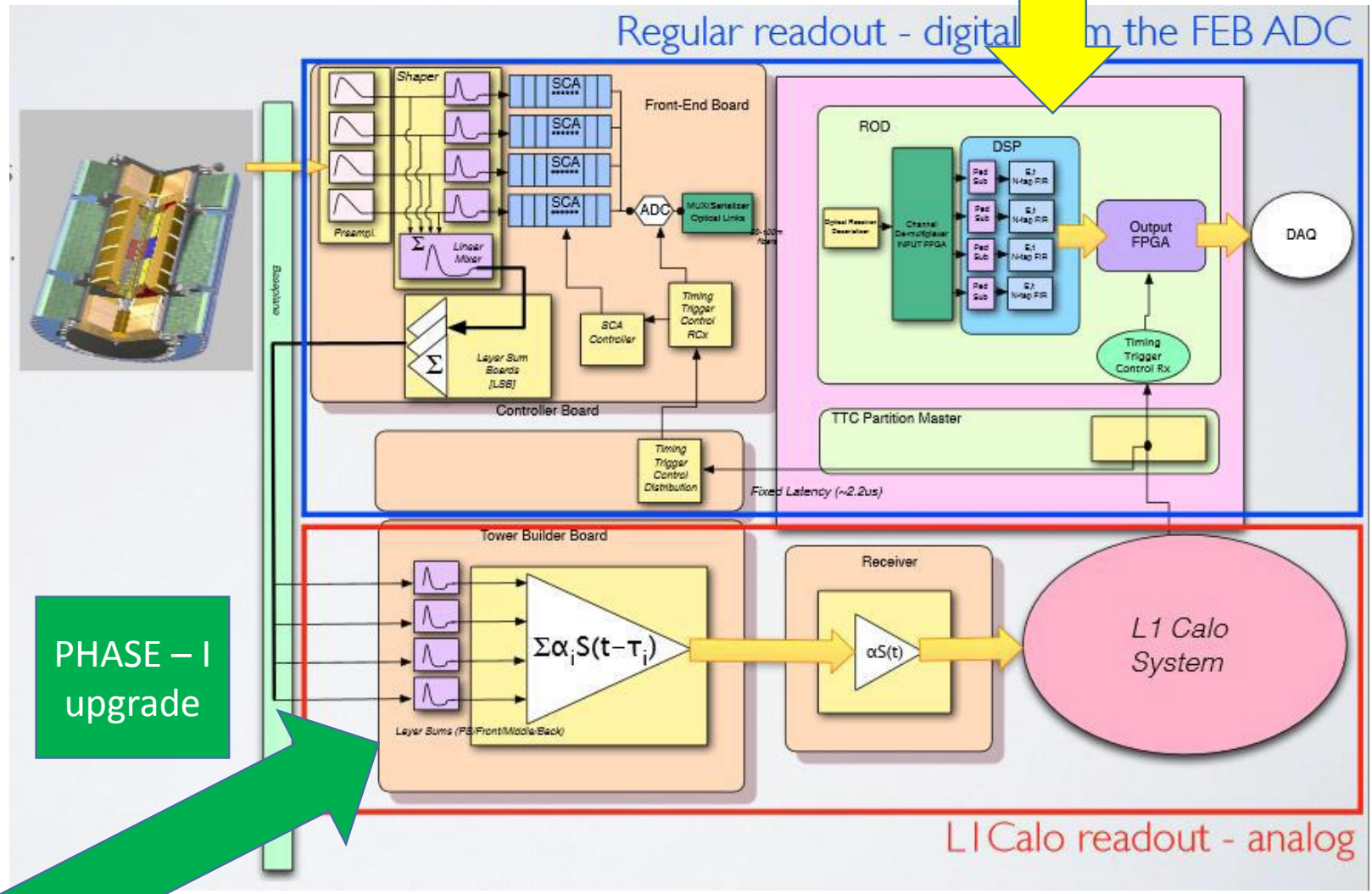
PHASE – II upgrade

- **Regular Readout**

❖ Amplification
❖ Shaping
❖ Analog pipeline
❖ Digitization upon L1 trigger (<100kHz)
❖ Data transmission (optical link)

- **Trigger readout**

❖ Summing signals on Layer Sum Boards
❖ Tower Builder boards sum analog Layer Sum Board signals in Trigger Tower to L1 calo

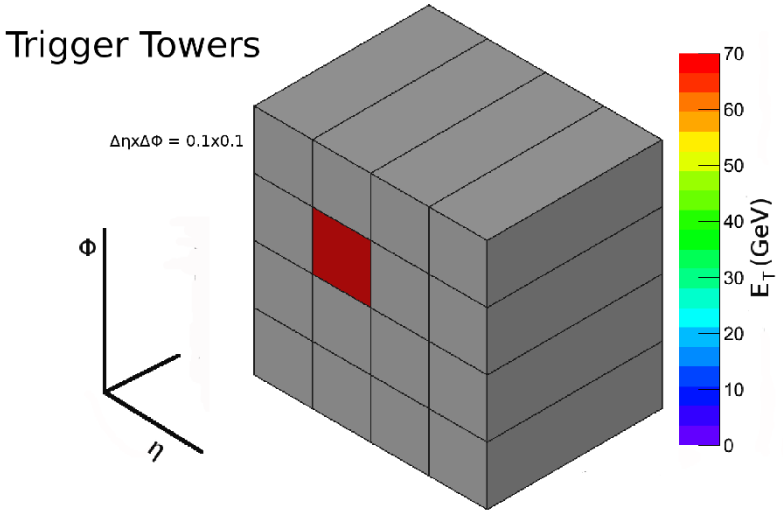


- **1600 Front End boards - 200 Readout Driver boards**

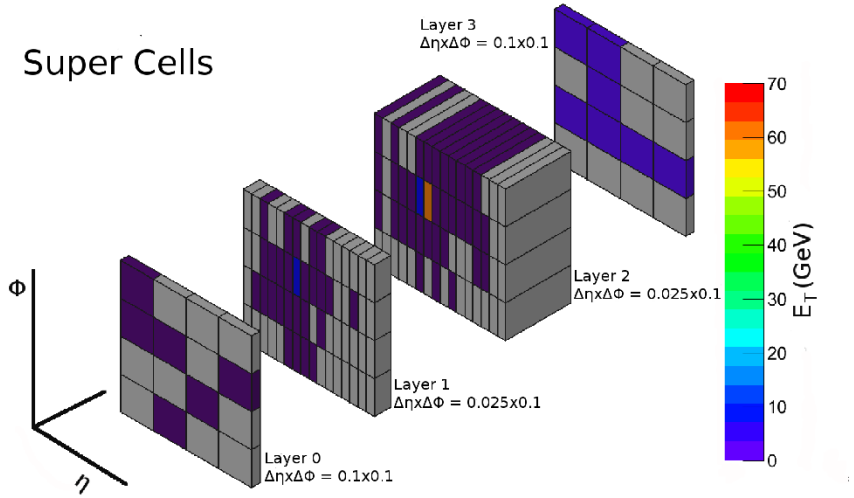
Phase – I upgrade

- **Phase 1 upgrade : concerns only the trigger path**
- **Current concept ➔ Trigger Tower: Transverse Energy (Et) summed over an area** $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
- **New concept ➔ Super Cell. Finer layer segmentation down to** $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$
  Keep layer information
- **Typically one Trigger Tower ~ 60 standards cells ~ 10 Super Cell**
- **Super Cell signals are digitized on the new LTDB boards ➔ Lar Trigger Digitizer Boards**

❑ **HIGHER GRANULARITY NEEDED TO KEEP THE SAME TRIGGER LEVEL DESPITE LUMINOSITY/PILE-UP INCREASE**



70 Gev electron shower
seen into only one Trigger Tower



70 Gev electron shower
seen into multiple Super Cells

Phase – I electronics upgrade

- **Trigger data flow becomes digital at Front-End level**

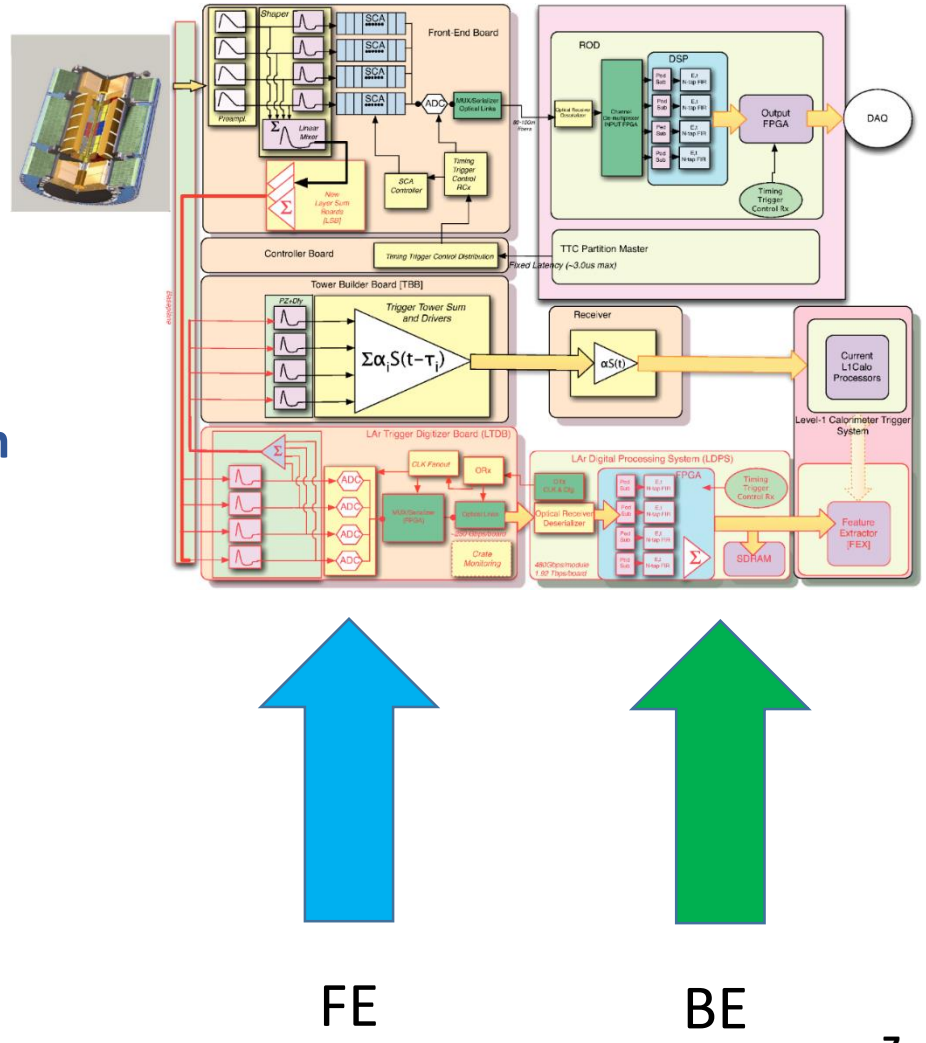
- **Front-End upgrade – ON-DETECTOR**

  - **Layer Sum Board (LSB): perform analog sums for super cells**
  - **Backplane update: keeps compatibility with existing setup**
  - **Lar Trigger Digitizer Boards (LTDB):**

    - ✓ **Super Cell signals are digitized @40 MHz ,**
    - ✓ **generate analog sums for compatibility with current system**
    - ✓ **send data to LDPB via optical links @ 5.12 Gbps**

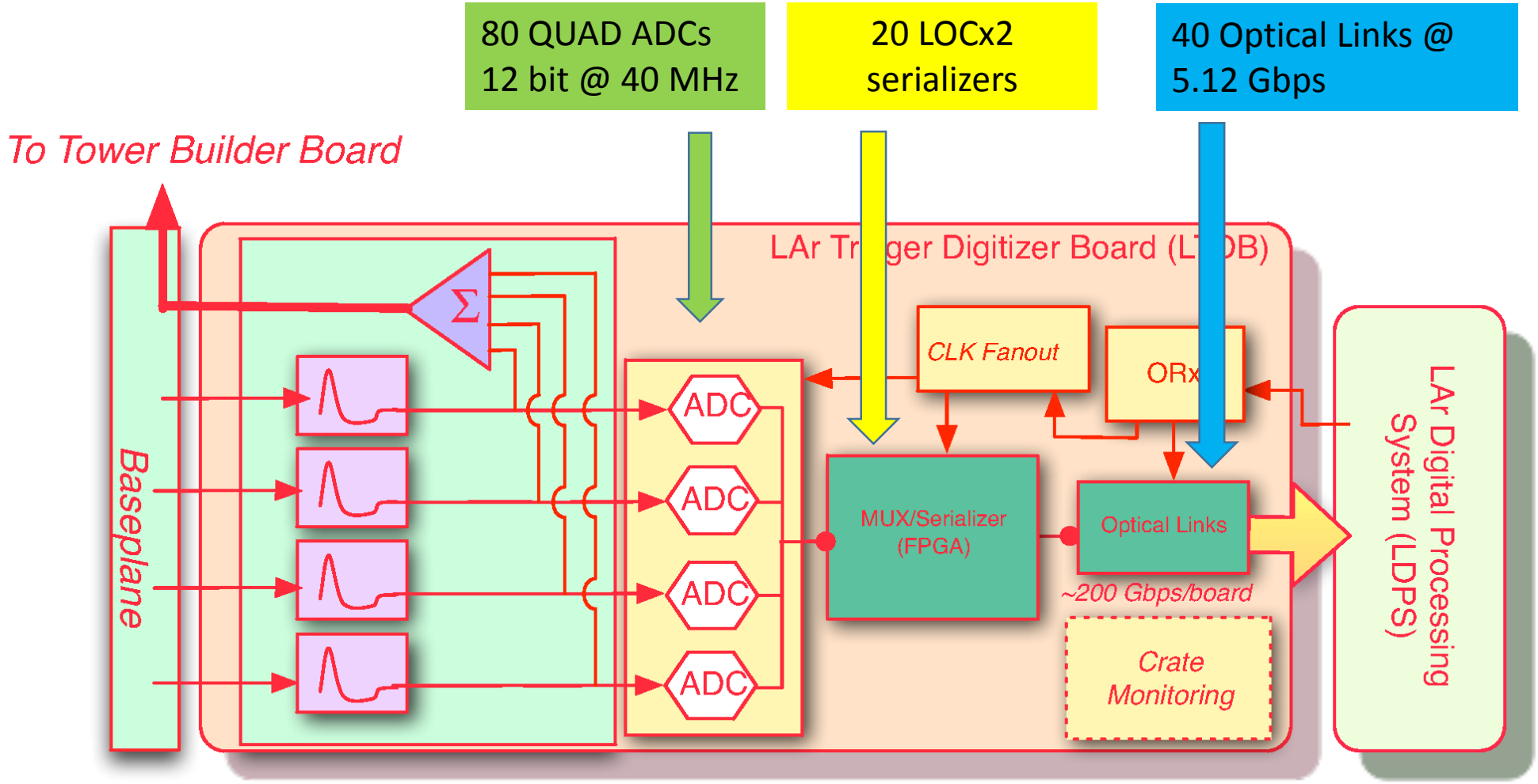
- **Back-End upgrade – OFF-DETECTOR**
  - **Lar Digital Processing Blade (LDPB)**

    - ✓ **Reconstruct the Super Cells transverse Energy**
    - ✓ **Sends the results to L1 Calo system @ 11.2 Gbps**



Front-End upgrade

- **An LTDB board processes 320 Super Cells ➔ 124 LTDBs cover the 34 k Super Cells**
- **Radiation tolerant ASICs**
  - **ADC**
  - **Serializer**
  - **Laser driver**
- **TTC clock : GBT links (Trigger and Timing)**
- **Phase – II Compatible**



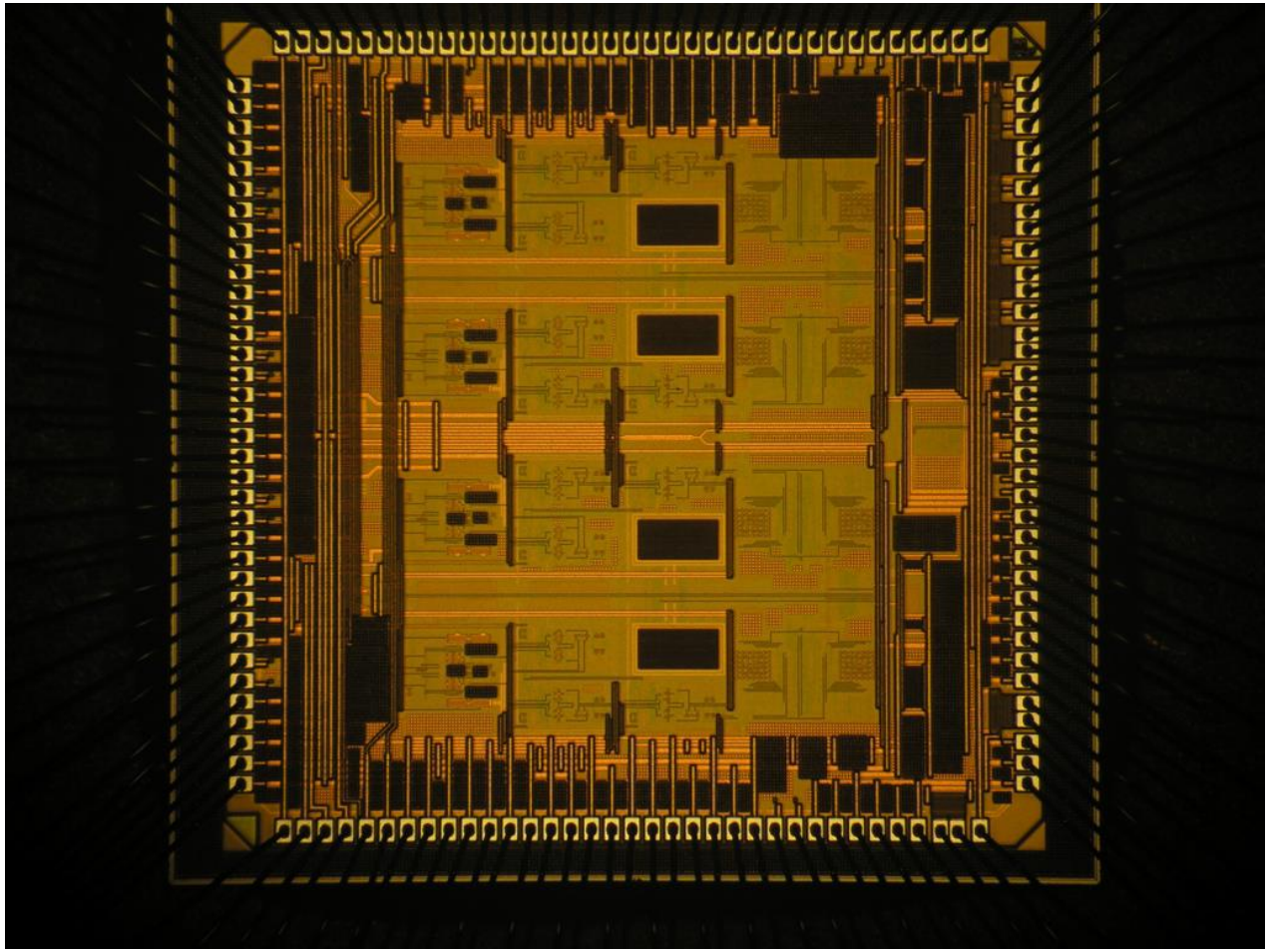
LTDB Block Diagram

Front-End upgrade LTDB - NEVIS ADC

- **QUAD channel**
- **40 Msps**
- **ENOB 11 bits**
- **Dynamic range**

Typically 11.8 bits

- **< 50 mW/channel**
- **112.5 ns latency**



3.6 x 3.6 mm

72 pins QFN

Global Foundry 8RF (130 nm CMOS)

Front-End upgrade
LTDB - NEVIS ADC – radiation tolerance

Table 1: Measurements of ADC performance before and immediately after irradiation in a 227 MeV proton beam at f_{in} = 10 MHz. The change in the ENOB is within the measurement errors of the testing setup.

Chip No.	Dose [MRad]	SNDR [dBc] Pre/Post-Irradiation	SFDR [dBc] Pre/Post-Irradiation	ENOB Pre/Post-Irradiation
1	2	62.43 / 61.05	67.27 / 70.06	10.08 / 9.85
2	1	63.54 / 62.36	70.92 / 72.98	10.26 / 10.10

TOTAL DOSE

- **1 Mrad is 10 times the dose expected in 4000 fb-1**

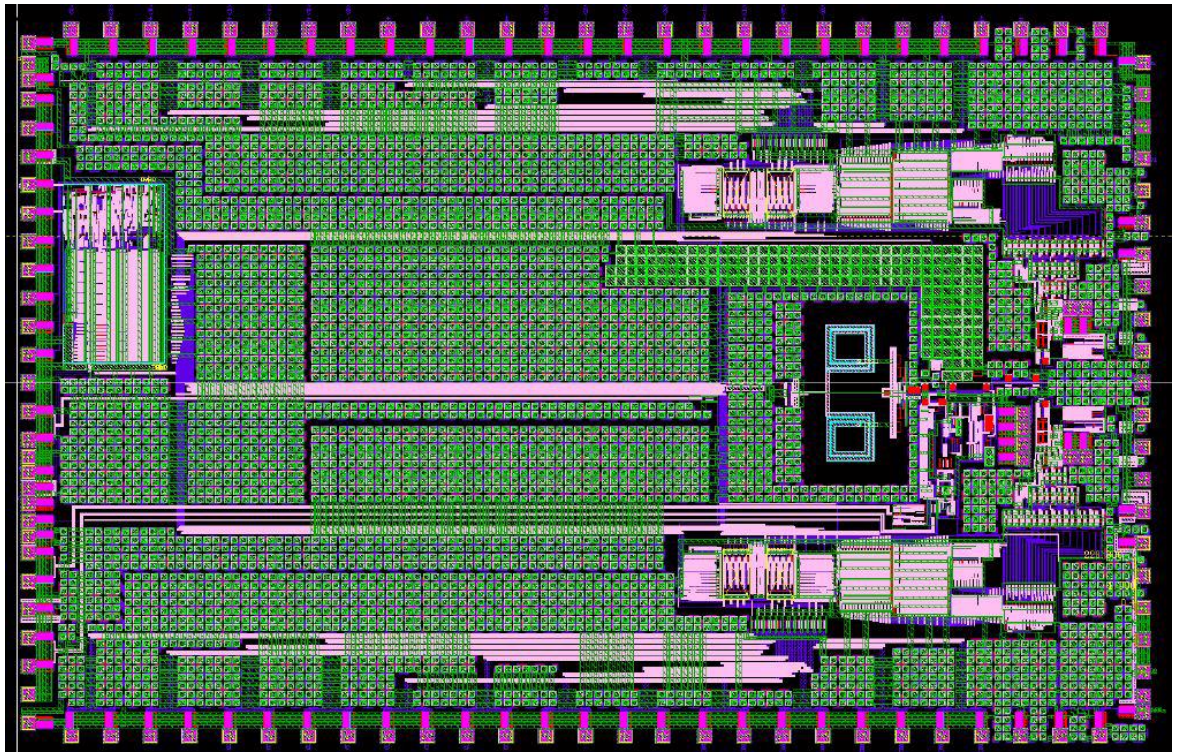
Table 2: Measurements of ADC SEE performance in a 227 MeV proton beam.

Chip No.	Rate [10^8proton/cm^2/s]	Dose [kRad]	SEFI	SEU (analog)	SEU (digital)	SEE	Cross section (w/analog errors) [10^{-12} cm^2]
3	19.0	101	0	8	1	12	0.6 (5.1 ± 1.8)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

SEE

Front-End upgrade LTDB - LOCx2

- **DUAL 8 x 14 bits serializer**
- **5.12 Gbps outputs**
- **Nevis ADC compatible**
- **Radiation tolerant**
- **1 W**
- **Fixed Latency < 75 ns**



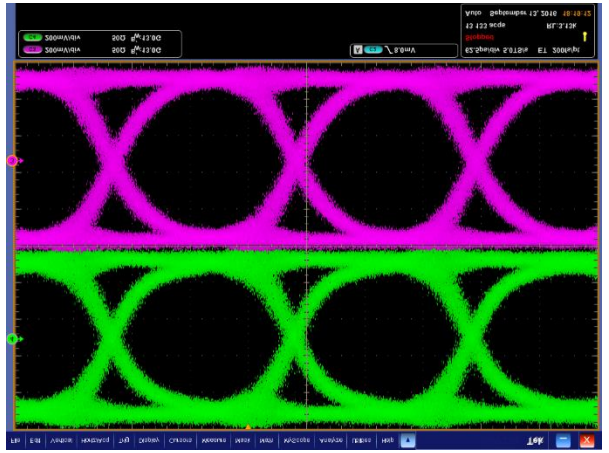
6.036 x 3.68 mm

100 pins QFN

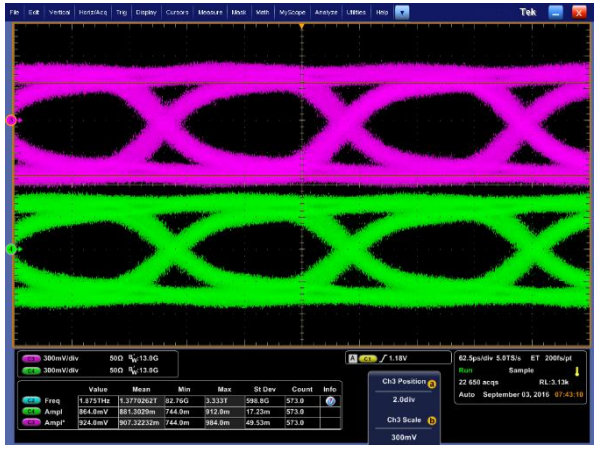
Silana Foundry **250 nm Silicon-on-Sapphire**

Front-End upgrade
LTDB - LOCx2 – tests – radiation tolerance

- **Eye Diagram 5.12 Gbps**
- **2 Channels chip soldered on PCB**
- **Total jitter ~ 50 ps (loop filter = 800 kHz)**

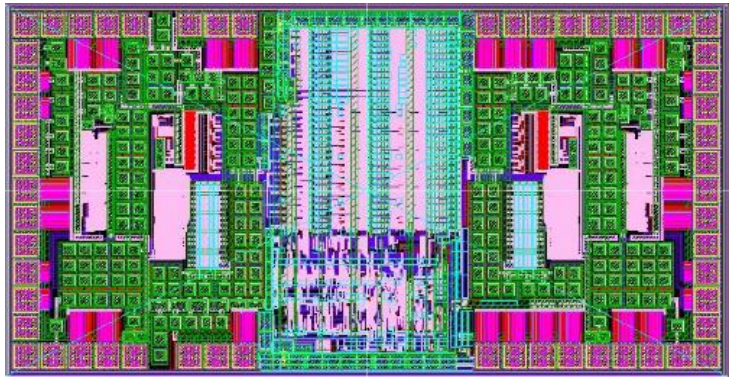


- **Eye Diagram after 182 krad TID**
- **Low or high dose rate (3krad/hr or 30 krad/h)**

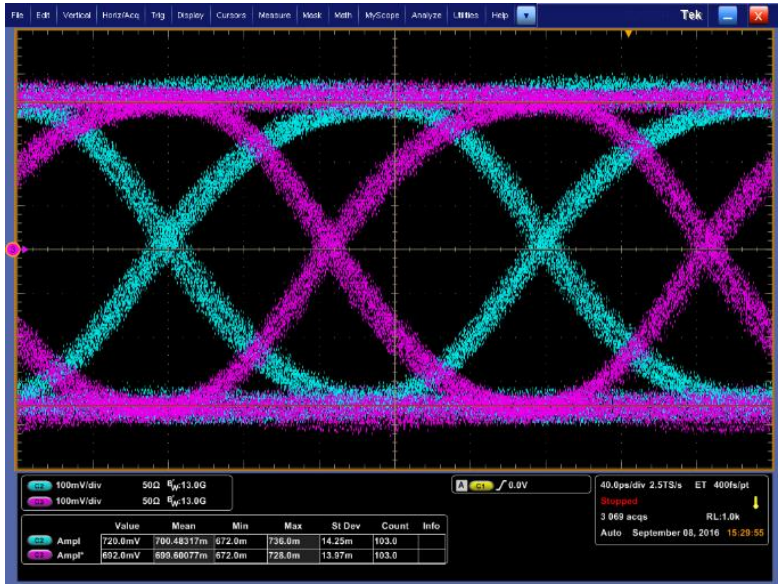


Front-End upgrade
LTDB – LOCID – tests – radiation tolerance

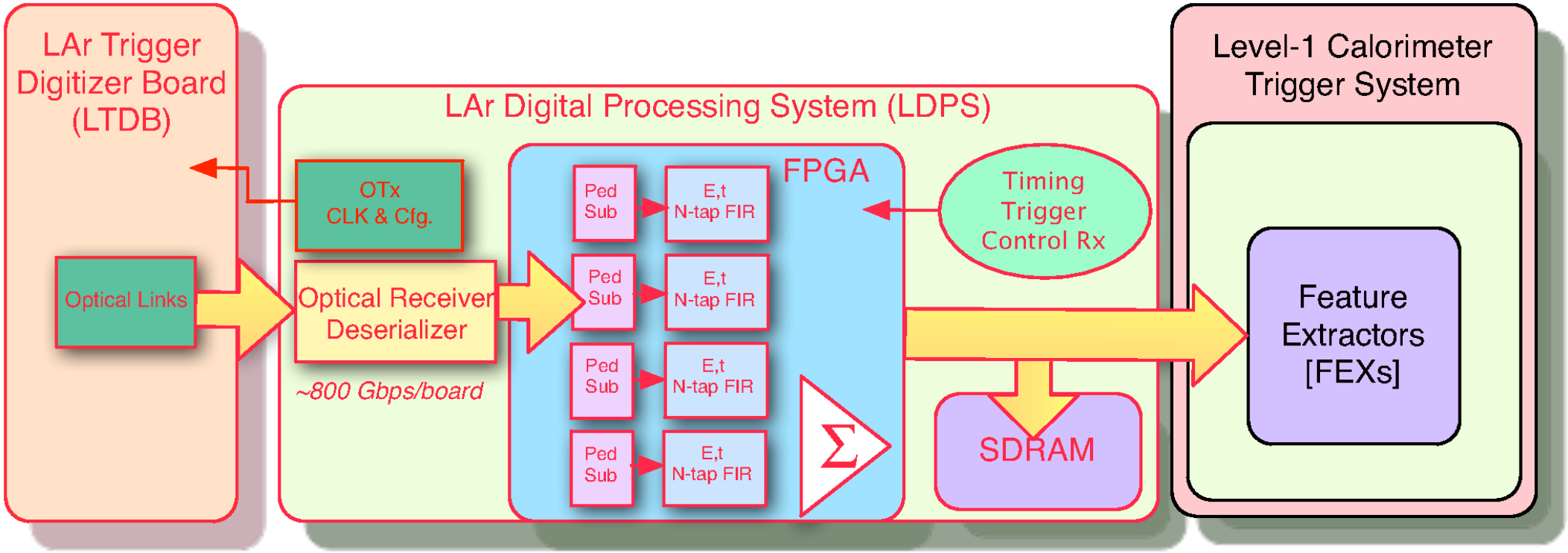
- **Dual channel VCSEL driver**
- **Radiation tolerant**
- **Die size: 2.114 x 1.090 mm**
- **40 pins QFN**



- **No eye diagram change after 200 krad**
- **2 channels shifted for display clarity**
- **Current change after irradiation < 10%**



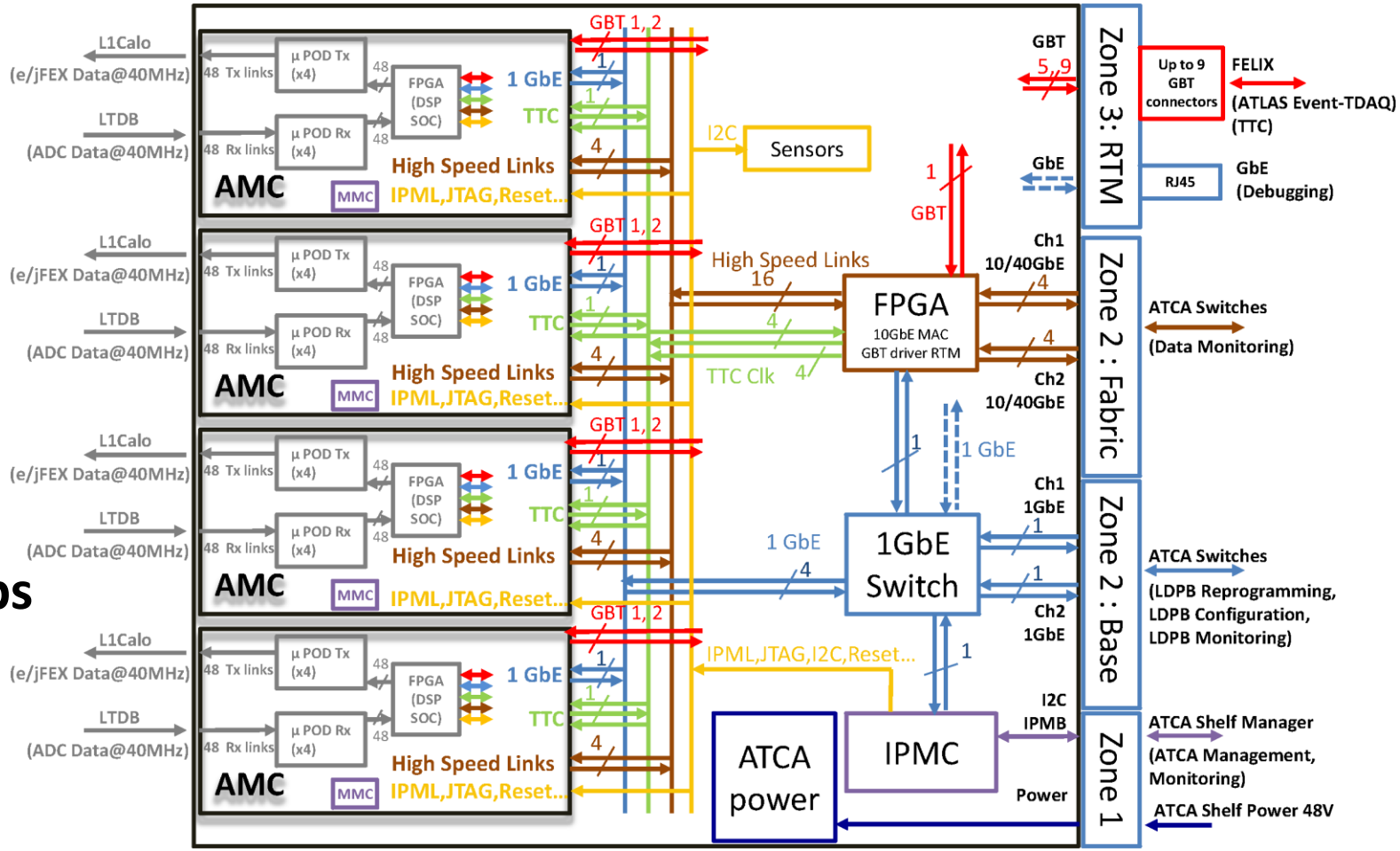
Back-End upgrade



LDPS Block Diagram

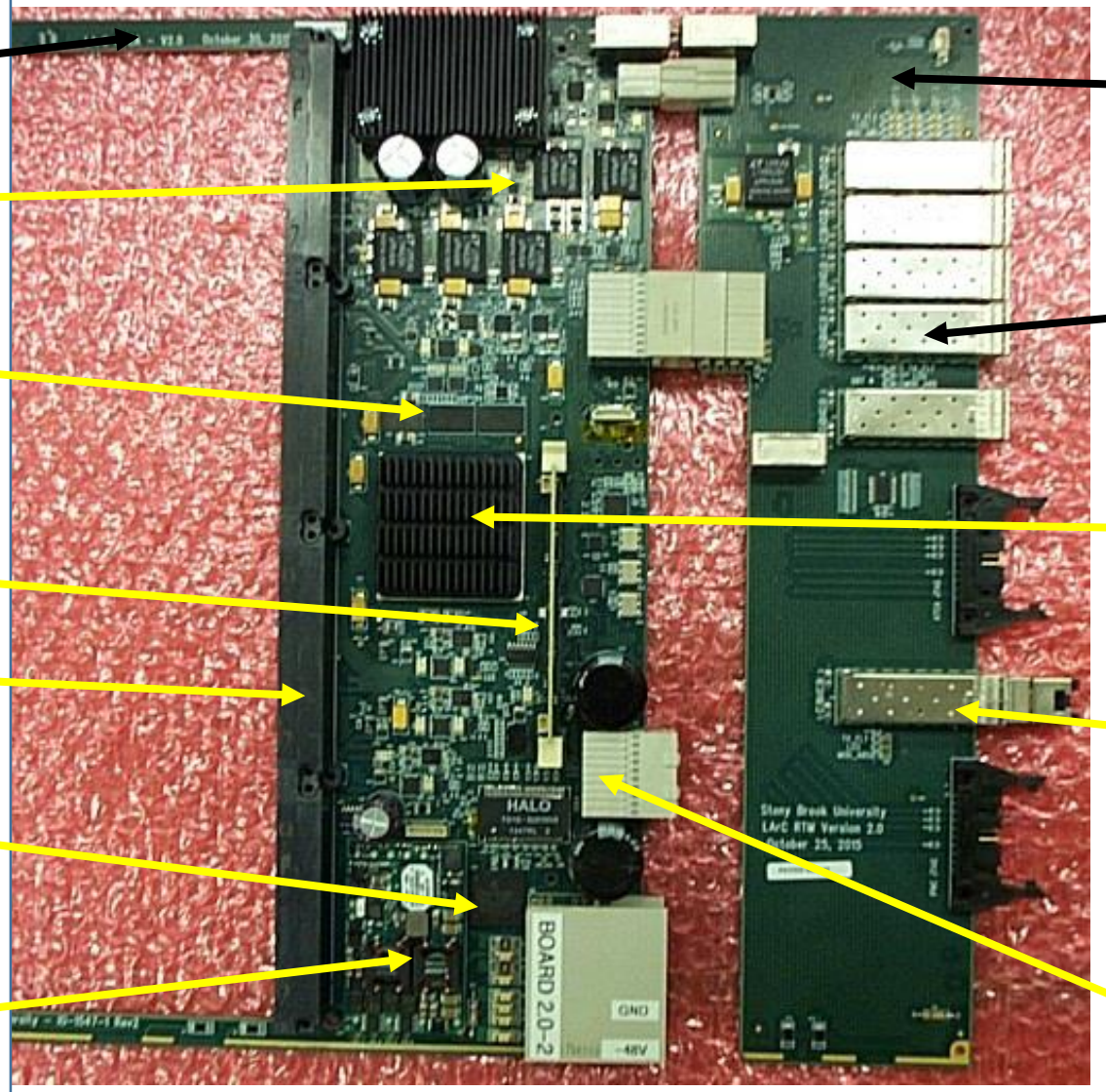
Back-End upgrade Lar Digital Processing System

- **LTDB : Processing Boards**
  - ❖ **A Carrier board**
  - ❖ **4 AMC mezzanine boards**
  - ❖ **192 input fibres @ 5.12 Gbps**
  - ❖ **192 output fibres @ 11.2 Gbps**
  - ❖ **Most recent FPGAs**



Total of 31 Processing Blades in 3 ATCA crates

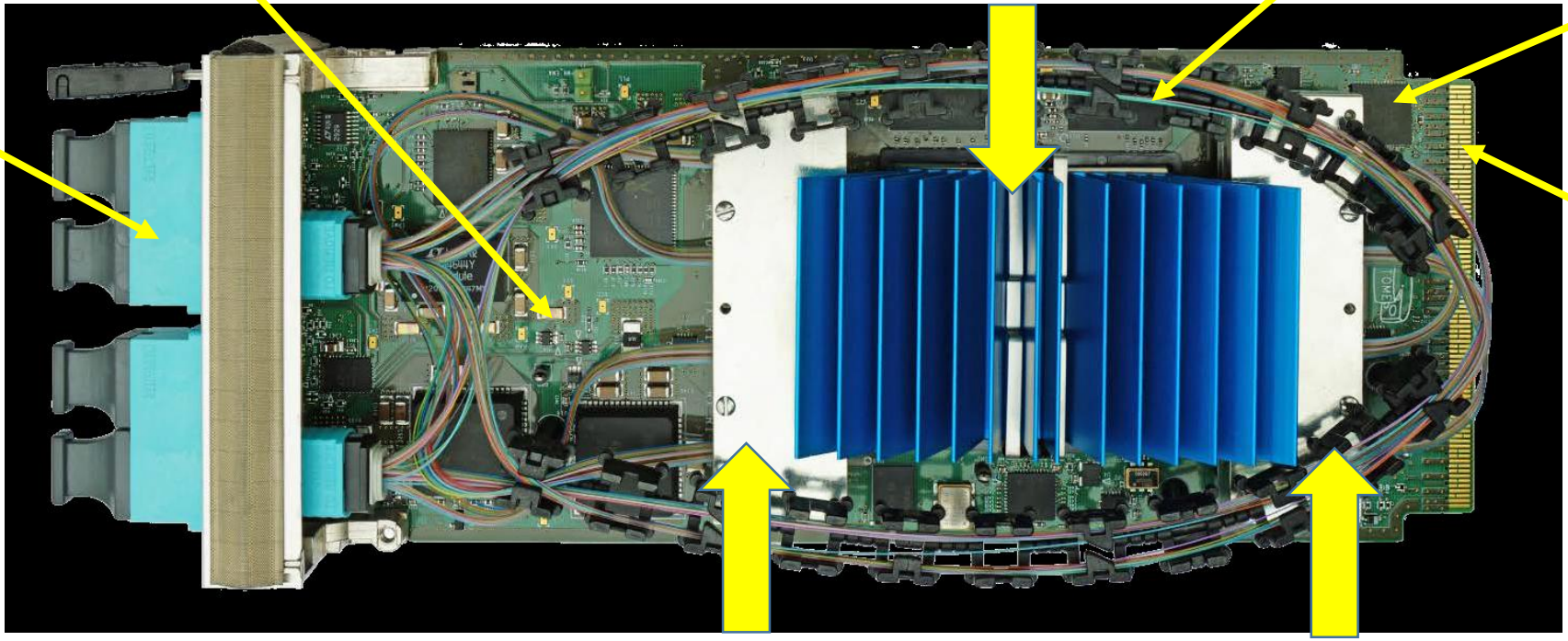
Back-End upgrade LDPB Carrier Board



Back-End upgrade LATOME- AMC board

- **Main DATA path**
  - ❖ **Receives Super Cells DATA from LTDB @5.12 Gbps on up to 48 optical links**
  - ❖ **Computes Super Cells transverse energy (E_T) using optimal filter**
  - ❖ **Builds trigger tower transverse energy**
  - ❖ **Sends trigger tower data @11.2 Gbps on up to 48 optical links**
  - ❖ **Sends Super Cell data to DAQ on L1A**
- **Receives Timing Trigger & Control clock (TTC) and data from the Carrier board**
- **Monitors data and sends report to TDAQ system upon request on 10 GbE network**
- **System has fixed latency less than 375 ns (15 BC)**

Back-End upgrade LDPB LATOME - Hardware



DC/DC blocks

ARRIA 10 FPGA
10 AX115R4F40
Under Heat sink

2 Gb DDR3 @800 MHz

MMC controller

MPO Fiber connectors

AMC interface

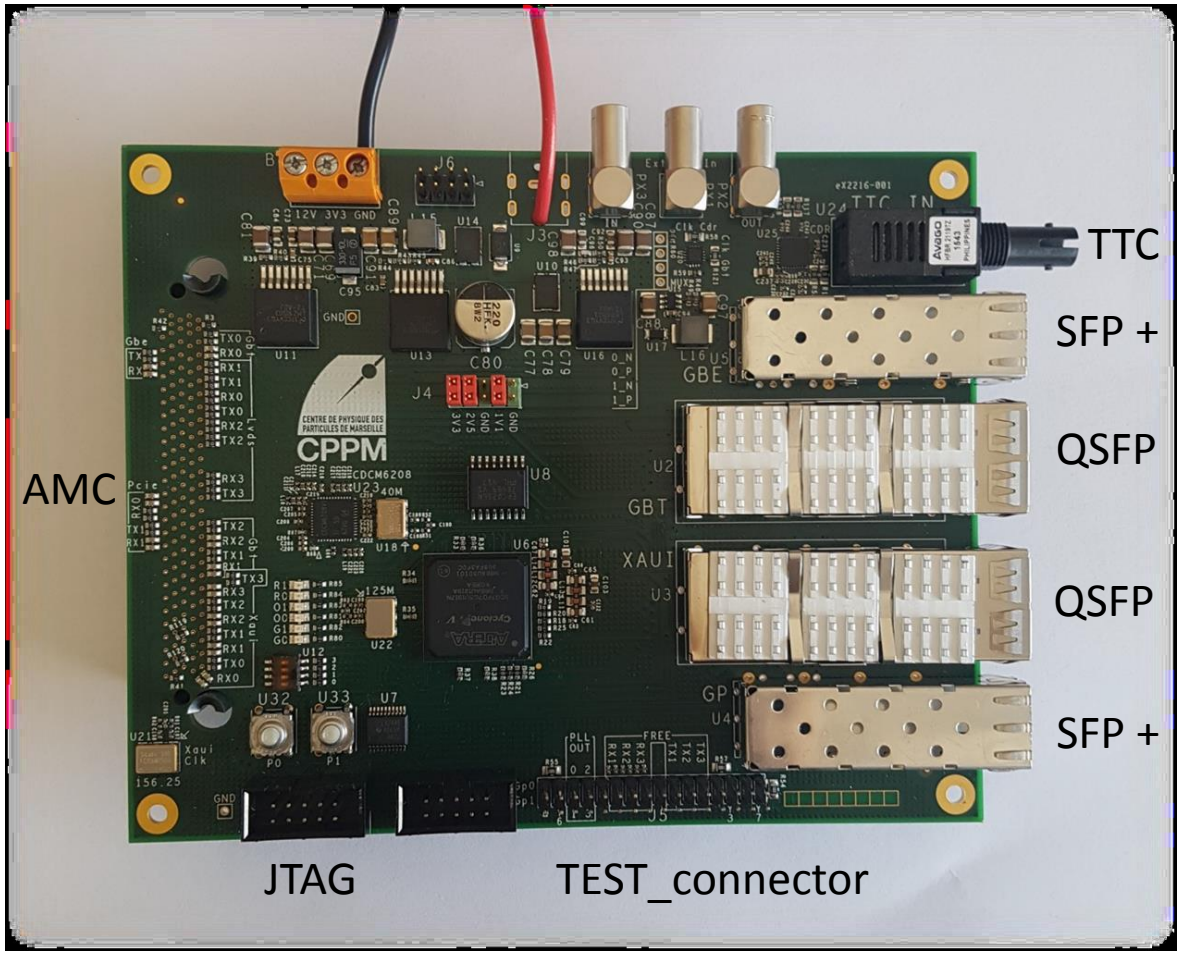
48 in from LTDB
@ 5.12 Gbps

48 out to L1
@ 11.2 Gbps

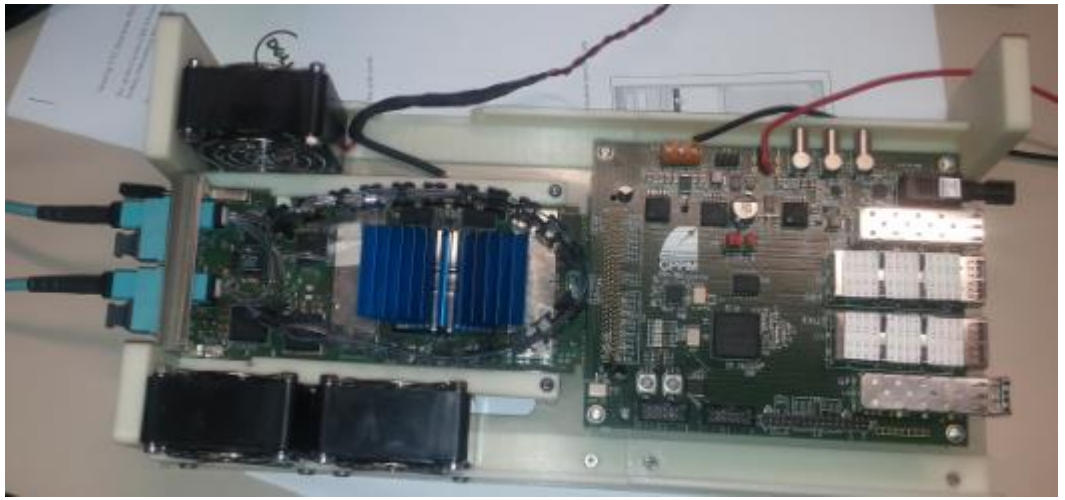
< 80 W

8 Avago uPODS (8 x 12 optical links)

Back-End upgrade LDPB LATOME_test Board



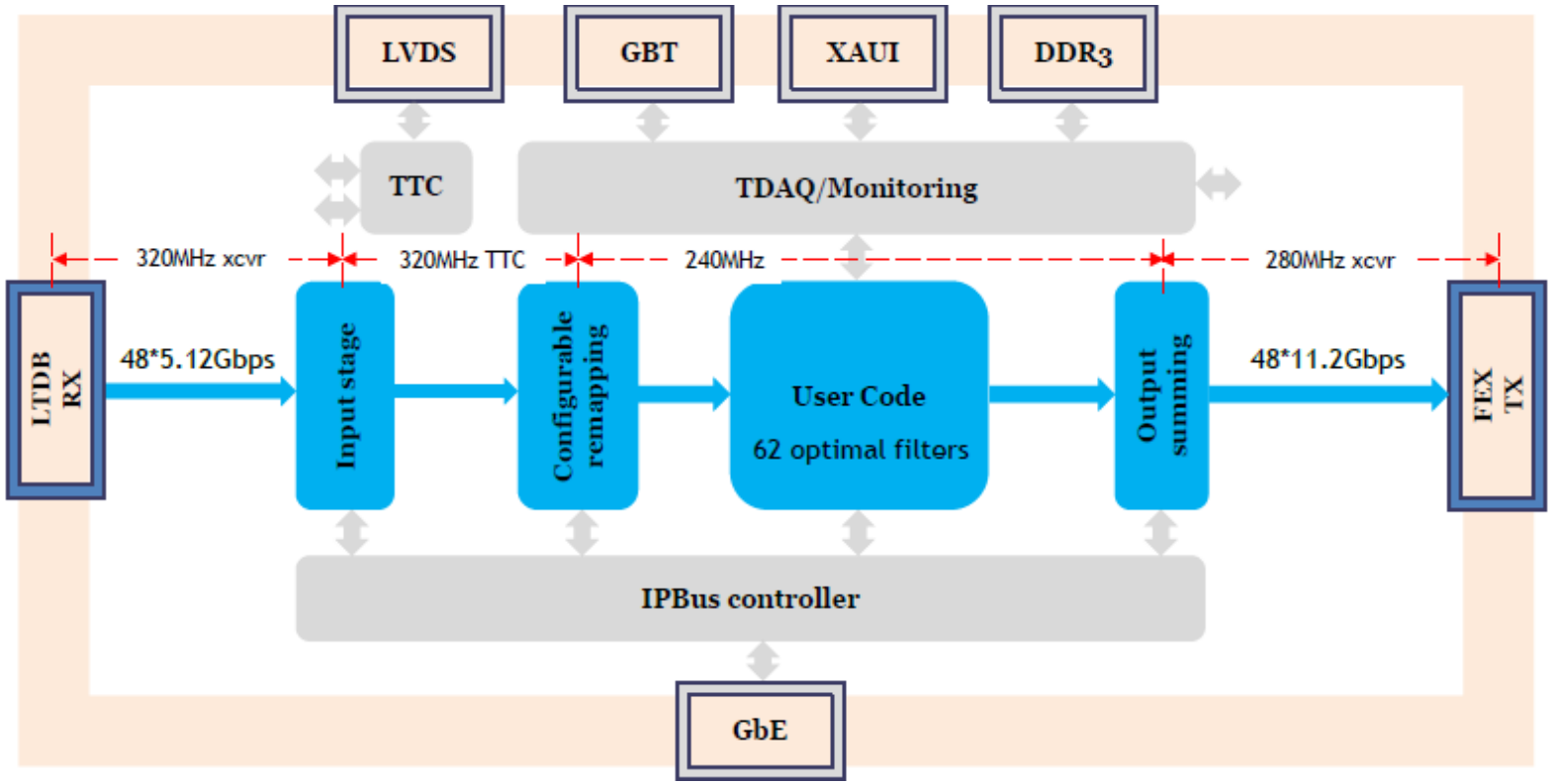
- **Dedicated test tool**
  - ❖ **Test the AMC boards**
  - ❖ **« Swiss knife » for various tests**



Mini_DAQ

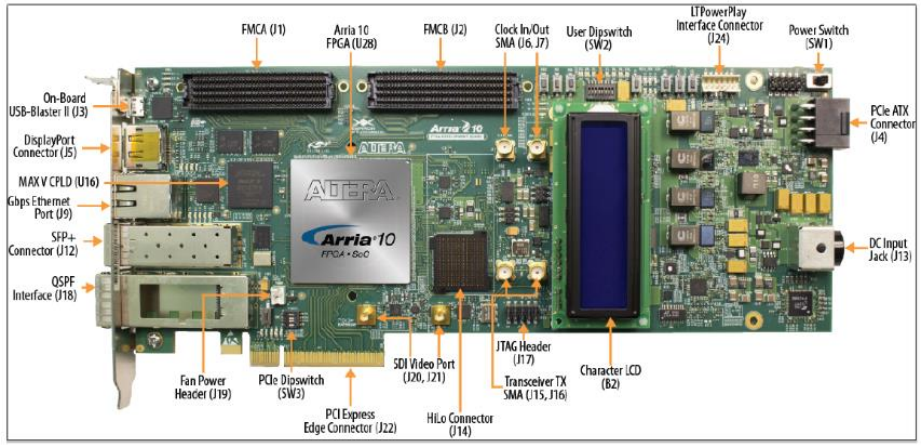
Back-End upgrade LDPB LATOME - Firmware

- **Input stage aligns all inputs to the same BCID**
- **Configurable remapping: reorders input data according to detector's topology**
- **User Code: computes Et and time using Finite Impulse Response filter (FIR)**
- **Output summing: builds trigger tower energies**

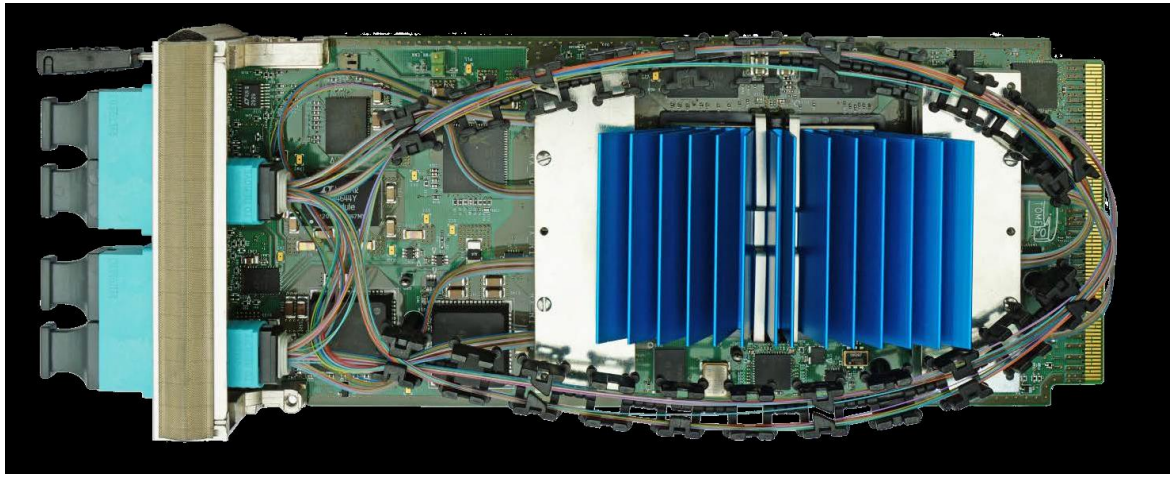


Back-End upgrade LDPB LATOME - Firmware

- **Huge effort ➔ 7 INSTITUTES**
- **Most of the code has been written and simulated**
- **Partial validation on :**



ARRIA 10 dev-kit ALTERA

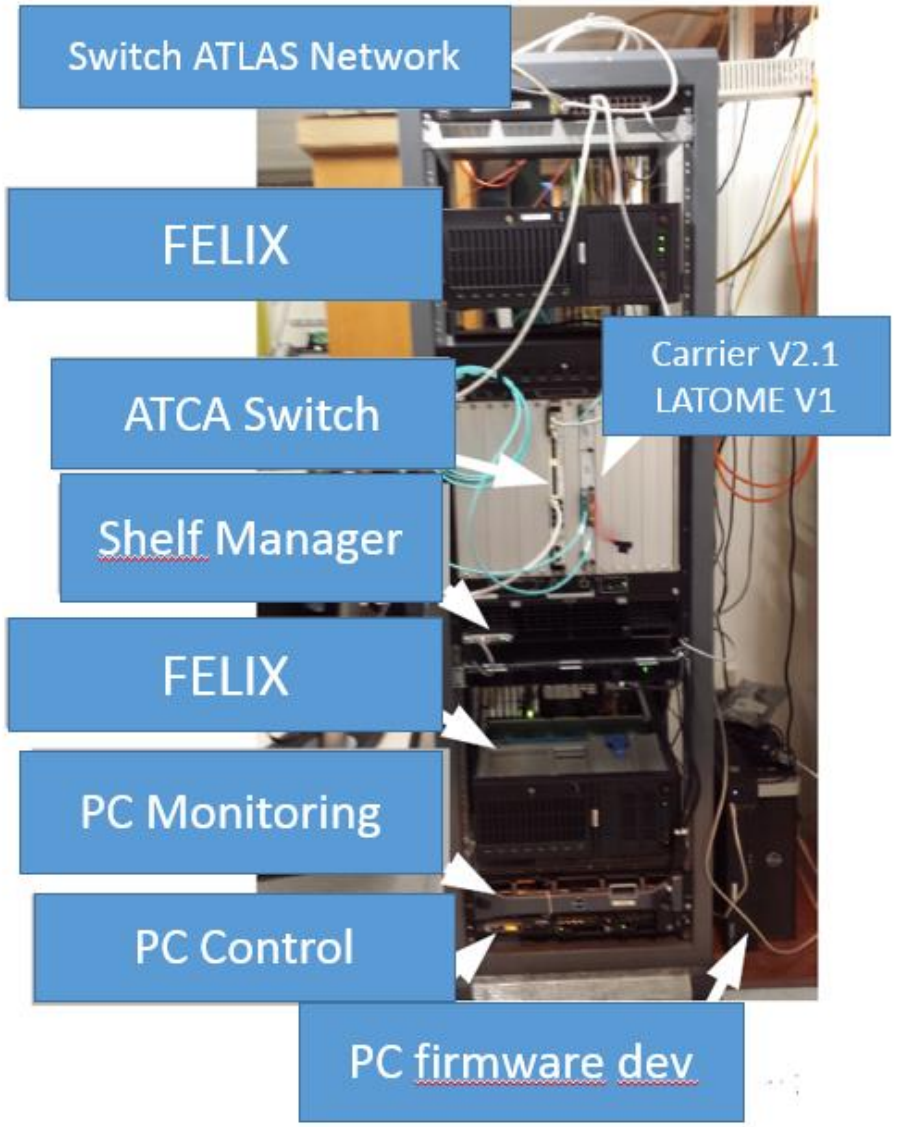


LATOME Board

- **Extensive System tests with Carrier boards and LATOME boards in Q1 2017 @ CERN**

Back-End upgrade LDPB LATOME – System Test

- **Connect to the real environment @ CERN**
  - TTC
  - ATLAS Network
  - Development PCs
- **First system test in march 2017**
  - Checks simple configuration
- **More system tests in Q2 2017**
  - Until fully functional
- **Production Readines Review**
  - Carrier boards and LATOMEs in 2017

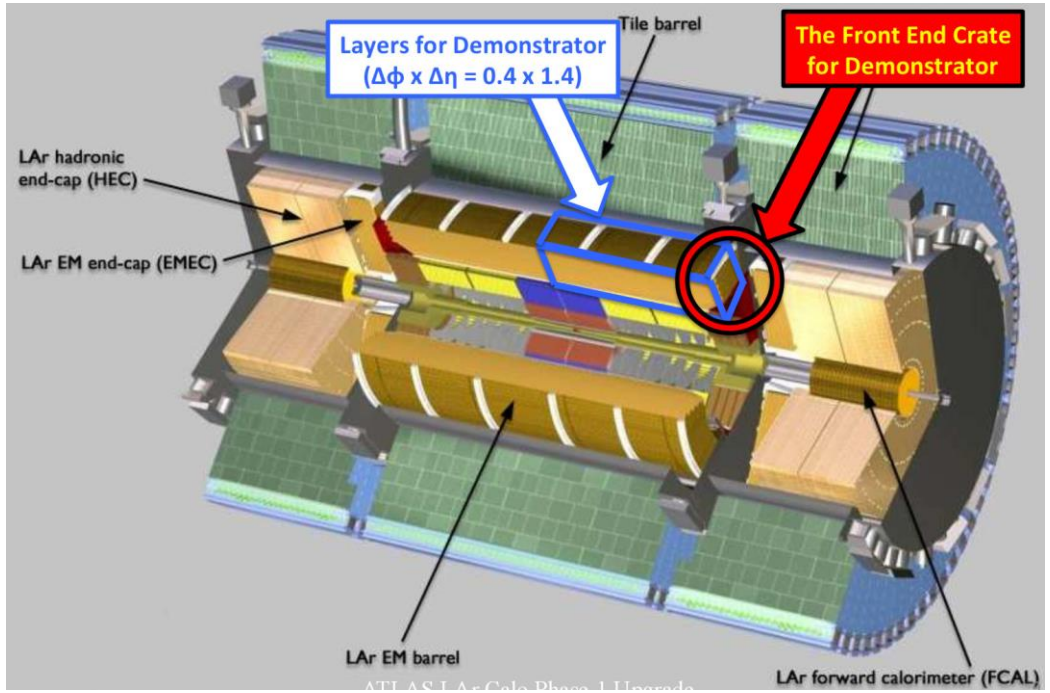


The Demonstrator

What are we doing while the upgrade is being produced ?

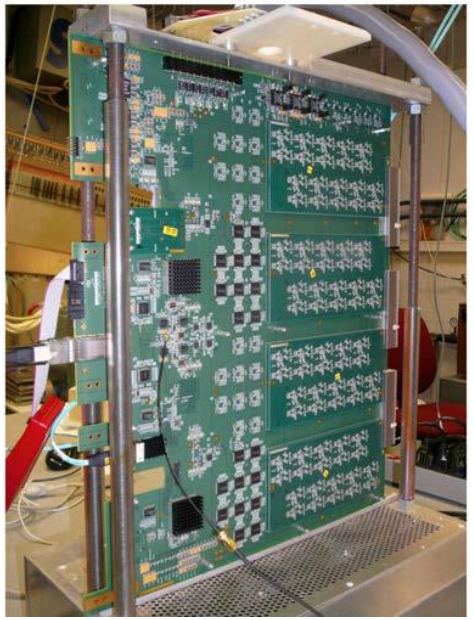
The Demonstrator - Motivation

- **Reads data from Super Cells**
- **Validates Energy reconstruction and bunch crossing identification**
- **Measures trigger efficiency and jet background rejection**
- **Gain experience in installation and operation of such equipment in the ATLAS environment**



The Demonstrator - LTDB

- **Handles up to 320 Super Cells signals**
  - ❖ **284 SCs in EM Barrel**
- **Super Cells digitized with 12 bit ADCs @40 MHz**
  - ❖ **Commercial COTS TI ADS5272 – not radiation tolerant**
- **Multiplexing 8 SC on one optical link @ 4.8 Gbps**
- **Throughput = 200 Gbps/LTDB**
- **Status**
  - ❖ **2 LTDBs demonstrators with different Architectures installed in August 2014**
  - ❖ **Taking collision data in LHC run 2**

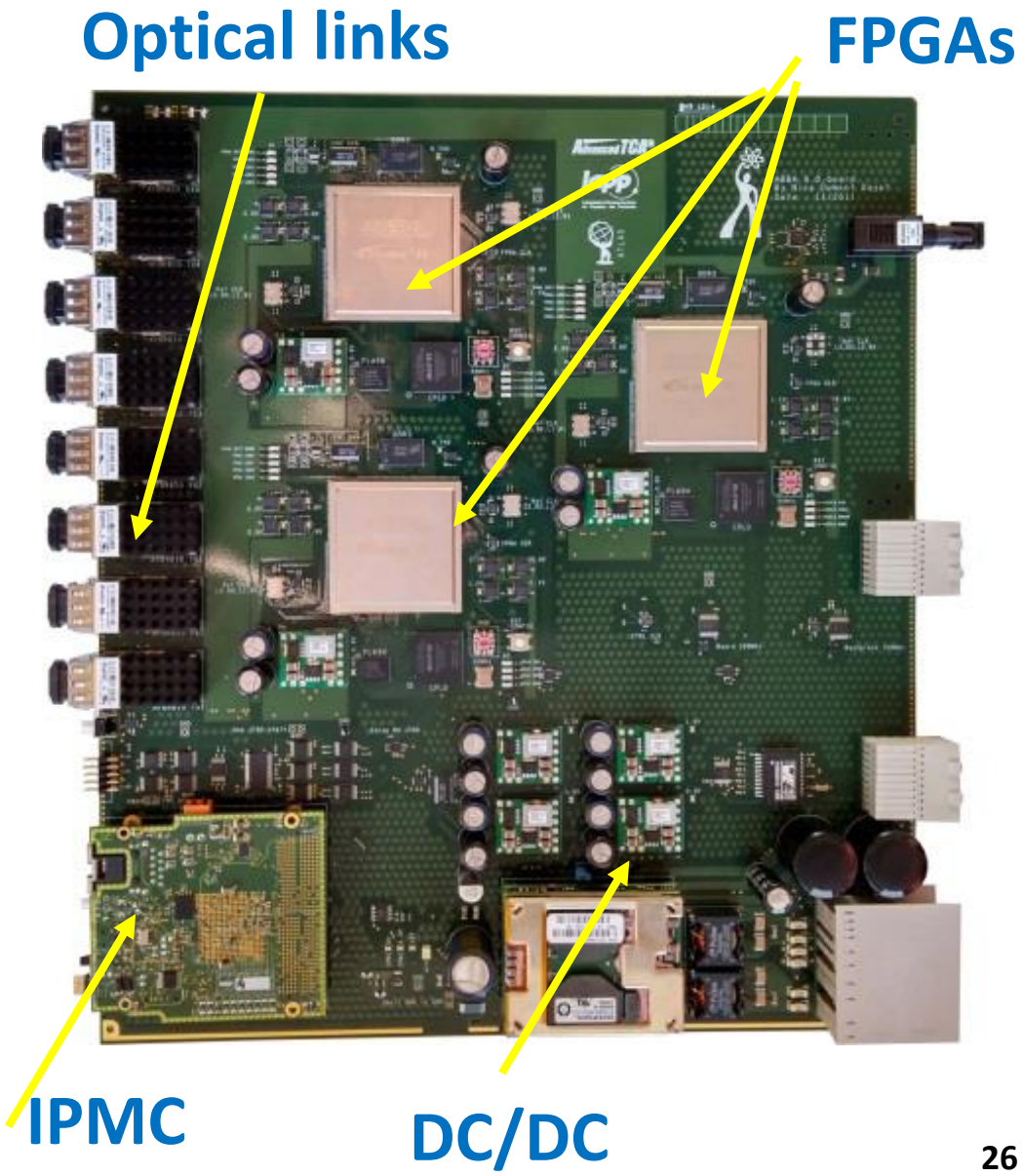


Digital MB + analog mezzanines

Analog MB + digital mezzanines

The Demonstrator – LDPB - ABBA

- ATCA board: 3 ALTERA FPGAs (Stratix IV)
- Receives up to 320 Super Cell data from one LTDB
  - ❖ 48 optical links @ 4.8 Gbps
- Stores Super Cells data in a circular buffer
  - ❖ Latency up to 2.5 us
- Waits for TTC trigger to readout Super Cells
  - ❖ Readout with filtered Level-1 trigger
- Readout through 10 GbE Ethernet network
  - ❖ Readout with ATCA fabric interface
- Status
  - ❖ 2 ABBA boards installed
  - ❖ Online software developped
  - ❖ Performs as expected



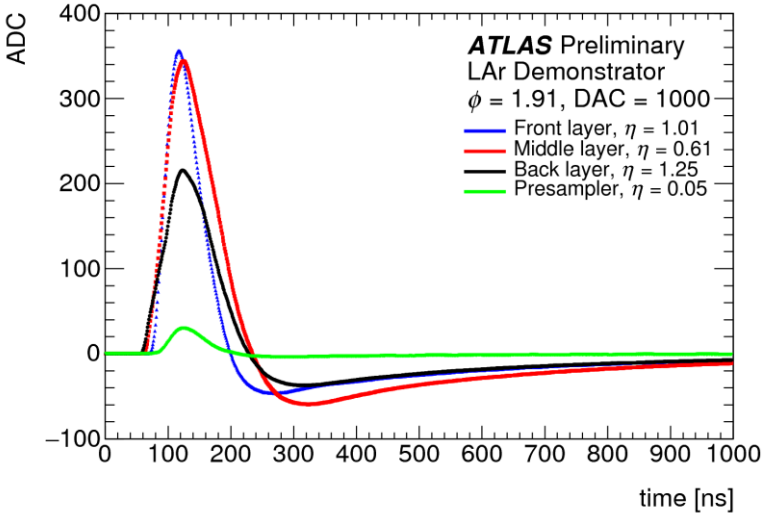
The Demonstrator - results

- **in calibration:**
  - electronic pulses sent by calibration board

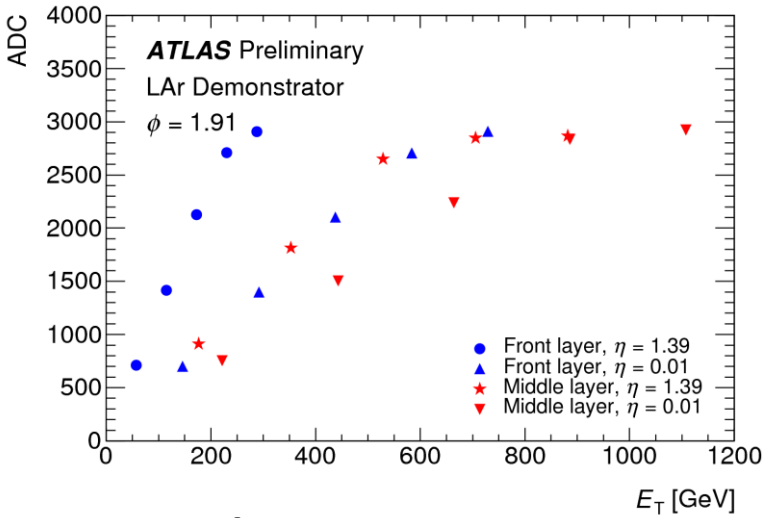
- **in collisions (proton-proton and heavy ion):**
  - collect data triggered in Demonstrator region
  - special L1Topo trigger item
  - compare Demonstrator readout and ATLAS main readout

  - ❖ Total noise on main readout of calorimeters cells of demonstrator (IO6) ~ neighboring crates

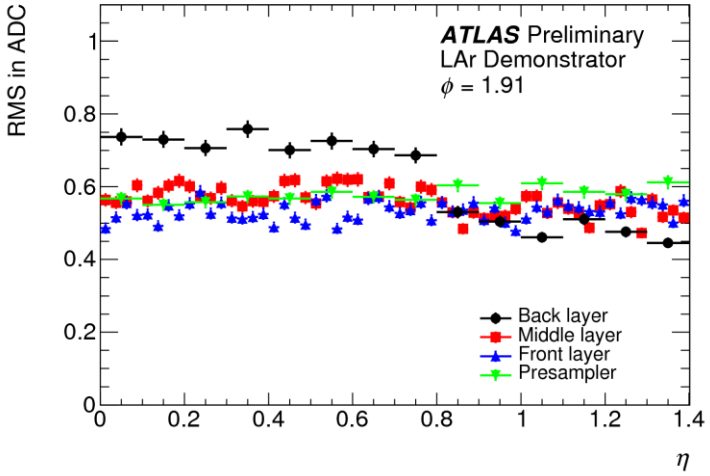
  - ❖ plan for early 2018 to have final prototype installed and running in end of Run 2



SC Pulse shape for each layer



Pulse max versus Et



Noise level of SC (< 250 MeV)

Conclusion

- **The ATLAS Lar calorimeter electronics will be upgraded after Long Shutdown 2 (2019-220)**
- **The trigger path will be digitized at Front-End level with an improved granularity**
- **Both Front-End and Back-End electronics will be new**
- **This huge effort involves the design of :**
  - ❖ **radiation tolerant ASICs (FE)**
  - ❖ **Most recent and powerful FPGA systems (BE)**
- **A demonstrator system has been installed in 2014 on a front-end crate**
  - ❖ **Works without disturbing the current system**
  - ❖ **All the results validate the concept of this upgrade**
- **LTDB and LDPS systems are being developped and tested**
  - ❖ **Production will start in 2017 – 2018**
- **Phase-I upgrade will be followed by Phase-II (installation in 2024-2026) ➔ Gustaaf BROOIJMANS talk**