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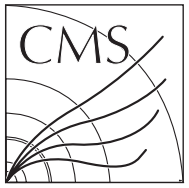

**The Compact Muon Solenoid Experiment**

# Conference Report

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# Level-1 track trigger for the upgrade of the CMS detector at HL-LHC

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**Abstract**

The Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) studies proton-proton collisions at a centre-of-mass energy of 13 TeV. With the LHC colliding proton bunches every 25 nanoseconds, the volume and rate of raw data produced by the detector are much larger than what can be read out, recorded, and reconstructed. Therefore, an efficient trigger system is required to identify events of interest in real time and to reduce the rate of events to a manageable level for later software reconstruction. The CMS trigger system consists of two processing stages, a level-1 (L1) hardware trigger and a high level software trigger. The current L1 trigger decision relies solely on calorimetric and muon system information. During the High Luminosity LHC (HL-LHC) era, the instantaneous luminosity of the collider is expected to increase by approximately an order of magnitude, resulting in a significantly larger number of collisions per bunch crossing than observed in the current run. In order to preserve physics performance under such highly challenging conditions, the L1 trigger system must be upgraded to accommodate the use of silicon tracker data. A new CMS L1 Tracking Trigger will reconstruct tracks with transverse momentum above 2 GeV/c at the LHC bunch crossing rate and within a tight latency budget of approximately 4 $\mu$s. In this article we provide an overview of the three architectures currently studied by the CMS collaboration for the future L1 Track Trigger system.

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PROCEEDINGS OF SCIENCE

# Level-1 track trigger for the upgrade of the CMS detector at HL-LHC

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The Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) studies proton-proton collisions at a centre-of-mass energy of 13 TeV. With the LHC colliding proton bunches every 25 nanoseconds, the volume and rate of raw data produced by the detector are much larger than what can be read out, recorded, and reconstructed. Therefore, an efficient trigger system is required to identify events of interest in real time and to reduce the rate of events to a manageable level for later software reconstruction. The CMS trigger system consists of two processing stages, a level-1 (L1) hardware trigger and a high level software trigger. The current L1 trigger decision relies solely on calorimetric and muon system information. During the High Luminosity LHC (HL-LHC) era, the instantaneous luminosity of the collider is expected to increase by approximately an order of magnitude, resulting in a significantly larger number of collisions per bunch crossing than observed in the current run. In order to preserve physics performance under such highly challenging conditions, the L1 trigger system must be upgraded to accommodate the use of silicon tracker data. A new CMS L1 Tracking Trigger will reconstruct tracks with transverse momentum above 2 GeV/c at the LHC bunch crossing rate and within a tight latency budget of approximately 4 $\mu$s. In this article we provide an overview of the three architectures currently studied by the CMS collaboration for the future L1 Track Trigger system.

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## 1. Introduction

During the High Luminosity [1] running phase, the LHC collider is expected to reach instantaneous luminosities of up to 5-10 $\times$ $10^{34}$ $cm^{-2}s^{-1}$. This translates into an average of about 140-200 overlapping proton-proton collisions (pileup) in each LHC bunch crossing. Even with the increase in the L1 accept rate to around 750 kHz for the upgraded system, momentum thresholds for basic physics objects (electrons, muons, jets, etc.) will need to be significantly increased if silicon tracker data is not used at the L1 trigger level. Silicon based tracking is known from HLT and offline reconstruction to be a very effective tool in pileup mitigation. Therefore, in order for CMS to maintain its physics performance during the high luminosity phase, the L1 trigger system needs to be upgraded to accommodate the use of silicon tracker data.

Tracking at L1 is challenging due to the high data rates and tight latency requirements imposed. L1 operation will become feasible in CMS through the special design of the outer tracker modules, which include two layers of silicon sensors separated by few millimeters. By correlating charged particle hit positions in the top and bottom layers, these $p_T$ modules will discriminate hits originating from high and low transverse momentum particles and transmit charged particle hits above a certain $p_T$ threshold for every bunch crossing. Data rates can be reduced by approximately an order of magnitude by suppressing L1 readout of hits from tracks below a certain transverse momentum threshold. The threshold is programmable, with an anticipated baseline of 2 GeV/c. Pairs of hits from the two sensors in a given module consistent with a track above the programmed $p_T$ threshold are known as stubs.

The tracking trigger will have approximately 4 $\mu$s to reconstruct and deliver L1 tracks to a downstream processing system, which will use these tracks together with trigger primitives from the calorimeter and muon sub-detectors to perform physics objects reconstruction.

## 2. Track trigger approaches

The three L1 track finding approaches [2] currently pursued in CMS are referred to as Associative Memory (AM), Tracklet, and Time Multiplexed Track Trigger (TMTT). The AM approach uses a combination of Associative Memory ASICs and FPGAs to perform real time pattern recognition, while the other two rely solely on FPGAs. In order to demonstrate that L1 track finding can be achieved and to compare the different approaches being proposed, small-scale hardware demonstration systems are being implemented for each approach. The aim is to understand L1 tracking performance, to optimize system designs, and to complete comparative cost-performance analyses. The following sections present brief overview of each of the three approaches being considered.

### 2.1 Associative Memory

The AM approach [2] works in two stages. At the first stage, pattern recognition is performed by matching formatted stubs with coarse pre-computed patterns stored in the AM chips. The AM offers fast parallel processing for complex combinatorics of track finding, with data from the detector being compared with all patterns stored in the memory almost simultaneously. In the second stage, full resolution position information is retrieved for the stubs passing the AM filtering stage and track fitting is performed in an FPGA.

The detector is divided into 48 trigger towers, and data from all towers is processed in parallel. The high volume of incoming data is time multiplexed using the large inter-board communication bandwidth provided by full-mesh ATCA backplanes. For the demonstration, data coming from a given trigger tower is processed by an ATCA based Pulsar-2b blade [3] developed at Fermilab. The data is formatted and then routed to FMC mezzanine cards equipped with AM chips, which perform the pattern recognition. Linearized track fitting is then performed using a Principal Component Analysis (PCA) algorithm implemented in the mezzanines' FPGA.

### 2.2 Tracklet approach

The tracklet approach [2] uses a road search technique for implementing L1 track finding. The road is seeded by "tracklets", which are pairs of stubs from adjacent layers. The algorithm forms seeds in multiple pairs of layers. The seeds are projected into adjacent layers to add hits consistent with a high $p_T$ track trajectory. The impact parameter in the $r-\phi$ plane is used as a constraint to calculate helix parameters of the trajectory in both the $r-\phi$ and the $r-z$ planes. A linearized $\chi^2$ fit is performed if a tracklet has matches with two or more stubs. As in the other approaches, a given track can be found and fit multiple times, thus a duplicate removal filter operates after the track fitting stage. The approach uses commercially available FPGA technology with $\mu$TCA based CTP7 boards [4] for the demonstration. The detector is divided into 28 sectors in $\phi$, each handled by a single FPGA. The approach is naturally pipelined and has a low time multiplexing factor.

### 2.3 Time Multiplexed Track Trigger

The TMTT approach [2] uses the concept of Hough Transformation [5] (a line detection algorithm) in the $r-\phi$ plane, to coarsely group stubs consistent with a high transverse momentum track into candidates, before a second stage fitting process is applied. A fully time multiplexed design using FPGA based hardware is considered to simplify the system architecture and the implementation of the Hough Transformation based track finding. Segmenting the tracker into independent trigger regions, for example in $\phi$ octants, allows all data from a region to be processed by a single processor board. This avoids replication of data shared among the regional detector boundaries. The TMTT hardware demonstration uses the MP7 $\mu$TCA board [6] for track processing. The detector is divided into 8 octants in $\phi$, with one octant being processed by a track finding processor.

## 3. Summary

Demonstration test benches have been assembled for each of the L1 Tracking Trigger approaches in order to measure the performance (latency, efficiency, purity, resolutions, etc.) using simulated data with HL-LHC occupancy and rate, and to compare different proposed architectures. The final goal is to demonstrate a viable L1 track finding system. Figure 1 shows the demonstrator systems under study for the AM, the tracklet, and the TMTT approaches, set up at facilities at FNAL and CERN. It shows the usage of the current ATCA based Pulsar 2b and $\mu$TCA based CTP7 and MP7 board technologies for the demonstrators. All the three approaches are being optimized to provide full coverage of the tracker detector, with segmentations in pseudo-rapidity and azimuth, and with a minimal fraction of redundancy.

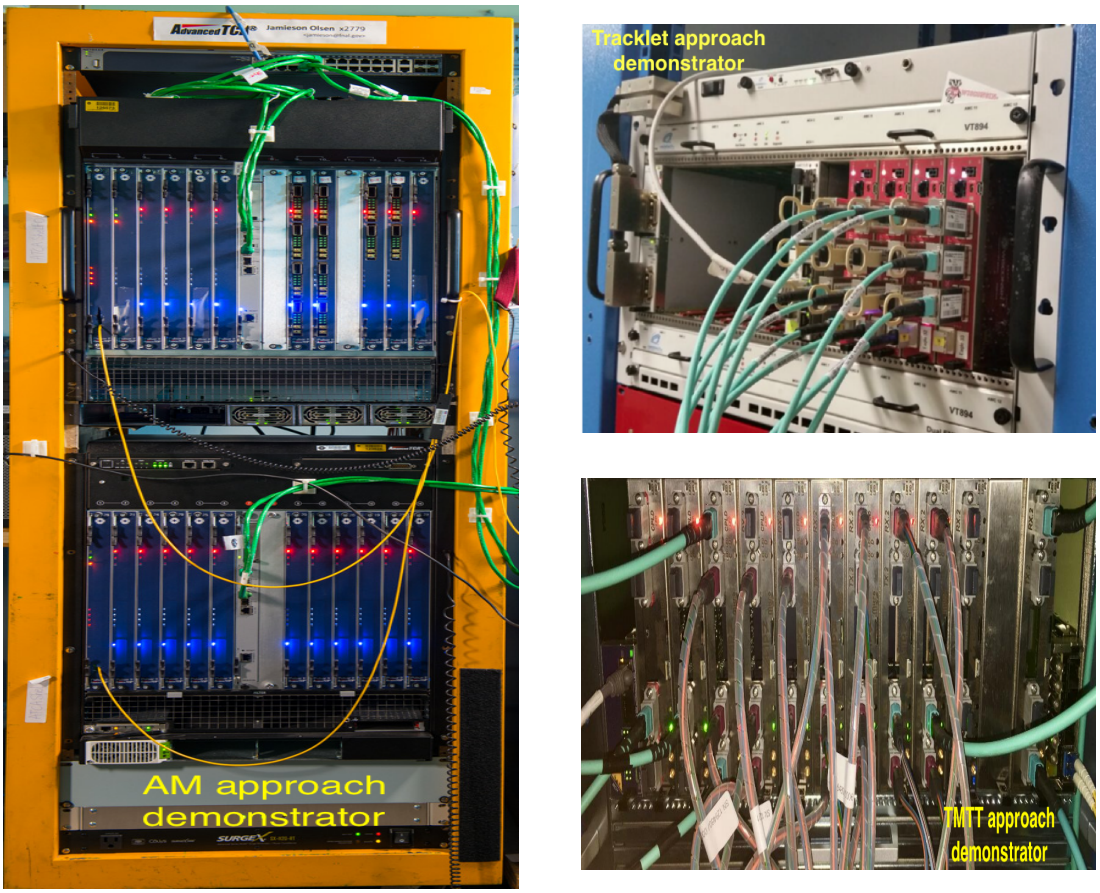


**Figure 1:** The AM, the tracklet and the TMTT demonstration systems.

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