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Radiation hardness of two CMOS prototypes for the ATLAS HL-LHC upgrade project

B.T. Huffman (University of Oxford) *et al*

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B.T. Huffman,[b] **A. Affolder,**[a] **K. Arndt,**[b] **R. Bates,**[c] **M. Benoit,**[l] **F. Di Bello,**[l] **A. Blue,**[c] **D. Bortoletto,**[b] **M. Buckland,**[a,p] **C. Buttar,**[c] **P. Caragiulo,**[d] **D. Das,**[e] **J. Dopke,**[e] **A. Dragone,**[d] **F. Ehrler,**[f] **V. Fadeyev,**[g] **Z. Galloway,**[g] **H. Grabas,**[g] **I.M. Gregor,**[h] **P. Grenier,**[d] **A. Grillo,**[g] **M. Hoeferkamp,**[q] **L.B.A. Hommels,**[i] **J. John,**[b] **K. Kanisauskas,**[b,c] **C. Kenney,**[d] **J. Kramberger,**[j] **Z. Liang,**[g] **I. Mandić,**[j] **D. Maneuski,**[c] **F. Martinez-Mckinney,**[g] **S. McMahon,**[b,e] **L. Meng,**[a,l] **M. Mikuž,**[j,k] **D. Muenstermann,**[r] **R. Nickerson,**[b] **I. Perić,**[f] **P. Phillips,**[b,e] **R. Plackett,**[b] **F. Rubbo,**[d] **J. Segal,**[d] **S. Seidel,**[q] **A. Seiden,**[g] **I. Shipsey,**[b] **W. Song,**[o] **M. Stanitzki,**[h] **D. Su,**[d] **C. Tamma,**[d] **R. Turchetta,**[e] **L. Vigani,**[b] **J. Volk,**[g] **R. Wang,**[m] **M. Warren,**[n] **F. Wilson,**[e] **S. Worm,**[e] **Q. Xiu,**[o] **J. Zhang**[m] **and H. Zhu**[o]

[a] *University of Liverpool, U.K.*
[b] *University of Oxford, Keble Road, Oxford OX1 3RH, U.K.*
[c] *SUPA — School of Physics and Astronomy, University of Glasgow, Glasgow, U.K.*
[d] *SLAC National Accelerator Laboratory, U.S.A.*
[e] *Rutherford Appleton Laboratory, Didcot, U.K.*
[f] *Karlsruhe Institute of Technology, Germany*
[g] *University of California Santa Cruz, Santa Cruz Institute for Particle Physics (SCIPP), Santa Cruz, CA, U.S.A.*
[h] *Deutsches Elektronen-Synchrotron, Hamburg, Germany*
[i] *Cambridge University, U.K.*
[j] *Jožef Stefan Institute, Ljubljana, Slovenia*
[k] *University of Ljubljana, Slovenia*
[l] *Universite de Geneve, Switzerland*
[m] *Argonne National Laboratory, U.S.A.*
[n] *University College, London U.K.*
[o] *Institute of High Energy Physics, Beijing*
[p] *CERN, European Center for Nuclear Research, Switzerland*
[q] *University of New Mexico, U.S.A.*
[r] *Lancaster University, U.K.*

E-mail: todd.huffman@physics.ox.ac.uk

[1]Corresponding author.

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Abstract: The LHC luminosity upgrade, known as the High Luminosity LHC (HL-LHC), will require the replacement of the existing silicon strip tracker and the transistion radiation tracker. Although a baseline design for this tracker exists the ATLAS collaboration and other non-ATLAS groups are exploring the feasibility of using CMOS Monolithic Active Pixel Sensors (MAPS) which would be arranged in a strip-like fashion and would take advantage of the service and support structure already being developed for the upgrade. Two test devices made with the AMS H35 process (a High voltage or HV CMOS process) have been subjected to various radiation environments and have performed well. The results of these tests are presented in this paper.

Keywords: Radiation damage to electronic components; Solid state detectors; Radiation-hard detectors; Particle tracking detectors (Solid-state detectors)

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Contents

1 Introduction — ATLAS Strip Tracker and CMOS Sensors

Motivation for HV and HR CMOS in ATLAS Ever since silicon detectors started to appear in high energy particle physics detectors in the early '90s there has been a desire to incorporate the amplification and data processing functions on the silicon sensor itself. MAPS (Monolithic Active Pixel Sensors) is the term used to refer to such devices. The desire for a fully integrated MAPS device was previously thwarted for a number of reasons, but one of those reasons was the simple fact that standard CMOS circuits use relatively highly doped substrates while silicon strip and pixel sensors need large depletion depths in order to obtain the sufficient signal and fast charge collection time and so require lower dopant levels.

This all started to change over approximately the last decade with the development of commercial processes within CMOS that were designed for high voltage (HV CMOS) and other commercial processes which used high resistivity substrates (HR CMOS). The group was formed in September 2014. As a result, the authors have been looking at the properties of test devices produced using either HV or HR CMOS [1, 3] (see also footnote 2.). Many different devices have been tested and the results regarding radiation tolerance and signal-to-noise look promising.

MAPS in ATLAS R&D The High Luminosity LHC (HL-LHC) is the next series of proposed upgrades to the CERN accelerator designed to deliver hundreds of fb^{-1} of data to the experiments starting in 2026 [4]. The ATLAS collaboration is preparing a baseline design for the HL-LHC that will use an all-silicon inner tracker starting with pixel detectors on the inner-most layers and then moving to silicon strip detectors for outer layers and end-cap disks at higher radii from the beam

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pipe. The baseline silicon strip tracker (SCT) would have over 200 m^2 of silicon strips and would take over 100 million wire bonds to connect the pre-amplifer/signal processing chips to the silicon sensors. Approximately 3 years have been scheduled in this project for wire-bonding.[1]

The ATLAS upgrade group along with members of other groups and IC designers have formed a collaboration to explore the possibility of using CMOS technologies in the ATLAS strip tracker instead of traditional silicon strips attached to separate amplifier IC's. This report outlines some of the results obtained on a pair of CMOS sensors. Future plans and conclusions from our tests are also included.

2 The Devices

Sensors and electronics in the volume of the inner tracker during HL-LHC running must be radiation hard. This requires extensive testing with a range of radiation sources to ensure that they will be radiation hard enough to operate with sufficient signal above the noise floor to maintain a high tracking efficiency. For the outer tracker we are required to maintain a high signal to noise ratio after 1.0×10^{15} neq/cm^2 fluence and 600 kGy of total ionizing dose.

For these studies we have two different silicon sensor chip designs which were implemented within the AMS H35 350 nm CMOS process. We have called them "HVStrip1" and "CHESS1" (or sometimes "AMS CHESS1"). The substrate resistivity of this process is nominally 20 Ω·cm. These test chips have several different types of active and passive elements. The salient details of the devices we use on these test chips are explained below.

2.1 HVStrip1

The HVStrip1 chip has several different test structures which allow characterization of a variety of active and passive devices.[2] The chip contains NMOS and PMOS transistors, a passive diode, and a 22×2 array of diode pixel sensors with active components implemented on the sensors. The active components include a pre-amplifier and a comparator that can be configured to adjust for time-walk effects from varying signal sizes. The chip has one analog output pad which can be connected to the output of the charge sensitive amplifier on any one of the forty-four 40×400 μm active channels. A nominal 0.5 fF capacitor is connected to the input of each active pixel for charge injection studies. X-ray calibration signals indicate the true value of this capacitor is 0.6 fF. The analogue output is used to test the performance of this device.

We refer to the active channels in the pixel array by their (column,row) designation. The front-end amplifiers in the array from columns 0 through 7 have a standard layout transistor in the feedback loop of the circuit. Those from columns 8 through 21 contain a circular transistor in that location. Figure 1 shows an example of each of these types of layouts [2]. This results in a gain profile that changes depending on the physical location of the channel. The circular transistors cause those channels to have significantly less gain: $\simeq$ 170 mV/fC compared to $\simeq$ 220 mV/fC. No trimming has been done partly in order to observe the effects of radiation on the different structures.

[1] "Wire bonding" in this case is a specialist task with bespoke equipment. Bonding is from non-standard detector-grade silicon on to non-rigid flex circuits. Some structures are 1.4 m long. Further, direct experience with the current ATLAS inner strip tracker with its 6 million wire bonds informs the estimated schedule.

[2] HVStrip1 was designed and submitted late in 2014 by I. Perić with a short turn-around..

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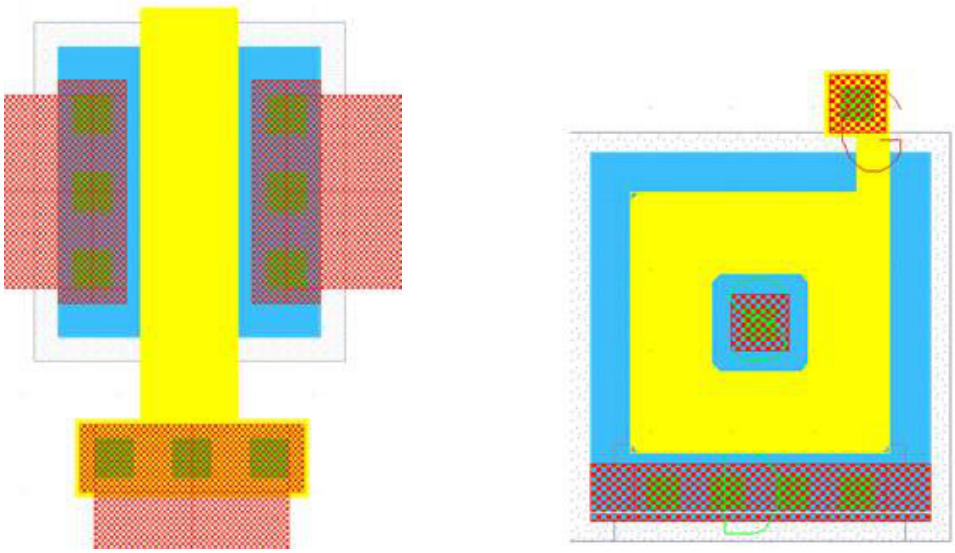

Figure 1. Shown on the left is the layout of a standard CMOS transistor while on the right is the layout of an enclosed (or circular) transistor.

2.2 CHESS1

The CHESS1 test detector was implemented in the AMS H35 process.[3] This chip has a large number of different structures including ≃ 80 amplified diode pixels, standalone amplifiers, and an array of more than 300 passive pixel elements of various sensitive areas. But we summarize here the structures that are used in tests.

Apart from the large passive pixel array mentioned above, the chip also has standalone amplifiers with inputs and outputs available as pads. The amplified pixels come in blocks of 9 pixels and the pixel blocks have different sized pixels ranging from $45 \times 100\,\mu$m to $45 \times 800\,\mu$m with the lengths increasing by factors of two. All active pixels have the same type of amplifier attached to the sensors. The amplifier was designed to be fast so drift would be the primary source of charge collection and so the noise and signal performance would be more akin to what is needed for a tracking detector with beam crossings every 25 ns. All these active sensors, and one additional block of 9 pixels without an amplifer, are located around the edge of the chip to accommodate laser charge injection at different depths within the chip. Many of the results presented here use this passive array.

3 Test results of discrete and passive components

The group has performed tests on a number of the discrete ccomponents on both the HVStrip1 and CHESS1 chips.

[3]The UCSC design was influenced by a similar device [5].

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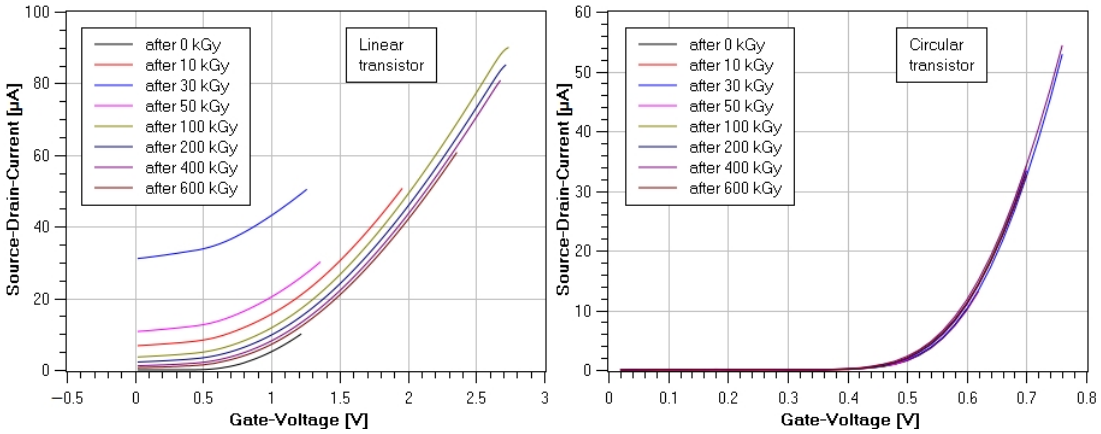

Figure 2. Shown is the performance of the two types of NMOS transistor on the HVStrip1 chip as the device is exposed to gamma rays. The left-hand plot shows the Source-Drain current as a function of gate voltage for a standard, linear layout transistor. The right-hand plot show the same quantities but the layout of this transistor is circular.

3.1 Transistor devices

On HVStrip1 the NMOS transistor elements are of two types, one is a standard layout transistor while the other is designed in a circular (or enclosed) configuration which is expected to maintain its performance when exposed to radiation. That this is indeed true is shown in figure 2. Both standard and circular devices were exposed to X-rays with a most probable energy of 35 keV (see [6] for details on the facility used).

We can see that the device featured in the left-hand plot in figure 2 has a much wider variation in operation as the device is exposed than its circularly laid out counterpart in the right-hand plot. Another interesting feature of the left-hand plot is that performance of the transistor first changes dramatically with the initial radiation exposure, but then returns to a state that is closer in operation to a pristine device as the exposure increases above 100 kGy. This behavior is consistent with competing effects of oxid charge generation and the activation of interface traps [7].

At the HL-LHC the inner layers of the ATLAS outer tracker are expected to receive no more than 600 kGy of ionizing radiation [4]. Since the transistors in figure 2 were exposed to these levels, one message from this result is that ionizing radiation in excess of that expected by the inner layer can be tolerated by the transistor elements if radiation hard design practices are employed. Other devices on the HVStrip1 chip and also radiation measurements on other devices have been reported in [8, 9].

3.2 Passive diodes

The CHESS1 chip has an array of passive diodes near its edge. This allows the injection of charges into the diodes from the side using a laser, the method is known as edge-TCT [10]. The laser has a wavelength of 1064 nm and can be focused to a spot size of $\simeq 5\,\mu$m in diameter. The chip is mounted on a motion stage so that, when side illuminated, the laser spot can be scanned down the depth of the silicon in the chip. Electron-hole pairs produced in the depletion region of the element will quickly (within ns) drift to the electrodes while inducing current on an electrode, while charge carriers that diffuse through the medium will take several hundreds of times longer. The laser spot

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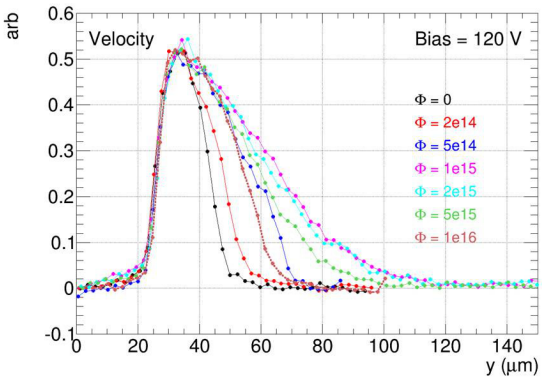

Figure 3. Shown above is the velocity profile when a laser is used to excite carriers at differing depths in the silicon detector. The horizontal axis is the depth in the silicon. The vertical axis is in units proportional to the charged carrier velocity. The region of high velocity charge maps out the drift region of the device. The different color curves show the effect of an increasing dose of reactor neutrons. The top surface of the chip is at $y \simeq 20\ \mu$m.

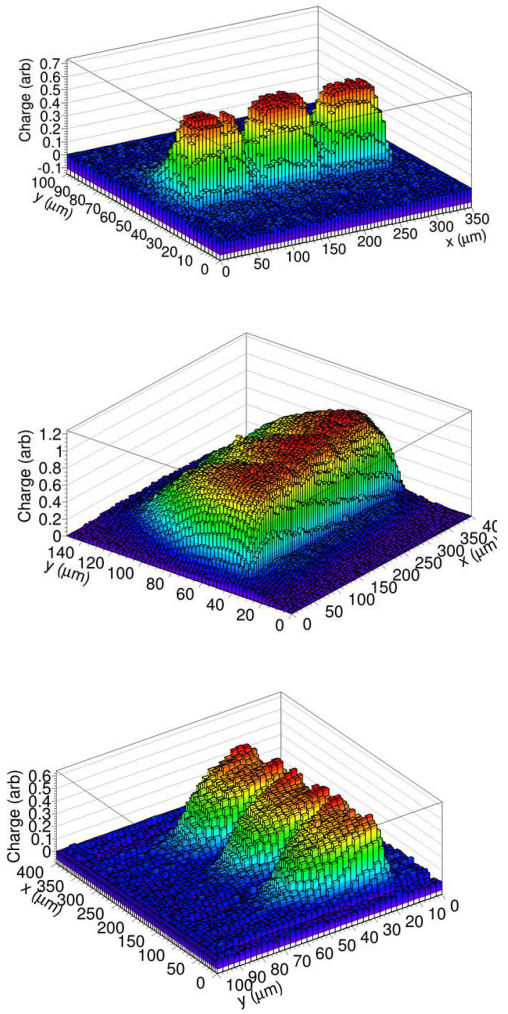

Figure 4. We can see the effect of increasing depletion volume in this triplet of plots showing a scan of three passive diodes using the eTCT system. Initially, the depletion region is small and one can clearly see the gaps due to guard ring structures between the three diode channels. The other two plots show the effects of increasing dose.

is scanned down the side of the chip from the top surface along its edge toward the chip's back face. Consequently, the charge injected will appear in the depletion region or in the bulk region depending upon the scan position. By recording the induced current a fixed, short time after the laser was triggered, a signal height as a function of depth is obtained that acts as a proxy for drift velocity. Laser spot depths showing high levels of signal are thus dominated by fast drift and are within the depletion region while diffusion carriers generate little or no signal with this method [10].

Extensive tests have been done on several CHESS1 passive diodes that have been exposed to fast neutrons in the Ljublijana research reactor using the eTCT laser system [11]. Neutron fluences

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up to 1.0×10^{16} neq/cm^2 have been studied on a couple of CHESS1 devices. The results obtained are consistent with the depletion region **increasing** as the device is exposed to more neutrons. Figures 3 and 4 show this. The fast-signal region (associated with a drift signal) attains its maximum extent between exposures of 1.0 and 2.0×10^{15} neq/cm^2 before decreasing again at 1.0×10^{16} neq/cm^2.

Figure 4 shows the effect particularly well. This is an eTCT scan with a laser source. The top image is a plot where the y axis is the depth down the edge of the silicon chip while the x axis has the laser spot scanning along the chip parallel to its row of pads. The third axis is the signal size detected on the diode from a fast signal defined as the integrated current pulse over 25 ns, and mainly contains drift carriers.

The top plot shows the CHESS device prior to any radiation where we see three passive diodes together and their depletion regions well-separated due to the presence of guard rings. The middle plot is the same device after exposure to fast neutrons from a reactor up to 2.0×10^{15} n/cm^2 and 1.0×10^{16} n/cm^2 for the bottom plot. Here the depletion regions of the three sensors have increased to the point where they have merged into one large sensitive region. The last picture shows that further increases in radiation so damage the silicon that the depletion volume falls once again, recovering the structure observed in the top picture. These results are understood as acceptor removal, which increases depletion depth and would increase the charge collected. However, as irradiation damage increases further, the higher density of trap sites eventually reduces the collected charge even though the depletion depth remains large.

3.2.1 Response to ^{90}Sr electrons

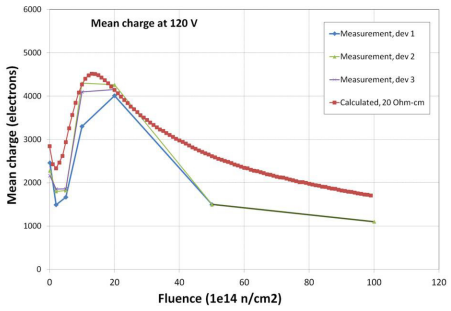

Figure 5. The measured signal size of three CHESS chips subjected to neutron radiation as a function of fluence. The red curve is a simulation of the signal size. ^{90}Sr electrons provided the signal.

If the depletion region truly is increasing as the laser measurements above imply then when a charged particle, such as an electron, passes completely through the silicon we ought to see an increased signal as the fluence increases. The maximum collected charge would be near the radiation exposure shown in the middle plot of figure 4. This prediction is borne out by a test where the diodes in the large passive array are exposed to beta radiation from ^{90}Sr. In this case, for three different devices shown in figure 5 we see that the amount of charge collected does indeed increase for fluences up to 2.0×10^{15} neq/cm^2 and then decreases afterward. The red curve in the figure is a simulation of the expected signal taking these effects into account. It models the increase in the depletion depth with radiation, and it also accounts for trapping losses which increase as the device is damaged [12, details of the simulation], [13].

4 Test results of Active channels

We have seen the interesting result that the signal size increases with sufficient exposure to radiation by looking at the passive elements. Although these devices can be laid out using radiation hard

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Table 1. Using charge injection on the HVStrip1 chip, the amplifiers' gains have been measured with standard (channel (5,0)) and enclosed (channel (12,0)) transistors. Shown are changes typical of what has been seen. The device was exposed to 27 MeV protons to 1.0×10^{15} neq/cm^2. The amplifier with enclosed transistors suffers the greatest loss of gain of 25.6%.

Pixel (c,r)	Before (mV/fC)	After (mV/fC)	Change (%)
(5,0)	147.4	132.7	-10.0
(12,0)	150.6	112.1	-25.6

design techniques, it is still necessary to understand the performance of the active cells given that radiation will damage the amplification transistors along with the sensor elements. Consequently, the HVStrip1 chip was also exposed to protons which have the property of simultaneously generating ionizing and bulk damage effects and their active channels observed.

All of the test results from active sensors presented in this section come from the HVStrip1 chip. They were exposed to 27 MeV protons from the Birmingham Cyclotron. The chips were exposed to approximately 1.0×10^{15} neq/cm^2. A combination of charge injection through the on-chip capacitor (~ 0.65 fF), ^{90}Sr electrons from beta decay, and X-rays from the decay of ^{55}Fe were used as signal sources to test performance after the irradiation. In some cases after radiation, secondary X-rays from K-shell electrons in Ag or Mo were used to create a larger signal from x-rays of a known energy within the irradiated sensors.

The first result is shown in table 1 and the results of this table come entirely from X-ray charge injection. As mentioned previously the HVStrip1 device has two different types of transistors in the layout of its pre-amp, and table 1 shows the results of the changes in gain these amplifiers exhibit before and after exposure to the proton beam. Channel (5,0) has the standard layout while channel (12,0) uses enclosed transistors. The decrease in performance marginally favors the pre-amp made with standard transistor techniques (5,0). The results presented in table 1 use signals deposited in the active pixels by X-rays and these do not deposit charge in the same manner as minimum ionizing particles, so further tests in this area are needed.

The decreases in gain experienced by the active amplifiers should be smaller than the increases in signal from minimum ionizing particles one would expect based on the results obtained with the passive elements. The evidence we have collected thus far supports this. Our group have confirmed, using ^{90}Sr electrons, that the active pixels in HVStrip1 are measuring higher levels of charge collection after irradiation. This is shown for centrally located channels in figure 6 comparing the amplifier+diode response to minimum ionizing electrons both before and after irradiation. In figure 6 the two plots only differ by channel number. The left plot shows a central channel with a standard layout while the right plot shows a central channel with an enclosed transistor layout. Electrons from the beta decay of ^{90}Sr have a spectrum and most of the electrons emitted are of very low energy. To screen out these low energy decays and keep only the minimum ionizing electrons, a scintillator was placed below the chip and its PCB carrier board. The chip+PCB act as an absorber making it unlikely that non-minimum ionizing electrons would be able to strike the scintillator and supply a trigger.

The signal from minimum ionizing electrons can be seen in both plots and the level of charge deposited increases. These were devices exposed to 27 MeV protons as described previously

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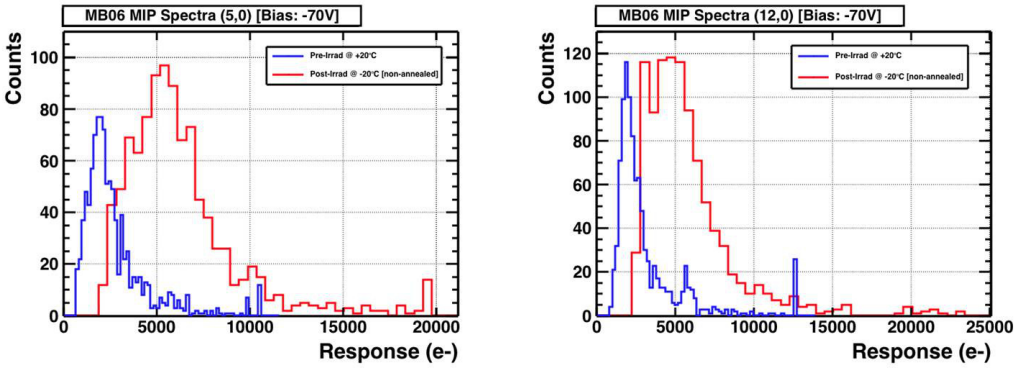

Figure 6. Shown are histograms of the peak signal obtained from the beta spectrum of ^{90}Sr filtered such that the signal (red) is from minimum ionizing eletrons. Channel (5,0), the left-hand plot, had active amplifiers with linear transistors while channel (12,0) (right-hand plot) used enclosed transistors. In both cases the blue curve is the peak signal histogram prior to irradiation while the red curve is after irradiation.

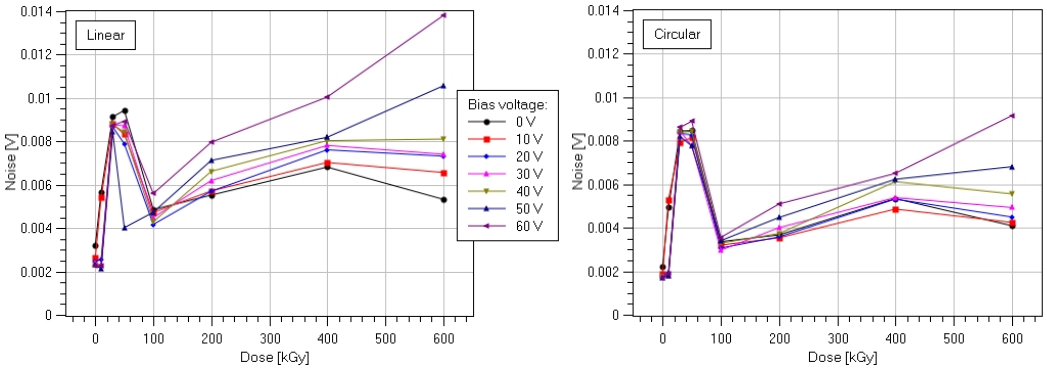

Figure 7. The noise performance of active pixels with linear and enclosed transistors as they are exposed to X-rays. The different colors show different pixel bias voltages.

1.0×10^{15} neq/cm^2. Because of the low energy protons used, which lose nearly all their energy within the chip, ionizing effects may dominate over bulk damage.

How the noise increases with high doses of ionizing radiation is shown in figure 7. Again we see some of the curious features of these devices where they seem to perform best with no radiation, pass through a period where their performance degrades, and then show improvements with greater doses. However, noise performance never improves to pre-irradiation levels and does tend to get worse as dose increases above 100 kGy [14]. Although the signal increases, since the noise of the system also increases requiring a higher trigger threshold in figure 6. On the basis of our observations of minimum ionizing particles the noise appears to increase approximately in step with increased leakage current.

5 Future Plans

The formal ATLAS CMOS strips project has two more years to run. As of the time of this writing AMS H35 CHESS1 devices will be exposed in the CERN Proton Source to $\approx$ 23 GeV protons to

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two levels: 1.0×10^{15} neq/cm^2 and half this value. In addition similar CHESS1 devices from the Tower Jazz foundry will be expected to arrive early in 2016. These CHESS1 chips will have a variety of substrate resistances up to 600 Ω·cm. This will give the project an opportunity to test whether larger depletion zones return the expected benefits in SNR.

In the final design stages are two prototype strip sensors which will act as our first test strip detectors that are fully architecturally functional. They will have 128 channels that include discriminators and z-encoding along the strips. They will incorporate a fully digital readout of channel numbers. The two sensors will be submitted to the AMS H35 process and the Tower Jazz 180 nm process and manufactured with a range of substrate resistances. Finished devices are expected in the early summer of 2016.

6 Conclusions

The ATLAS collaboration, along with other partners, formed a working sub-group last year that has successfully tested two MAPS devices in HV CMOS (HVStrip1 and CHESS1) using the AMS H35 process. The two devices have been subjected to ionizing, minimum ionizing (X-rays, gamma rays, and protons), and bulk damage radiation (protons and neutrons). In all cases the devices continued to perform after doses of 600 kGy and in excess of 1.0×10^{15} neq/cm^2 (and with neutrons alone up to 1.0×10^{16} neq/cm^2).

One interesting effect is that the depletion region for a given bias voltage begins to grow increasing the available signal. However, the noise also increases with radiation damage. The additional damage these devices suffer at moderate doses is a concern, as most of the sensor area will be at the higher radii where the radiation levels will not be as high as the maximum dose. The HVStrip1 device indicates that the signal-to-noise ratio after the expected HL-LHC maximum dose will be 13:1 with this process. Tests of chips with high resistivity substrates where it may be possible to increase the depletion depth are an obvious next step.

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