AGH University of Science and Technology

SALT – a Dedicated Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment

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on behalf of the LHCb UT collaboration

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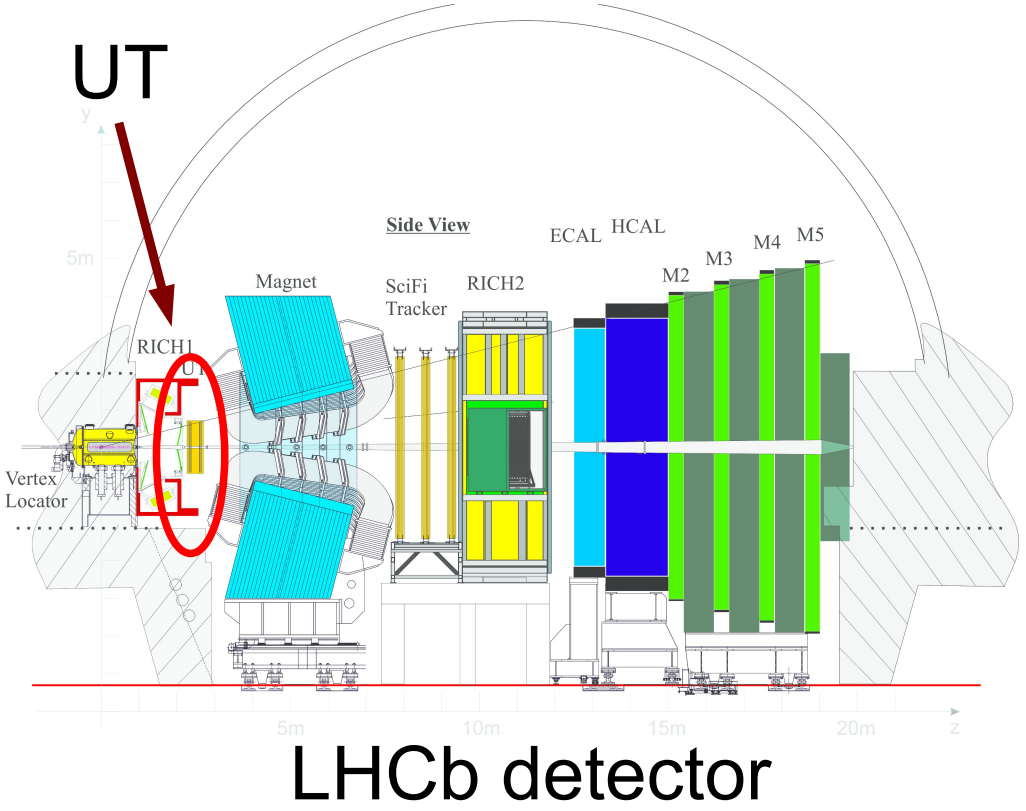
Outline

- Introduction
- SALT design
- Tests results of SALT prototypes

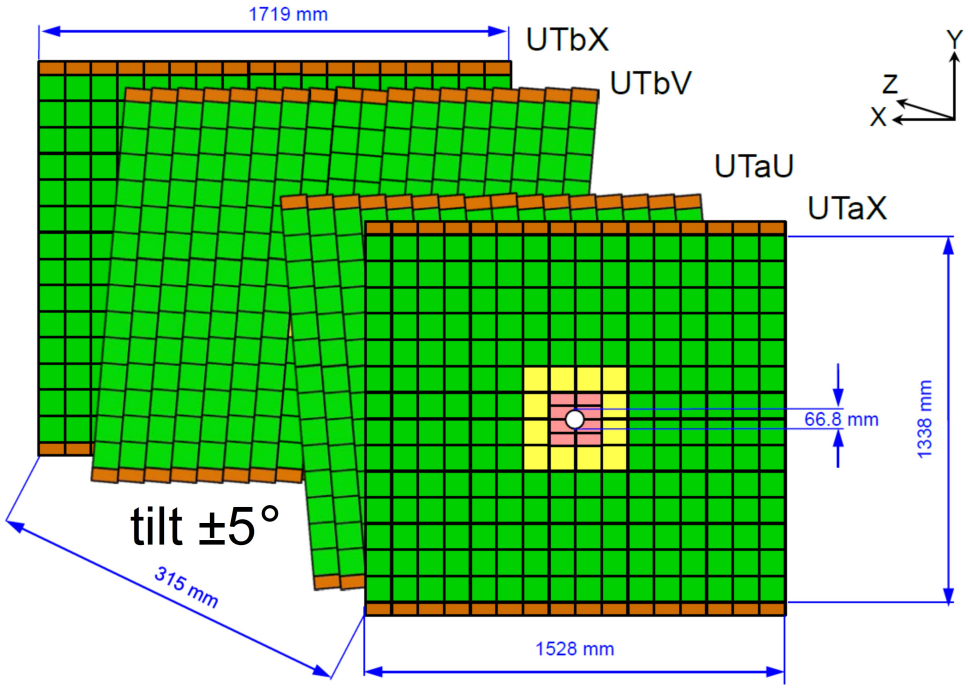
Introduction
Upgrade of LHCb Inner Tracker at LHC

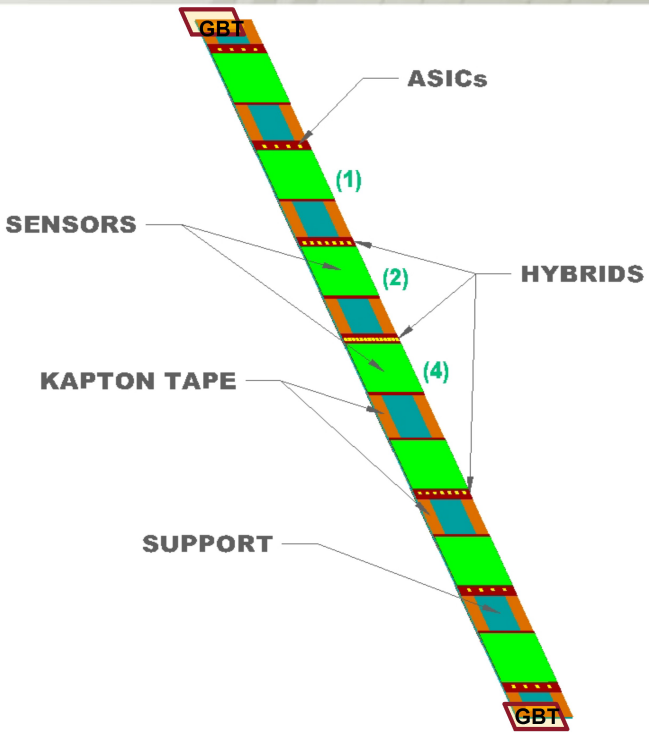
- Upstream Tracker (UT) replaces the Tracker Turicensis (TT)
- 500 000 silicon strip detector channels
- Readout frequency increases to 40 MHz – *currently Level-0 trigger is limited to 1MHz*
- New readout electronics is needed!



LHCb detector

Introduction
Readout of UT silicon strip detectors





- 4 sensor types
  - p^+-in-n, 10 cm length
  - n^+-in-p, 10/5 cm length
- ~1000 hybrids with 4 or 8 ASICs

- ~4000 128-channel readout ASICs – SALT
- Data rate depends on position – different number of active e-links in SALT

Introduction
SALT specification

- CMOS 130 nm technology
- 128 channels, Front-end & ADC in each channel
- Sensor: capacitance 5–20 pF, AC coupled
- Both input signal polarities (p^+-in-n and n^+-in-p)
- Input charge ~30 ke–
- Noise: ENC ~1000 e– @10 pF + 50 e–/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after T_{peak}+25 ns
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit/polarity), 40 MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization & Data transmission: 320 Mbps e-links to GBTx, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~30 MRad

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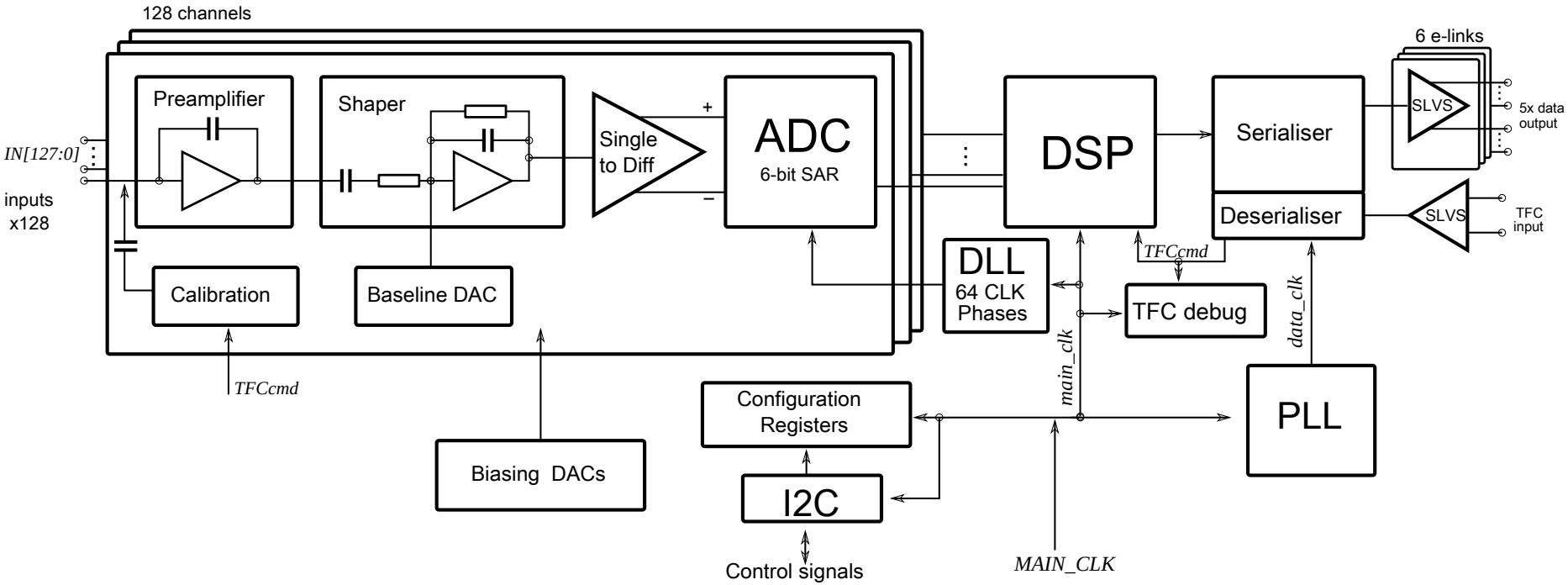
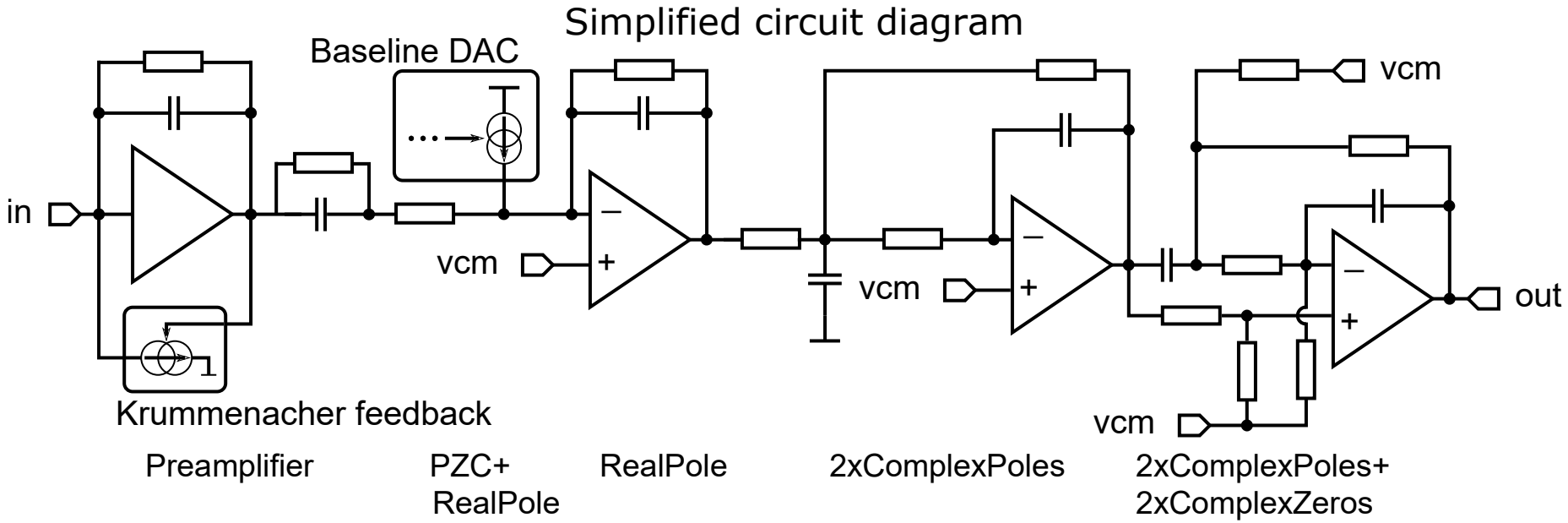
- **SALT design**
- Tests results of SALT prototypes

SALT design Architecture



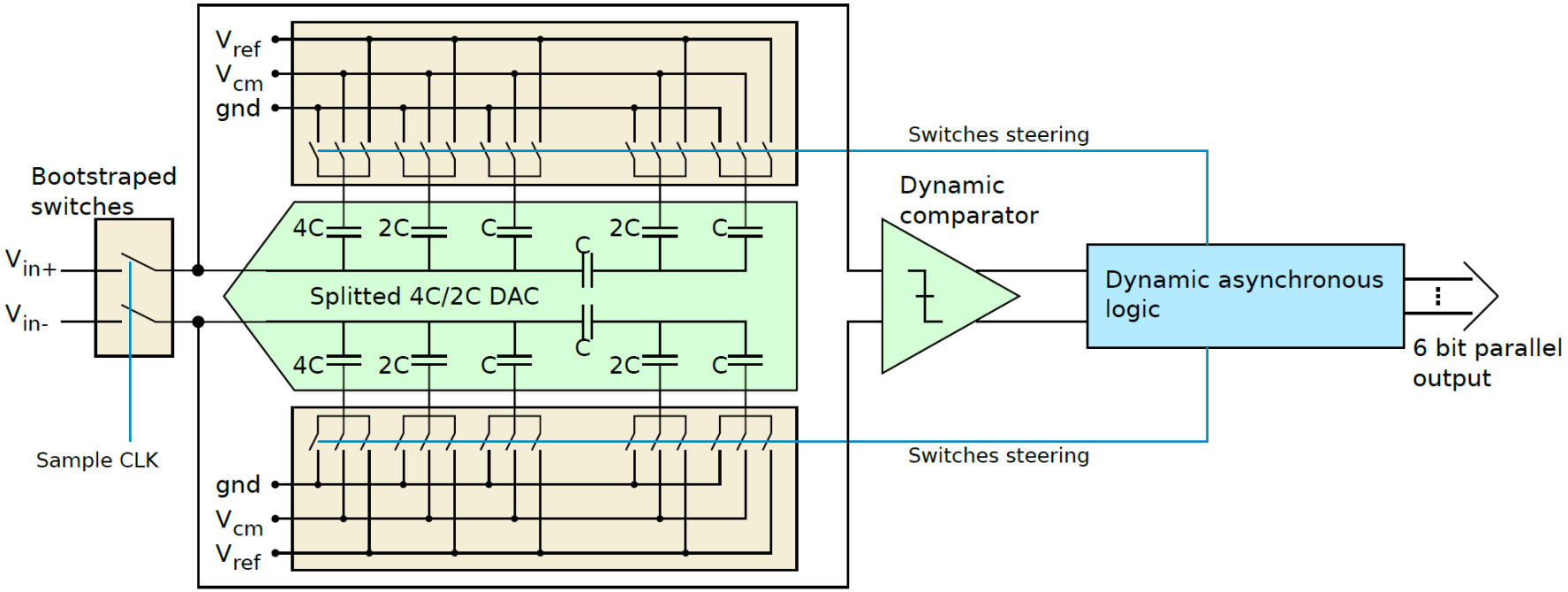
- Front-end & ADC in each channel
- Advanced Digital Signal Processing (DSP)
- many other features/blocks: PLL, DLL, TFC, I2C, SLVS I/O, ...

SALT design
Preamplifier and Shaper



- Charge sensitive amplifier (Krummenacher for DC output)
- 3-stage shaper (complex poles and zeros) gives the requested pulse with short tail
- Common mode (vcm) is kept at half power supply to work with both pulse polarities
- Power consumption: ~1.2 mW

SALT design
6-bit ADC

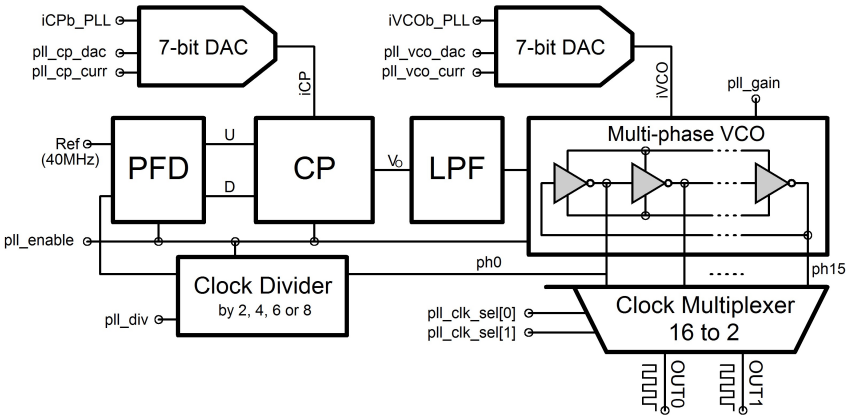


Main features:

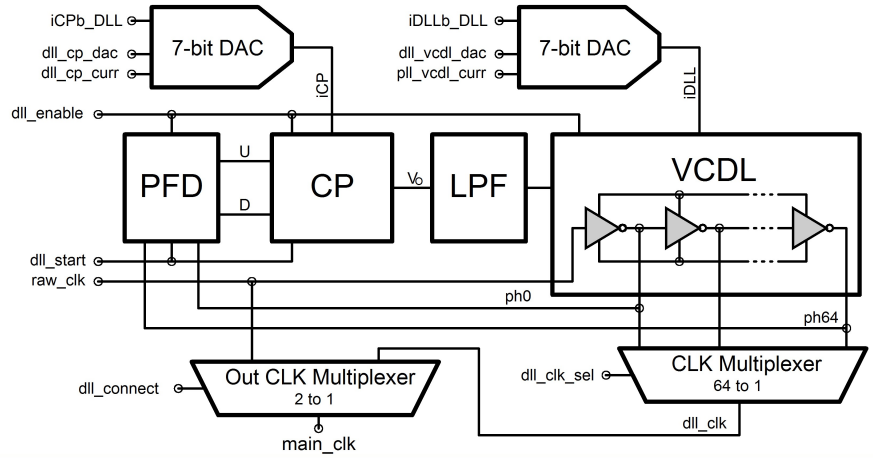
- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Merge Capacitor Switching (MCS)
- Capacitive DAC with 3b/2b split
- Dynamic comparator
- Dynamic asynchronous logic
- Bootstrapped input switches
- Power consumption ~350 uW

SALT design
PLL, DLL

PLL



DLL



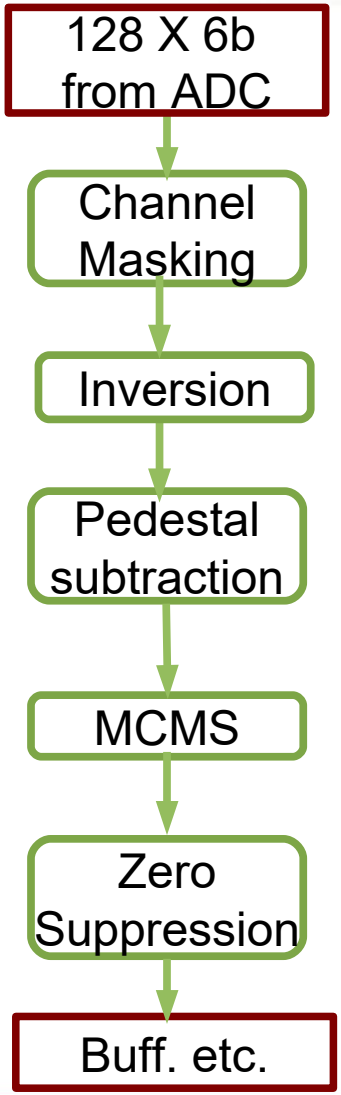
PLL features:

- High frequency (160 MHz) clock for serializer
- Input frequency 40 MHz
- Power consumption ~0.5 mW @ 160 MHz
- Multiplexing – 2 output phases selected from 16 uniform phases (DDR deserialization)

DLL features:

- ADC sampling phase setting
- Input frequency 40 MHz
- Power consumption ~0.7 mW
- Multiplexing – 1 output phase selected from 64 uniform phases

SALT design
DSP operations

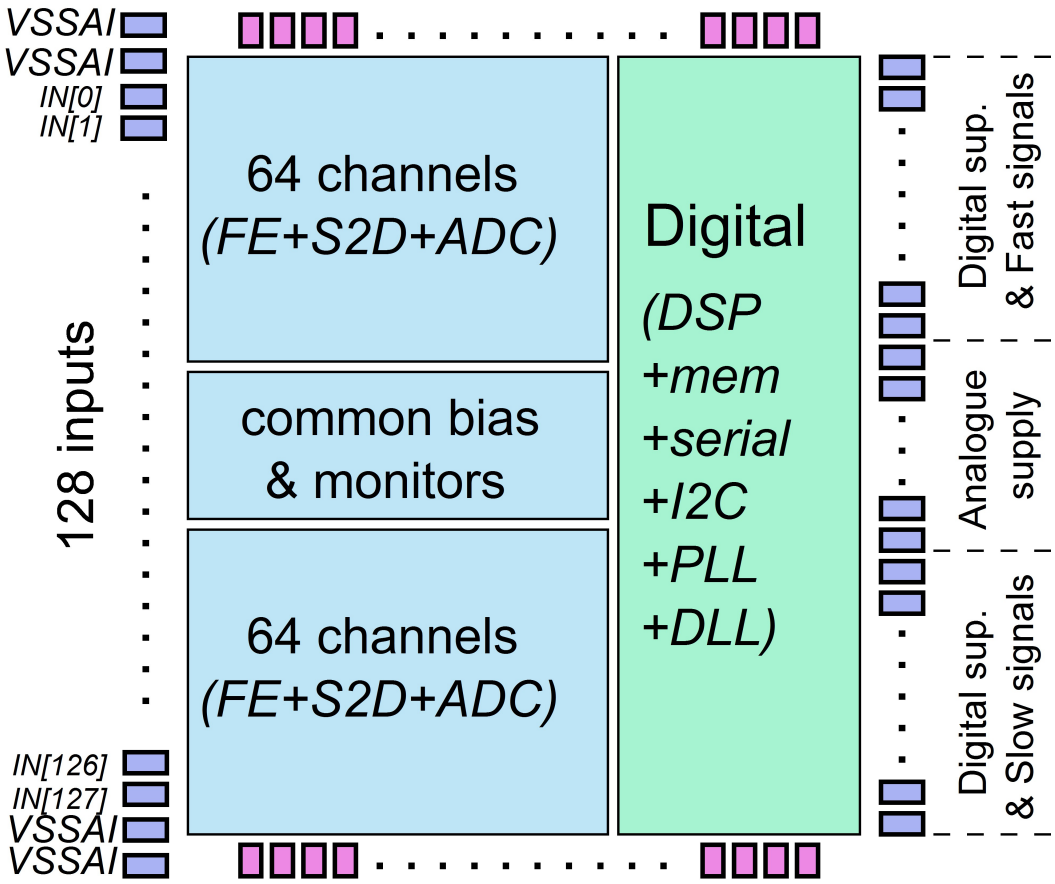


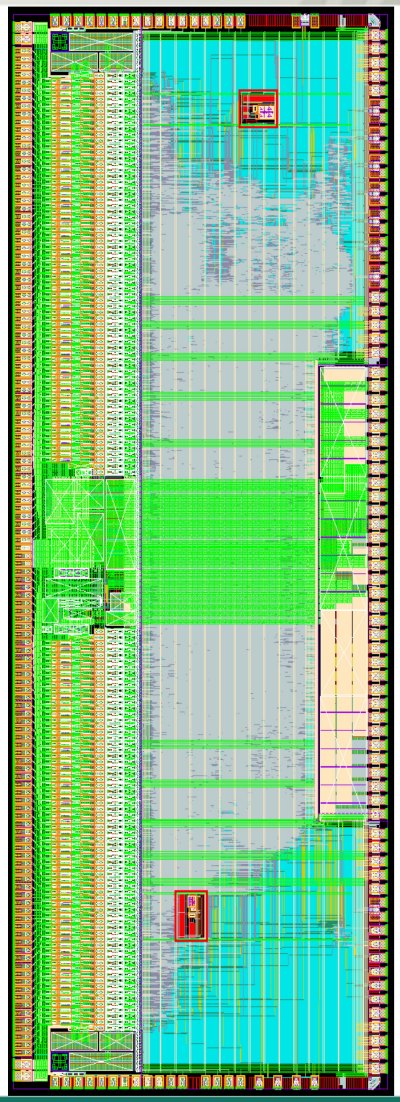
- ADC output is synchronized via async FIFO
- Input data: 6 bits (5 bits plus sign)
- Noisy or dead channels can be masked
- All channel values can be inverted (1 config bit)
- Pedestal subtraction – subtraction in each channel with different value
- MCMS – Mean Common Mode Subtraction
- ZS – Zero suppression

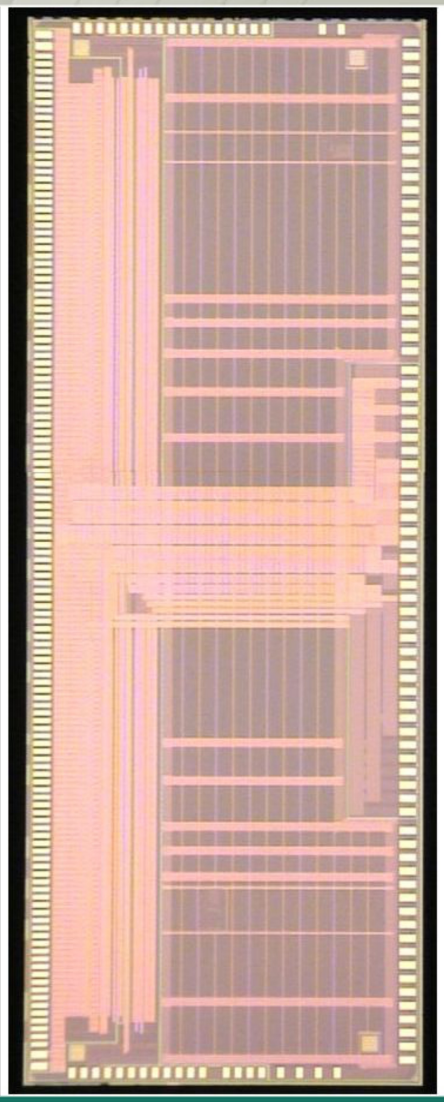
SALT design
Floorplan and layout

4095um x 10900um

Top & bottom pads only for wafer screening







Left & right pads bonded to the hybrid.

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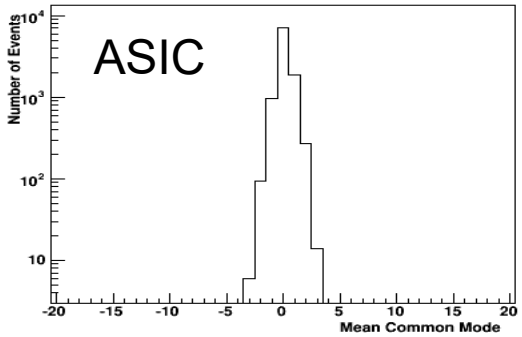
- Introduction
- SALT design
- **Tests results of SALT prototypes**

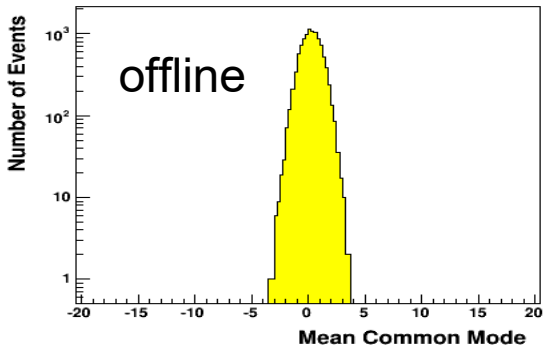
Tests of SALT prototypes
Key functional blocks

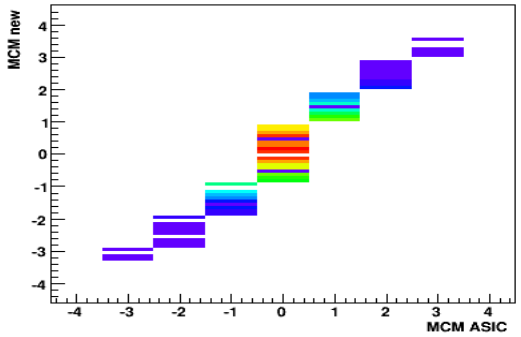
- Operation of all key blocks (Front-end, ADC, PLL, DLL, Bandgap) was positively verified
- SALT8 version 1 was functional, whole readout chain was tested, some issues in analogue and digital parts were found and corrected in SALT8 version 2
- SALT8 version 2 – almost all requested functions implemented, functional tests finished
- SALT (SALT128) – delivered, partially tested

Tests of SALT prototypes
SALT8 MCM

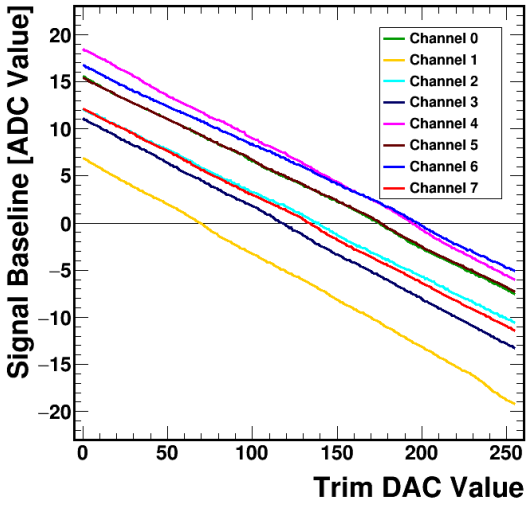
- Mean common mode (MCM) is an average over channels without signal.
- NZS event packet includes MCM & the number of channels used in the calculation.
- SALT8 was configured specially to achieve large MCM range for test purpose.
- MCM from offline calculation are consistent with SALT8 calculation.

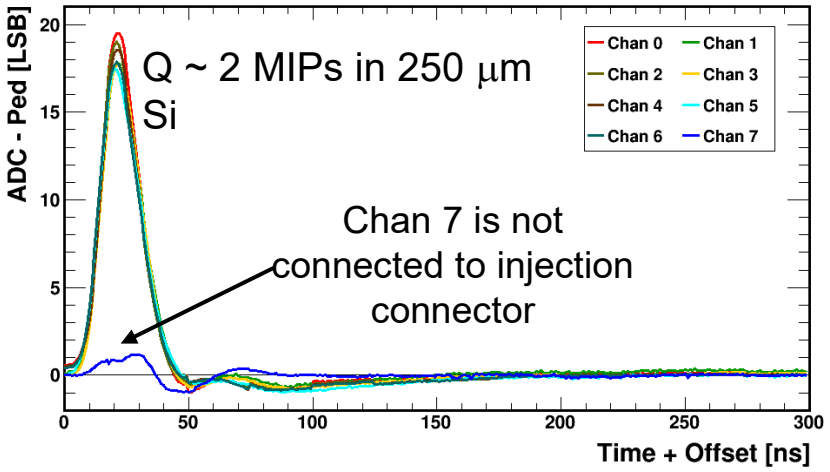






Tests of SALT prototypes
SALT8 trim DACs and test pulse

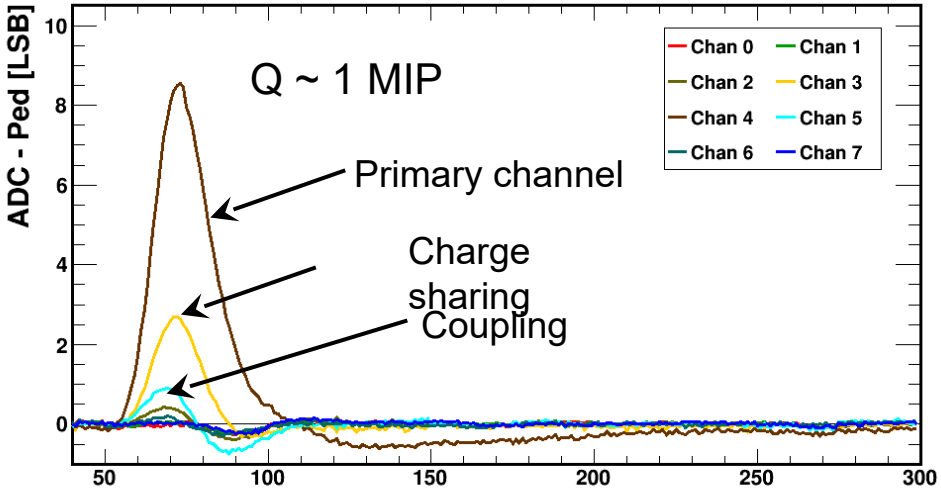


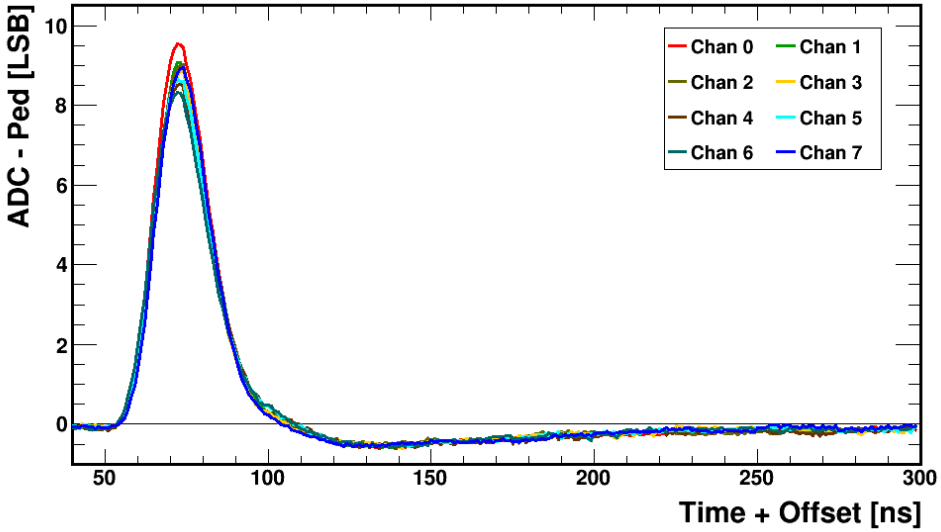


- The fact that we see the expected signals at the SALT8 output, when applying input signal, means that the whole multi-channel (8) chain (front-end, single-to-differential, ADC, digital processing) works well

- Front-end pulse can't be observed directly
  - collecting NZS data packets
  - each point is an average from several hundred measurements
  - delay controlled via SALT8 configuration

Tests of SALT prototypes
Pulse shape using laser source





- Laser beam of ~7 ns width.
- The laser beam is centred on strip connected to channel 4, ~20 um from the border between strips.
- For long strips crosstalk is around 5% as in specs.

- In each of 8 runs, laser beam is centered on the strips one by one.
- Collection of pulse shapes from all channels that are hit by laser beam in each run.

Summary

The development of the SALT ASIC for the LHCb Upstream Tracker is almost finished.

- Two 8-channel SALT prototypes, with nearly complete functionality, were fabricated and tested
- The 128-channel prototype was submitted in June:
  - chips were delivered at the end of August
  - the first test results are promising...
- Radiation tests for 8-channel prototypes have been done, for 128-channel prototype coming soon ...

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Thank You