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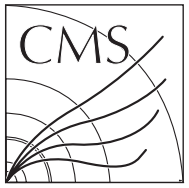

The Compact Muon Solenoid Experiment

Conference Report

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First Implementation of a Two-Stage DC-DC Conversion Powering Scheme for the CMS Phase-2 Outer Tracker

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Abstract

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First Implementation of a Two-Stage DC-DC Conversion Powering Scheme for the CMS Phase-2 Outer Tracker

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Abstract: The 2S silicon strip modules for the CMS Phase-2 tracker upgrade will require two operating voltages. These will be provided via a two-step DC-DC conversion powering scheme, in which one DC-DC converter delivers 2.5 V while the second DC-DC converter receives 2.5 V at its input and converts it to 1.2 V. The DC-DC converters will be mounted on a flex PCB, the service hybrid, together with an opto-electrical converter module (VTRx+) and a serializer (LP-GBT). The service hybrid will be mounted directly on the 2S module. A prototype service hybrid has been developed and its performance has been evaluated, including radiative and conductive noise emissions, and efficiency. In addition system tests with a prototype module have been performed. In this report the service hybrid will be described and the test results will be summarized.

Keywords: Si microstrip and pad detectors; Particle tracking detectors (Solid-state detectors); Voltage distributions

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Contents

1 The CMS Phase-2 Tracker Upgrade

The CMS experiment is one of the six experiments installed at the Large Hadron Collider (LHC), CERN. As of 2016, about 75 fb^{-1} of data at various center-of-mass energies have been collected with the CMS detector [1]. The detector's performance is excellent, even at instantaneous luminosities exceeding the design value of $1 \times 10^{34}\,cm^{-2}s^{-1}$. The accelerator will be upgraded during Long Shutdown 3 (2024-2026), to allow it to achieve instantaneous luminosities of $5-7.5\times10^{34}\,cm^{-2}s^{-1}$, and the result of this upgrade is referred to as the High Luminosity LHC (HL-LHC). To cope with the harsher conditions in terms of radiation, particle rates and data volumes, the CMS detector will be substantially upgraded as well (CMS Phase-2 upgrade) [2]. In particular, the complete silicon tracking system will be replaced. The new device will feature improved radiation hardness, a reduction of the material budget and higher rate capability, and will be able to provide data to the first stage (Level 1) of the CMS trigger system. This will allow the trigger rate to be kept below 750 kHz.

The layout of the new tracker is shown in Fig. 1. The active area of the pixel detector will increase to 4.7 m^2, and its acceptance will extend to a pseudorapidity[1], η, of 4. The outer tracker consists of a cylindrical barrel with six module layers, accompanied by five disks per side in the forward direction. Only two module types will be used, where each module consists of two sensor layers (Sect. 2). The PS modules consist of one strip sensor and one macro-pixel sensor. The

[1]CMS uses a right-handed coordinate system, with the origin at the nominal interaction point, the x-axis pointing to the center of the LHC ring, the y-axis pointing up, and the z-axis along the anticlockwise-beam direction. Cylindrical coordinates (r, ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the z-axis. The polar angle θ is measured from the positive z-axis. The pseudorapidity η is defined as $-\ln[\tan(\theta/2)]$.

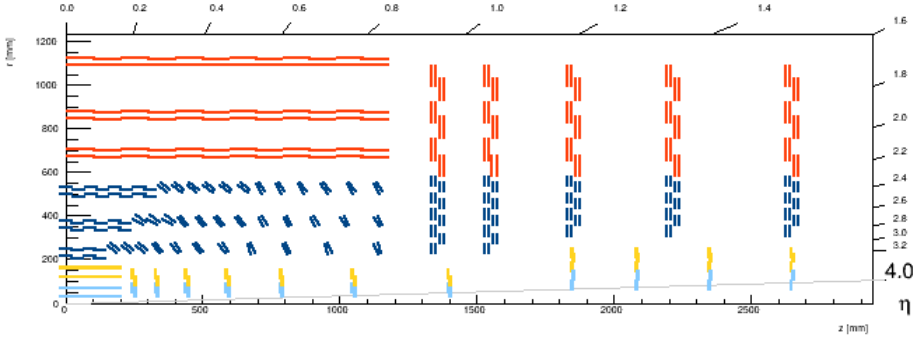

Figure 1. Schematic view of the Phase-2 tracker layout. One quarter is shown in the $r - z$ view, with the interaction point in the lower left corner. The pixel modules are shown in blue and yellow, the PS modules in dark blue, and the 2S modules in red.

macro-pixels will have a pitch of 100 μm and a length of 1.4 mm, while the strips will have a 90 μm pitch and a length of 5 cm. A total of 5332 PS modules will be installed at radii below 60 cm. At larger radii, 2S modules with two identical strip sensors will be used, each with two rows of 5 cm long strips at a pitch of 90 μm. It is foreseen that 8224 2S modules will be installed.

2 The p_T Module Concept and the 2S Silicon Strip Modules

The CMS outer tracker modules follow a new concept, referred to as the p_T module concept [2]. The goal is to provide tracking information at the bunch crossing frequency of 40 MHz to the Level 1 (L1) trigger. Due to bandwidth limitations this information has to be limited to tracks with a transverse momentum, p_T, above a certain value (e.g. 2 GeV). The concept is illustrated in Fig. 2, left. Charged particle tracks are bent in the 3.8 T magnetic field of CMS, with the bending radius depending on p_T. The hit patterns in the two closely spaced sensor layers are compared on-module, in the readout chip, and two-hit tracklets (so-called stubs) compatible with a programmable threshold are sent to the L1 trigger. Tracks are formed from stubs at the back-end, and merged with calorimeter and muon information in the High Level Trigger (HLT). Upon reception of a L1 trigger signal, the full event information is read out at 750 kHz.

The overall module concept is shared between 2S and PS modules. This work focuses on 2S modules, which will therefore be explained in more detail. A drawing of the 2S module is shown in Fig. 2, right. Each sensor has an area of about 10 cm $\times$ 10 cm and contains two rows of strips. The mid-planes of the sensors are separated by either 1.8 mm or 4.0 mm. The strips are wire-bonded to CMS Binary Chips (CBCs) [3], of which eight are located on each front-end (FE) hybrid [4]. Each CBC receives data from both the top and the bottom sensor. The data from the eight CBCs on one FE hybrid are re-formated and serialized by the Concentrator Integrated Circuit (CIC). The CIC forwards the data to the Low Power Gigabit Transceiver (LP-GBT) ASIC, which is a serializer and a distribution hub for trigger, clock, reset and I^2C signals. Data communication with the back-end is performed using optical fibers. The Versatile Transceiver (VTRx+) module houses the VCSEL array plus a laser driver ASIC, as well as the PIN diodes together with an amplifier ASIC.
The 2S service hybrid, explained in detail in the next section, is a flex hybrid arranged perpendic-

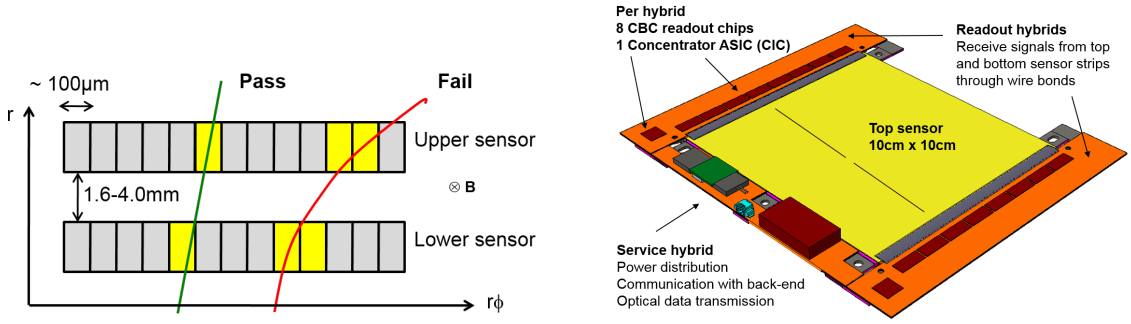

Figure 2. Left: illustration of the p_T module concept, showing a cut through the sensor layers. Hit strips are high-lighted in yellow. The green track with high p_T passes the requirement, while the red track does not due to its larger bending radius. Right: CAD-drawing of a 2S module, with sensors in yellow, front-end hybrids in orange, and CBC and CIC ASICs in red. On the service hybrid the shield of the power part is shown as red box, the input connector is shown in light blue, the left grey box shows the LP-GBT and the green box symbolizes the VTRx+ module.

ularly to the FE hybrids. It distributes the high and low voltages and houses the LP-GBT and the VTRx+ module.

3 The Service Hybrid of the 2S Module

The 2S module's service hybrid (SH) is a flex board that is laminated onto a carbon fiber (CF) stiffener of 500 μm thickness. The final version of the board will have four copper layers. Part of the board is folded around the stiffener. The bias voltage circuit is located on the back side, providing the bias voltage via two flexible Kapton tails to the back sides of the sensors. A temperature sensor is also integrated into one of the Kapton tails, and glued to one of the sensors. The LP-GBT, the VTRx+ and the low voltage (LV) power components are located on the top side. The LP-GBT is a low power version of the GBTx chip [5], a development by CERN. It receives the readout data at 320 Mb/s from the CIC on the FE hybrid, and forwards them to the VTRx+ at 5 Gb/s. The LP-GBT distributes trigger, clock and reset signals to the CIC, as well as sending I^2C commands to the CIC, the CBCs and the VTRx+. The LP-GBT is still under development. The SH houses a connector for the VTRx+, which is also under development at CERN. The challenge is to achieve a low profile form factor. Present prototypes still use some commercial components and are thus not radiation-tolerant; moreover, their geometry is still subject to change. In its present prototype version the VTRx+ comes as a small pluggable PCB, which mates with a connector on the SH.

Two supply voltages are required for the module. The CBCs, CICs, LP-GBT and VTRx+ require 1.25 V. The total current for this supply rail is estimated to be around 2.4 A. The VTRx+ requires in addition about 0.12 A at 2.55 V to drive the VCSELs. With an estimated power consumption of 4.7 W and 6.3 W for 2S and PS modules, respectively[2], the total tracker FE power will amount to around 72 kW. This power has to be provided via 80 m long cables by power supplies located in the counting room. The resistance of these cables leads to large Ohmic losses, and consequently

[2]These numbers include an estimate for the efficiency of the DC-DC converters, which are discussed in more detail below.

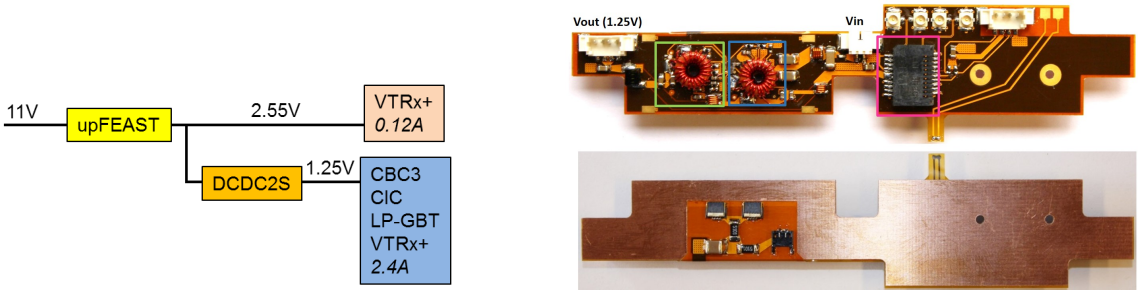

Figure 3. Left: the two-step DC-DC conversion powering scheme envisaged for the 2S module. Right: photos of the top side (top) and bottom side (bottom) of the SH prototype, with the FEAST2 and LTC3412A areas indicated by a green and blue box, respectively, and the VTRx+ connector framed by a pink box. The input and 1.25 V output connectors are labelled. The four connectors on the top right are used for electrical data transmission. The shield is not mounted. On the backside the HV circuit is visible.

to a low power system efficiency and a high heat load on the cables. In addition, voltage drops on the supply cables can be much larger than the actual ASIC supply voltages. A DC-DC conversion powering scheme is therefore foreseen, based on step-down DC-DC buck converters, building on the experience from the implementation of such a scheme for the CMS Phase-1 pixel detector upgrade [6]. In this scheme the power is supplied to the FE at a higher voltage, V_{in}, which implies a smaller current, I, for the same power value. This voltage is converted on-detector to the required one, V_{out}. Hence voltage drops (proportional to I) and power losses (proportional to I^2) are reduced by the conversion ratio, $r = V_{in}/V_{out}$, or r^2, respectively. A two-step DC-DC conversion scheme, with two DC-DC converters working in series, has been chosen to provide the two required voltages of 1.25 V and 2.55 V to the module, taking into account system efficiency, cabling aspects, and required development effort. Both DC-DC converters are located on the SH, so that each module comes with its own LV distribution. This has a number of advantages: each module works as a standalone entity, all cabling up to the module must only carry the small input current, which helps to reduce the material budget, and the distance between the DC-DC converter's output and the load is short, limiting subsequent voltage drops.

The two-step powering scheme is schematically shown in Fig. 3, left. In the first stage the upFEAST DC-DC converter by CERN will receive 11 V and convert this to 2.55 V, as required by the VTRx+. The second stage DC-DC converter, DCDC2S by CERN, converts 2.55 V into 1.25 V. Both these DC-DC converter chips are still under development. They both require an air-core inductor as the energy storage element (ferrite inductors would saturate in the CMS magnetic field), a number of passive filter components and an electro-magnetic shield.

It should be noted that the PS modules will use similar SHs, although split into a power board and a data transmission board, since the PS modules are much narrower. While the overall concept is the same, the details differ. For example, a third supply voltage is required, and the data transmission rates are higher.

3.1 Service Hybrid Prototypes

A prototype of the 2S module SH has been developed, as shown in Fig. 3, right. Due to the fact that all active components are still under development and are therefore currently not available

for use, it differs in several aspects from the final design. The upFEAST DC-DC converter is replaced by its predecessor, the FEAST2 ASIC [7]. The functionality of the two chips is the same, however the upFEAST will feature increased radiation-hardness, to be compatible with HL-LHC applications. An air-core toroid with an inductance of 200 nH and a DC resistance of 38 mΩ is used, and the switching frequency is set to 2 MHz. The DCDC2S is replaced by a commercial device (LTC3412A). The inductor is the same as the one used for FEAST2, and this DC-DC converter is set to switch at 2.45 MHz. Pi-filters are implemented at the LV input and output, as well as between the two DC-DC converters. Both DC-DC converters reside under a common shield. A connector for the VTRx+ prototype is provided. In the absence of the LP-GBT, four miniature electrical connectors are implemented, allowing (differential) data to be fed to the VTRx+ from the outside, and data to be read back. The HV circuitry is integrated on the fold-over region.

The prototype board has two 18 μm thick copper layers. The board was laminated onto an FR4 stiffener, which has 18 μm thick copper surface layers to resemble the electrical properties of CF.

Even though these prototypes are far from the final product, they are very useful in many respects. For example, they allow the general behaviour of a two-step DC-DC conversion powering scheme to be studied, the electromagnetic shielding to be developed, experience with the data transmission to be gained, and system tests to be performed by using them to power 2S prototype modules, allowing the impact of the DC-DC converters on the module's performance to be studied.

4 Results

4.1 Electromagnetic Shielding

The operation of a DC-DC converter with an external inductor makes the usage of an electromagnetic shielding inevitable, so that the silicon sensors and the FE electronic components are protected from electromagnetic radiation. The shielding has to obey certain geometrical constraints and should be as light as possible.

Prototypes of the shield have been produced using two different technologies. The first prototype (Fig. 4, left and center) is made from an etched aluminium foil of 150 μm thickness. An additional layer of tin of about 5 μm thickness was added to ensure that the shield can be soldered to the PCB. The corners are spot-welded, avoiding the use of large amounts of solder. With this technology very thin structures, such as pins for alignment or notches to spare out traces on the PCB, can be manufactured. The second prototype (Fig. 4, right) is based on a plastic body, made by rapid prototyping, onto which 60 μm of copper is galvanically deposited.

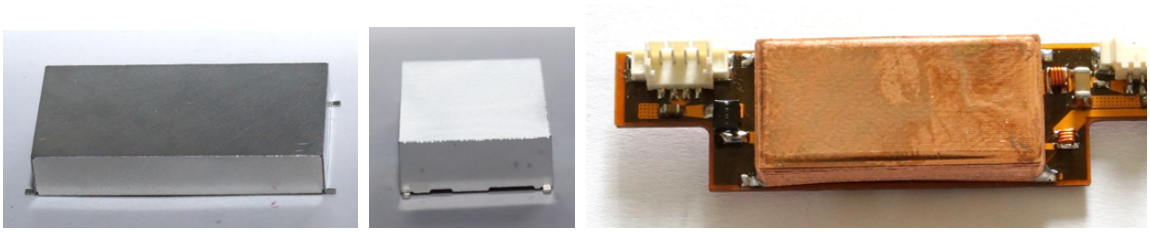

Figure 4. The left and center photos show the aluminium shield, with pins and notches clearly visible. The right photo shows the copper shield, mounted on the SH.

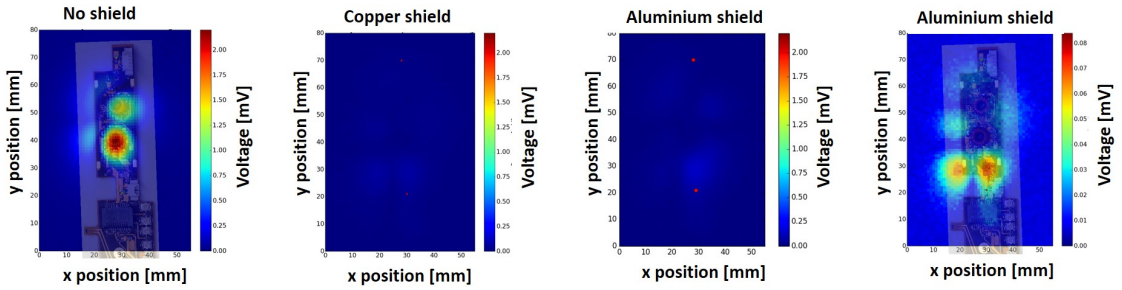

Figure 5. Scan of the magnetic field, measured in Millivolts. The maximum measured emission is plotted in a two-dimensional representation, where x and y refer to the axes of the scan table. From left to right, measurements are shown without shield, with the copper shield, and twice with the aluminium shield. The left three pictures share the same voltage scale, while the rightmost picture shows a zoom, with the maximum decreased from 2 mV to 0.08 mV. Photos have been superimposed onto two of the scans to illustrate where the emissions originate. The small red dots represent alignment marks, used to position the SHs and to superimpose the photos.

Both shields have been mounted onto SHs and the shielding performance was measured using an automated scan table, where a pick-up probe is moved in 1 mm steps across the SH. The picked up signal is measured with a spectrum analyzer and either the peak emission or the mean emission in a given frequency band is compared to the corresponding measurements without the shield. The results are shown in Fig. 5. The peak emissions are reduced drastically by both prototypes: by a factor of 30 for the aluminium shield and by a factor of 16 for the copper shield. This is plausible, as the skin depth at a frequency of 2 MHz, corresponding to the FEAST2's switching frequency, amounts to 58 μm for aluminium and to 46 μm for copper, which is close to the copper shield's thickness. As is visible from the rightmost plot in Fig. 5, the remaining emissions are at a low level and originate from components located outside the shield.

Overall the aluminium shield is preferred, as it performs slightly better, represents less material and allows the manufacture of finer structures.

4.2 Common Mode and Differential Mode Noise Spectra

In DC-DC buck converters two power MOSFETs are used to alternately connect and disconnect the load to the input voltage. This switching of large currents at MHz frequencies results in noise propagating through the power lines, both at the converter's input and output. Two modes are distinguished: Differential Mode (DM) noise refers to the ripple on the power line, while Common Mode (CM) noise refers to noise propagating in parallel through the power and return line, and returning through the system ground via parasitic coupling. In a dedicated set-up both noise modes were measured at the SH's input and output. The DM and CM spectra are shown in Fig. 6. In the DM spectrum only peaks from the first converter stage (FEAST2) are visible, while peaks associated with both conversion stages are present in the CM spectrum. For quantification both the height of the switching peak and the quadratic sum of all peaks up to 30 MHz are considered.

Figure 7 shows quantitative comparisons under various conditions. The left plot presents results for all four noise modes for two different inductors, the default one with 200 nH and one with 430 nH. The FEAST2 switching peak is decreased by using a larger inductance for all modes, while

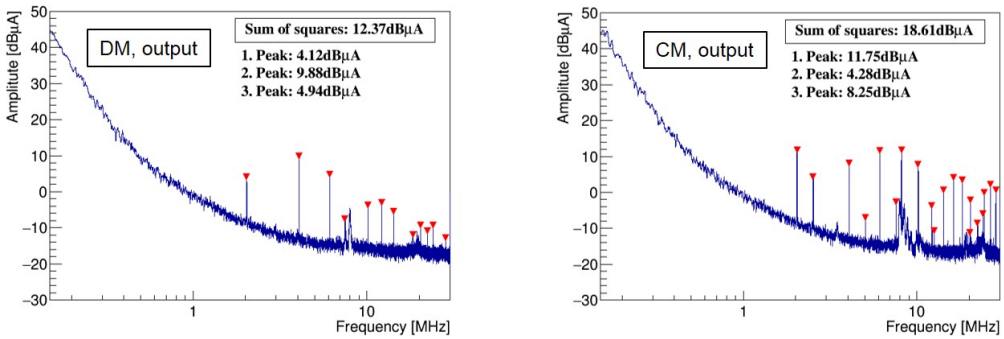

Figure 6. DM (left) and CM (right) noise spectra as measured at the output of the SH.

the noise of the second stage increases in almost all modes. The total CM noise is increased, but a decrease of the DM noise at the output is achieved. This improvement in noise has to be balanced against integration aspects and the material increase accompanying a larger inductor.

In a second study the geometry of the shield was varied. Since both converters are located under a common shield, the emission of one DC-DC converter could couple to the other DC-DC converter. To study this potential effect, the common shield was replaced by two separate shields as well as with a shield with an internal separation wall. As shown in Fig. 7, right, neither approach to separate the DC-DC converters leads to a significant reduction in noise; on the contrary, the separate shields increased the CM noise. The conclusion is that mutual influence of the DC-DC converters is – if at all – a small effect, and that a common shield with a simple geometry is sufficient.

4.3 Power Efficiency

In a two-step powering scheme the power efficiency, defined as the output power divided by the input power, is a critical aspect, as the individual efficiencies of the two stages multiply. The targets are 75 % and 85 % for the first and second stage, respectively, leading to a total system efficiency of 65 %. Both the combined efficiency as well as the individual efficiencies have been measured on the SH, where the measurement of the individual efficiencies required a modification of the board. At present, the total efficiency that has been achieved is 48 % when using the parameters as expected for the final application (Fig. 8). This is driven by the second stage, as the efficiency of

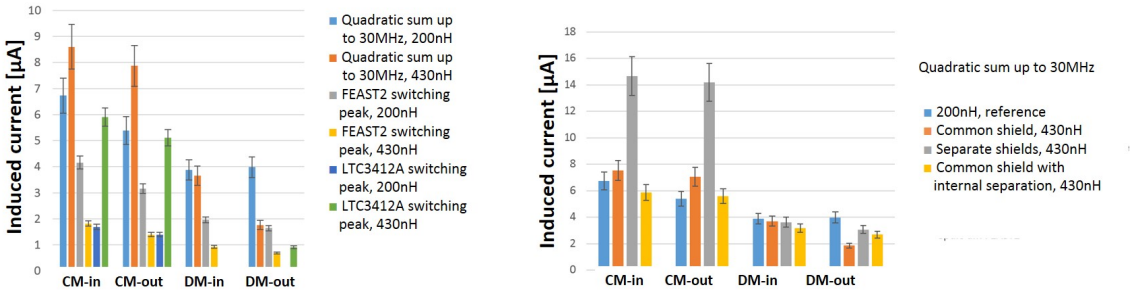

Figure 7. Comparison of DM and CM noise at the input and output, for different inductors (left) and shields (right). In the left plot the noise is also shown separately for the FEAST2 and LTC3412A converters.

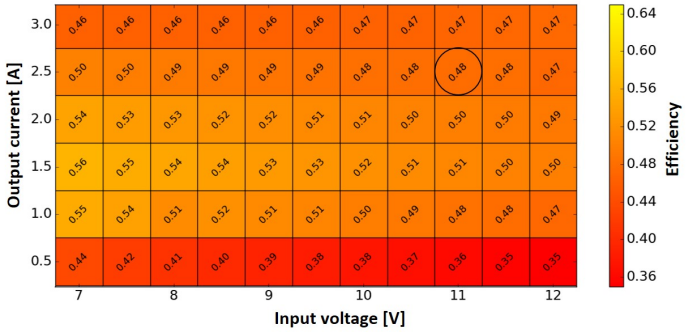

Figure 8. Efficiency measured behind both cascaded DC-DC converters versus input voltage to the FEAST2 chip and output current of the LTC3412A chip. The working point for the final application is circled.

the commercial converter drops rapidly with load current (Fig. 9, right). The efficiency of the first stage, however, is close to the target value (Fig. 9, left). This aspect will have to be revisited once the final DC-DC converters are available.

4.4 System Tests with a 2S Mini-Module

System tests have been performed to study potential effects of the powering from the SH on the module performance. Since full 2S modules were not available for the test, a so-called 2S mini-module with two CBC2 readout chips and two sensors, each with one row of 5 cm long strips, has been used. The SH was used to power the module, and was itself powered from a prototype power supply with line drop recovery instead of sensing, as envisaged for the final application, via a 80 m long cable. Scans of occupancy versus threshold were performed and the noise was extracted from the width of the resulting S-curves. The noise was measured for various positions of the SH, where the closest position, resembling the SH's position in a module, is shown in Fig. 10, left. The results are summarized in Fig. 10, right. No significant differences in noise were observed between powering the module directly from a lab power supply and powering through the SH, as long as the DC-DC converters were shielded. Without the shield, an increase in noise is observed, as expected.

In a second study the prototype VTRx+ module was used. It was powered from the SH and

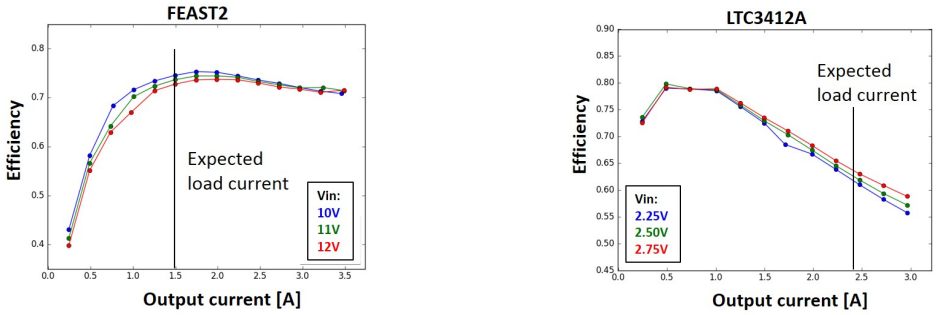

Figure 9. Power efficiency of the FEAST2 (left) and LTC3412A (right) versus their output currents, for various input voltages. The vertical lines indicate the approximate currents expected in the final application.

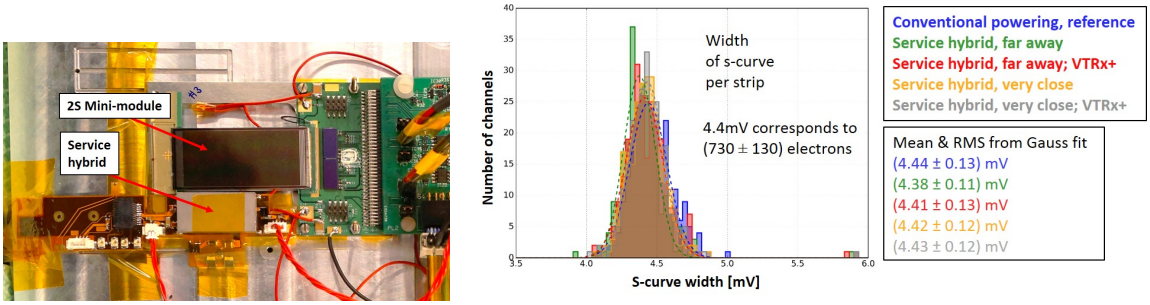

Figure 10. Photo of the system test setup with a 2S mini-module (left), and histograms of the noise of all strips of one CBC2, measured with conventional powering (blue), a SH placed far away (green) and as close as shown in the photo (yellow), plus measurements with data flowing through the VTRx+ (red and grey).

a Gigabit Link Interface Board (GLIB) [8] was used to push random data through the VTRx+ at 5 GB/s. These data were then looped back to the GLIB. No bit errors were observed and the module performance was not affected by this high-speed digital data traffic on the SH.

Finally the dynamic behaviour of the power system was studied with an oscilloscope and a dynamic load. Switching on and off was smooth and overshoots for large load reductions were acceptable, e.g. the output voltage of the SH increased by about 80 mV for 10 μs for a drastic reduction of the load from 2 A to zero.

5 Summary and Outlook

A two-step DC-DC conversion powering scheme was implemented on the service hybrid for the 2S modules of the CMS Phase-2 Tracker upgrade. Various aspects of performance have been studied and no major problems were identified. The next steps include the integration of the final DC-DC converters and using the SH to operate a full-size 2S module.

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