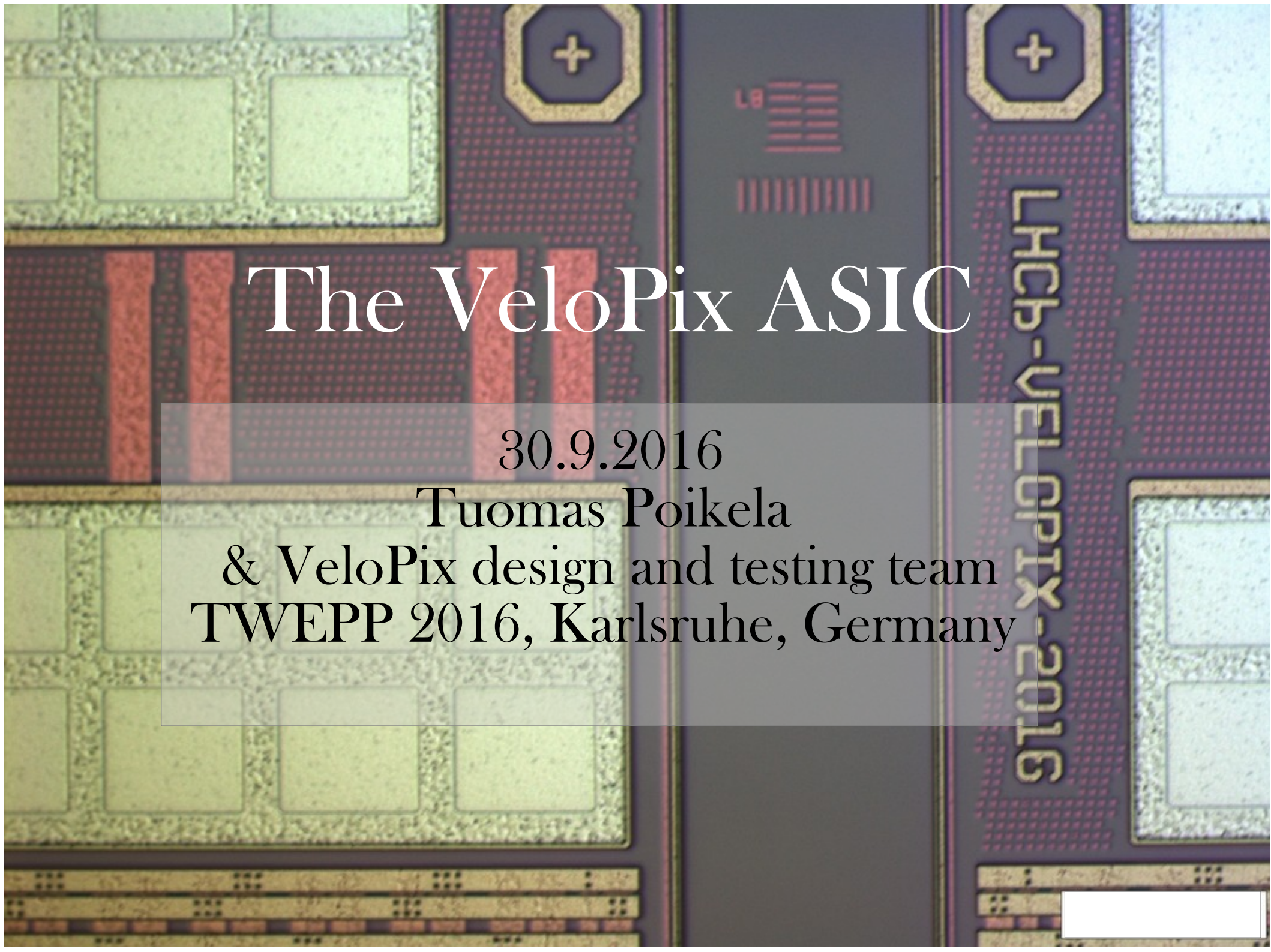


The VeloPix ASIC

30.9.2016

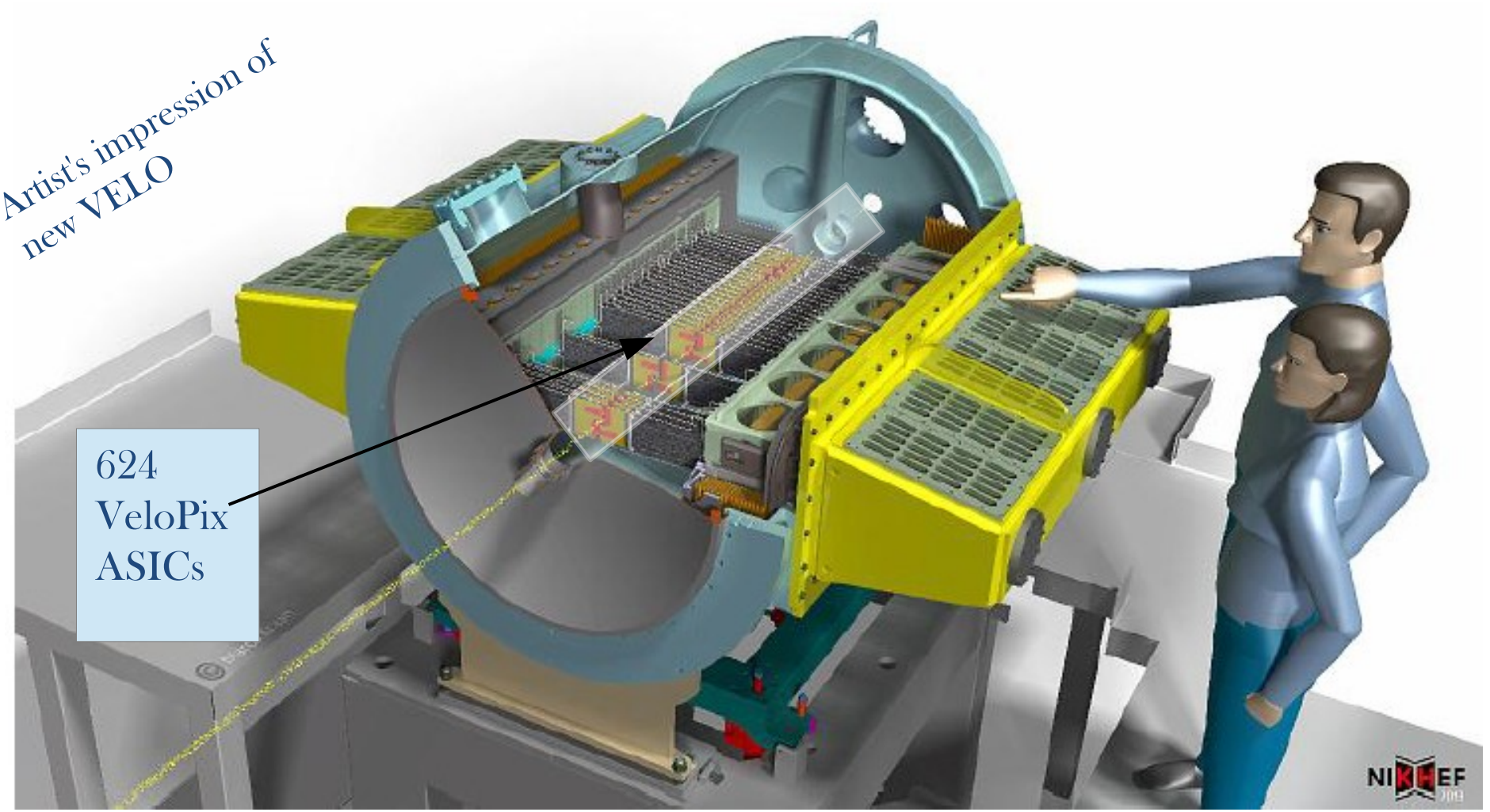
Tuomas Poikela
& VeloPix design and testing team

TWEPP 2016, Karlsruhe, Germany

Overview

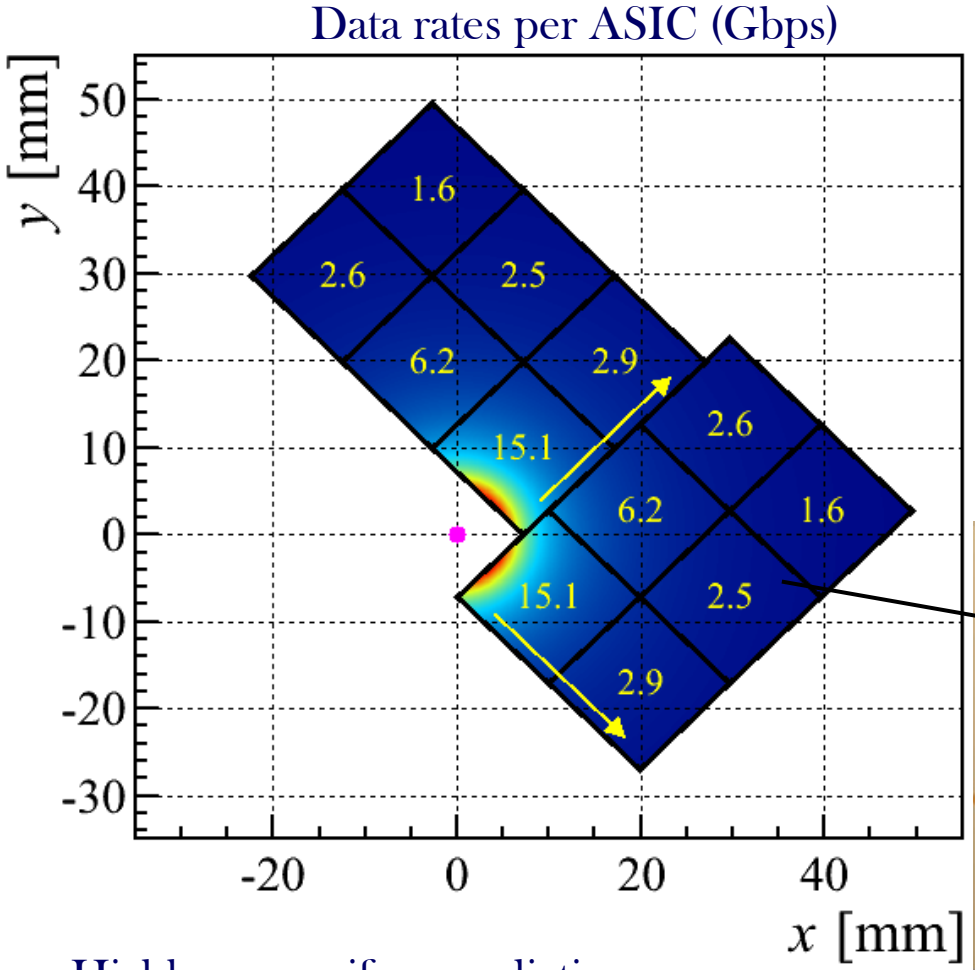
- A quick VELO upgrade overview
- Chip architecture
- First measurements
- Summary & future plans

The LHCb VELO upgrade



TWEPP 2016 : Sneha Naik “On-detector electronics for the LHCb VELO Upgrade”

VeloPix ASIC module



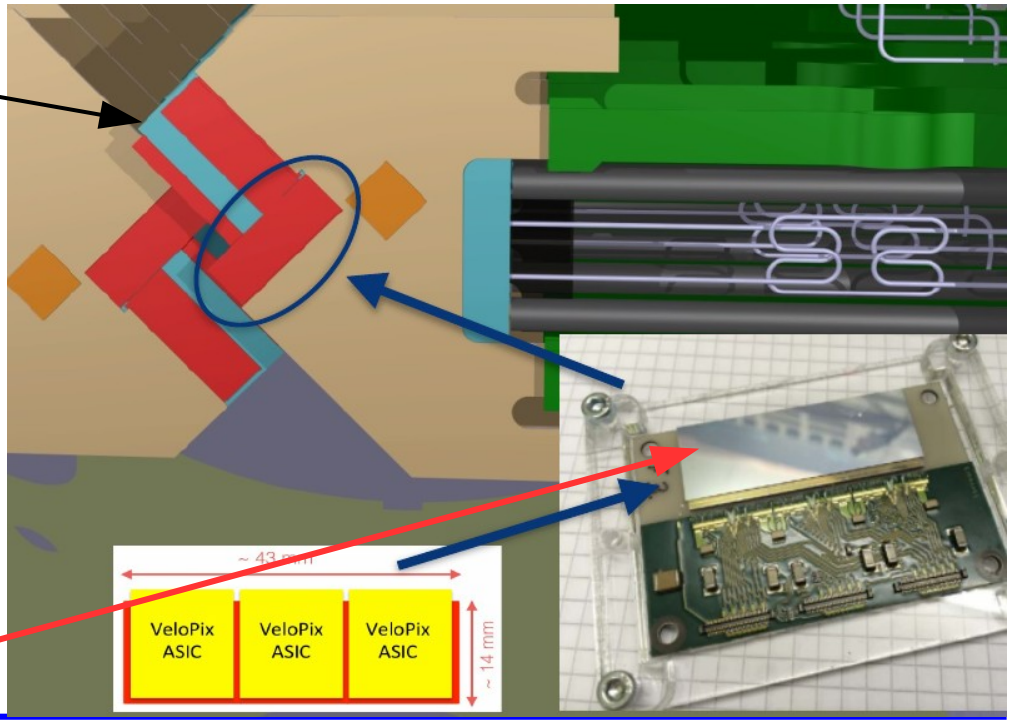
The hottest chips 5.1 mm from the beam

Data per chip: ~15.1 Gbps, 2.9 Tbps for VELO

The module installation during the CERN Long Shutdown 2 (LS2) 2019/2020.

Highly non-uniform radiation within the hottest chip: From 50 to 400 Mrad.

Hybrid pixel readout chip: Bonded to a sensor.

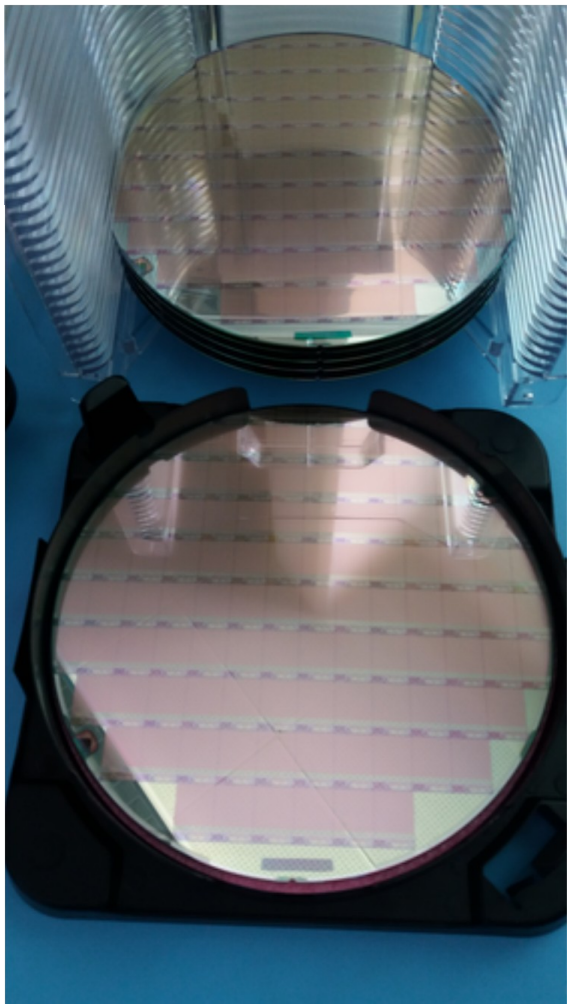


Quick comparison

Feature	VeloPix (2016)	Timepix3 (2013)
Readout type	Continuous, trigger-less, binary	Continuous, trigger-less, ToT
Timing resolution/range	25 ns, 9 bits	1.5625 ns, 18 bits
Power consumption	< 1.5 W cm^{-2}	< 1.0 W cm^{-2}
Pixel matrix, pixel size	256 x 256, 55 um x 55 um	256 x 256, 55 um x 55 um
Radiation hardness	400 Mrad, SEU tolerant	-
Peak hit rate	800 Mhits/s/ASIC 50 khits/s/pixel	80 Mhits/s/ASIC
Sensor type	Planar silicon, e- collection	Various, e- and h+ collection
Max. data rate	20.48 Gbps	5.12 Gbps
Technology	130 nm CMOS, tech A	130 nm CMOS, tech B

Project overview

- Design started in June 2013 (after Timepix3 submission)
- Change of technology (130nm → 130nm)
- The chip was submitted May 26th 2016, wafers received on 31st August
- Fabricated (and diced) chips back at CERN on 7th September
- Production testing later this year (624 chips)
- Irradiation campaign in the future with sensors bonded



VeloPix wafers

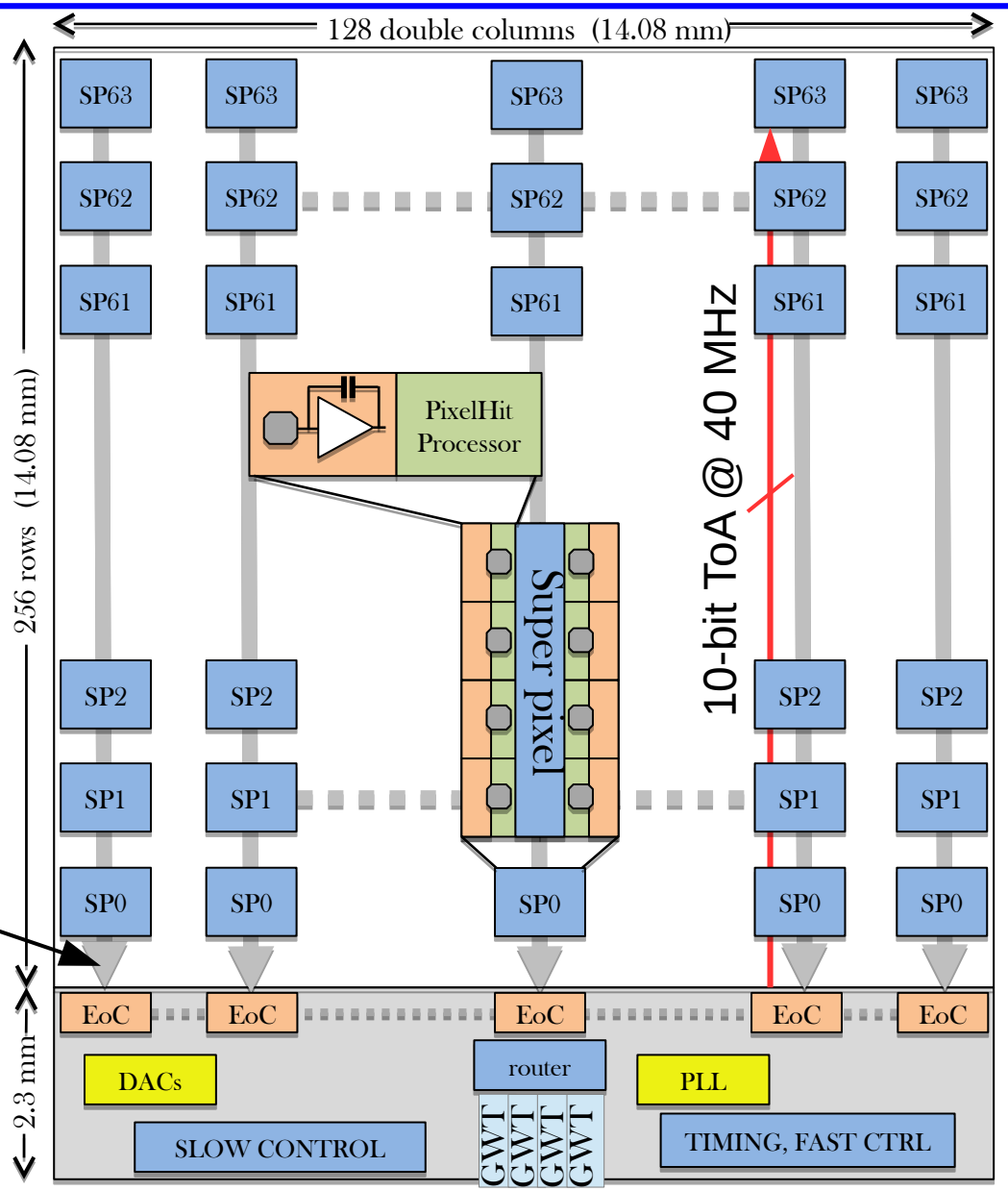
Chip architecture

The pixel matrix:
256 x 256 pixels
128 x 64 super pixels (2x4 pixels each)

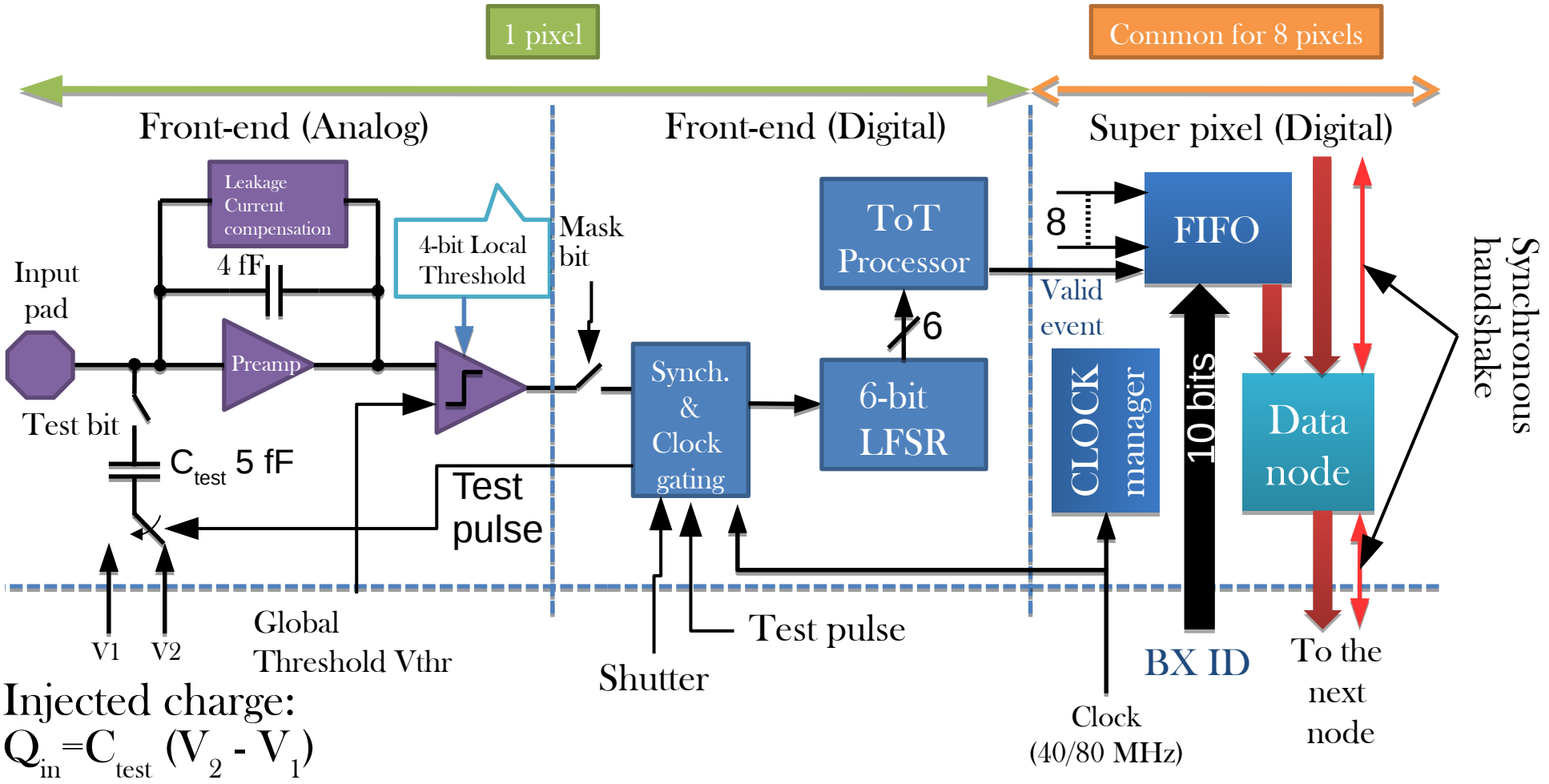
Architecture:
Packet-based, 8 pixels/packet + 9 bit time stamp

Leads to 30% reduction in data rate

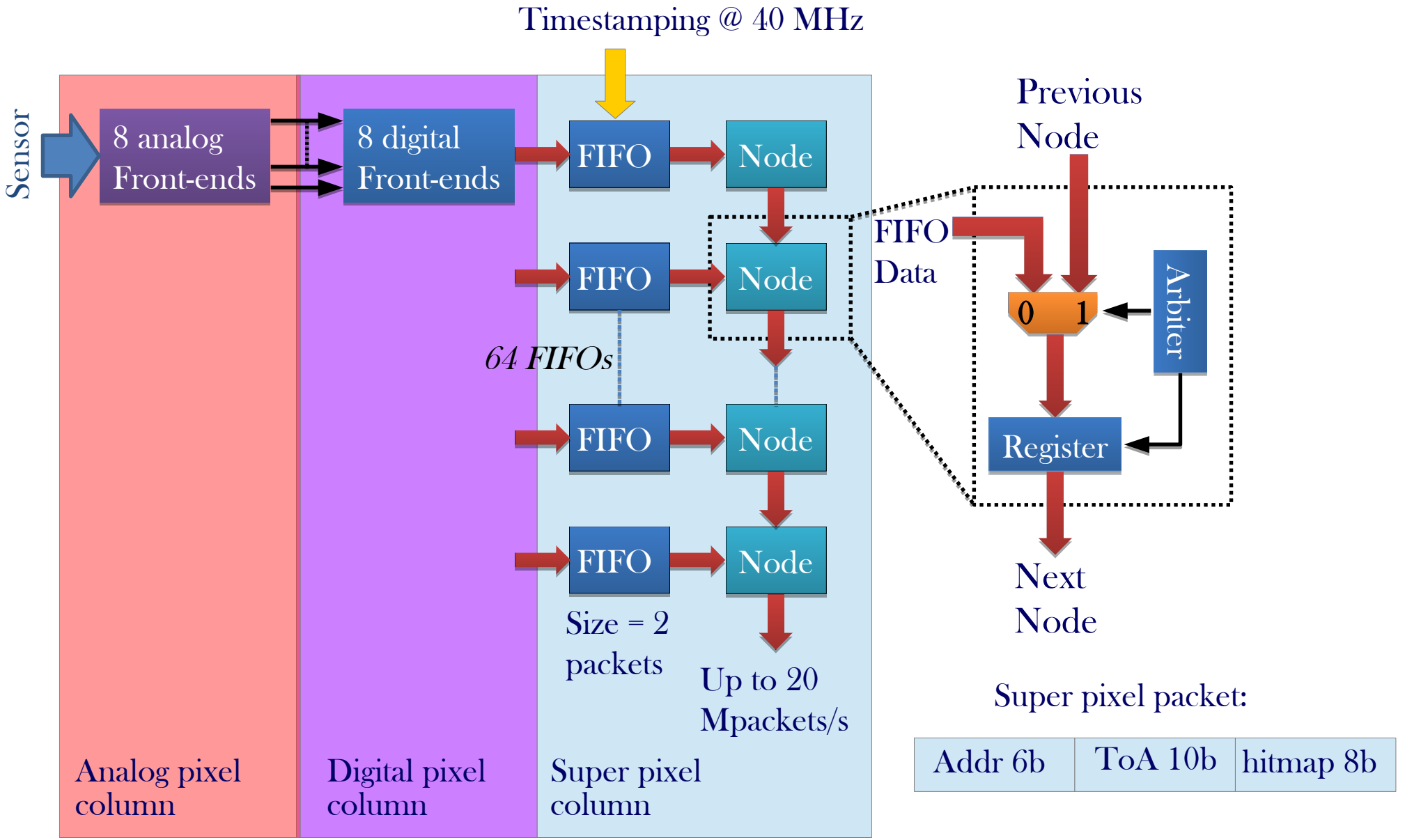
Data-driven, 20Mpackets/s / double column
- Timepix3 rate: 1.2 Mpackets/s



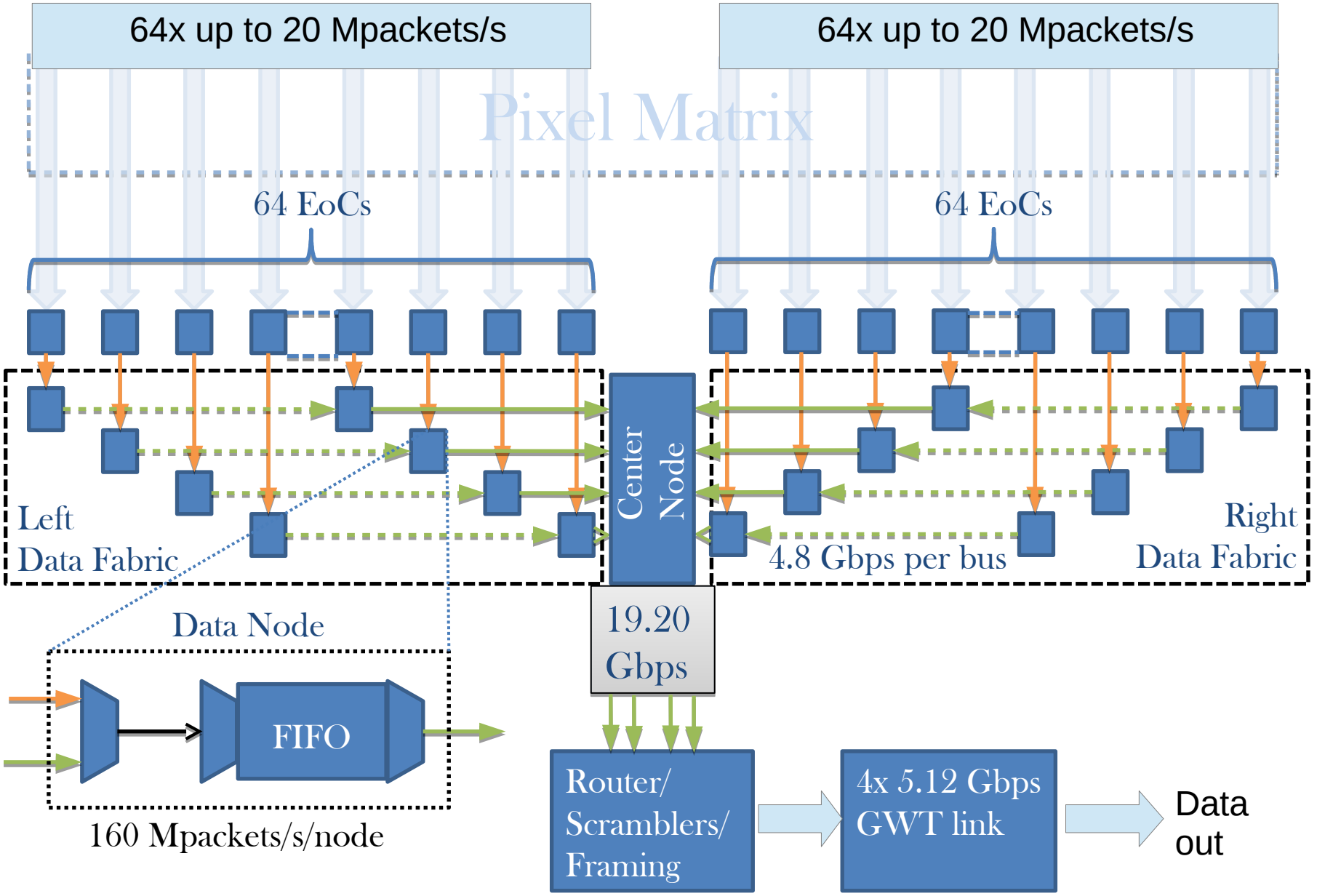
Front-end architecture



Double column datapath

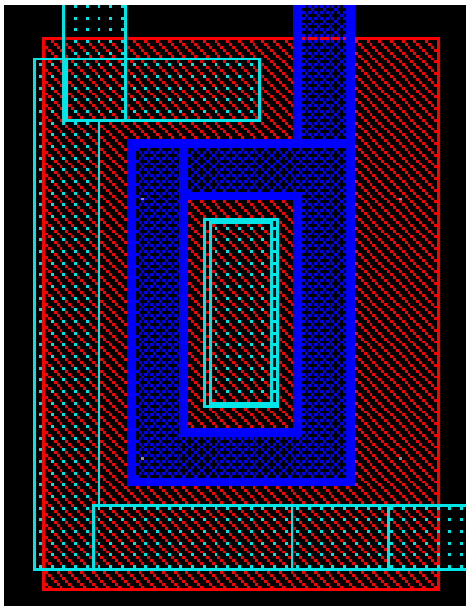


Periphery datapath

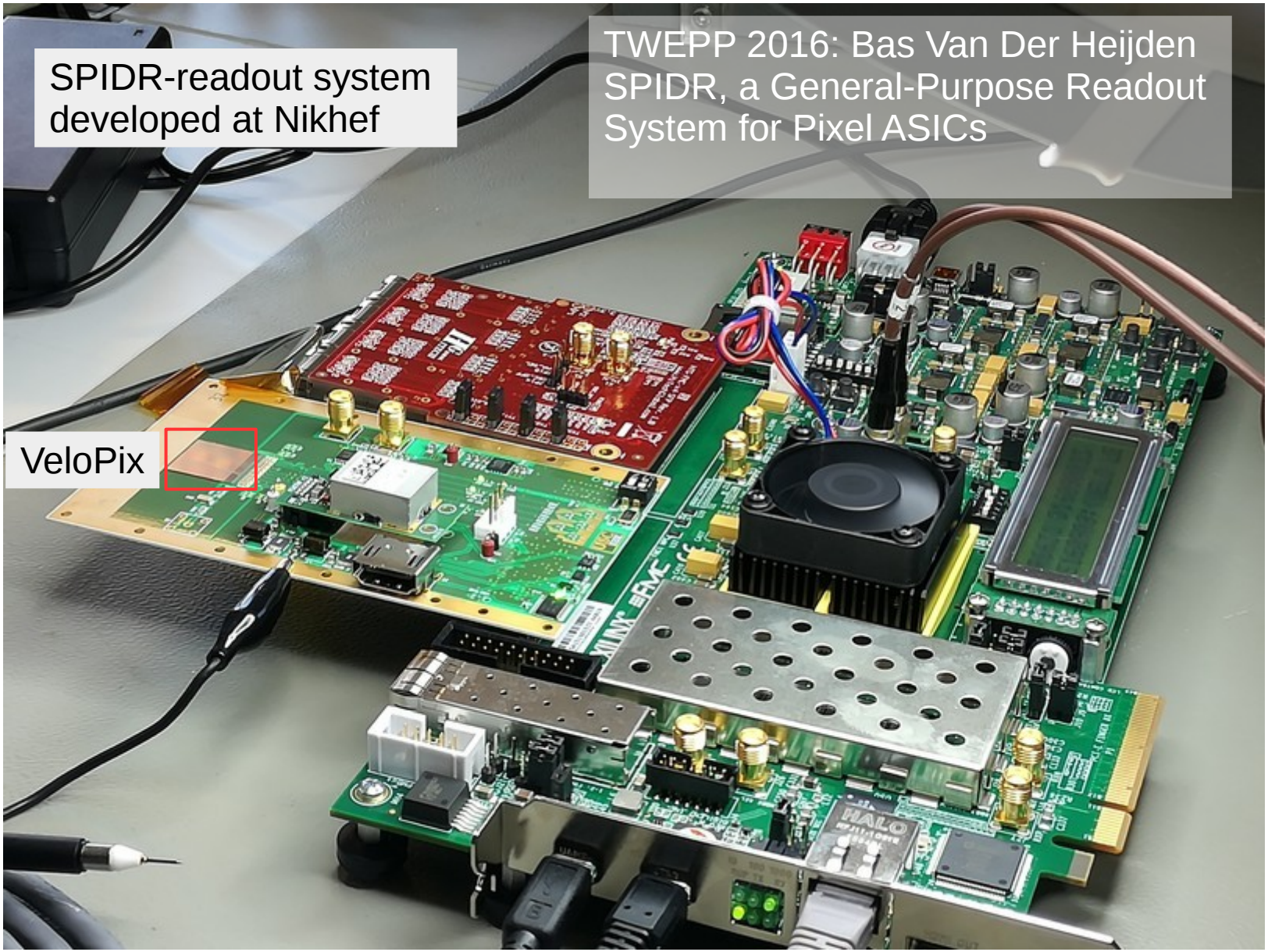


TMR/RadHard design

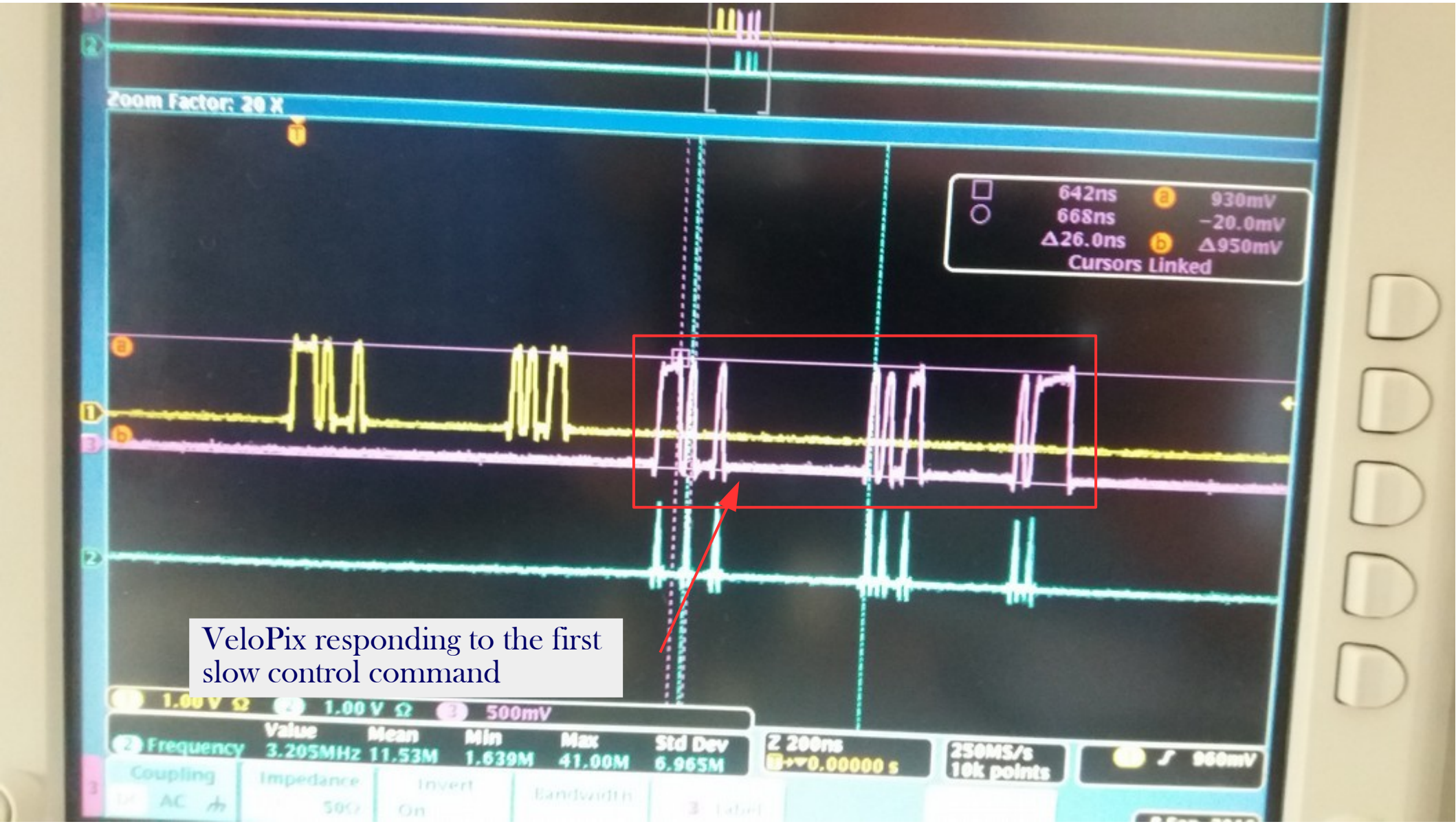
- Manual triplication (except configuration registers)
- Pixel data flip-flops (FF) unprotected
- Full TMR in FSM & configuration FFs, pixel config latches
- No on-chip SRAM!
- NMOS ELT transistors used in analog front-end
- Std cell library characterized at 400 Mrad, High-Vt NMOS
- Corner used for syn/PnR: slow process, VDD 1.08V, 400 Mrad, 25°C



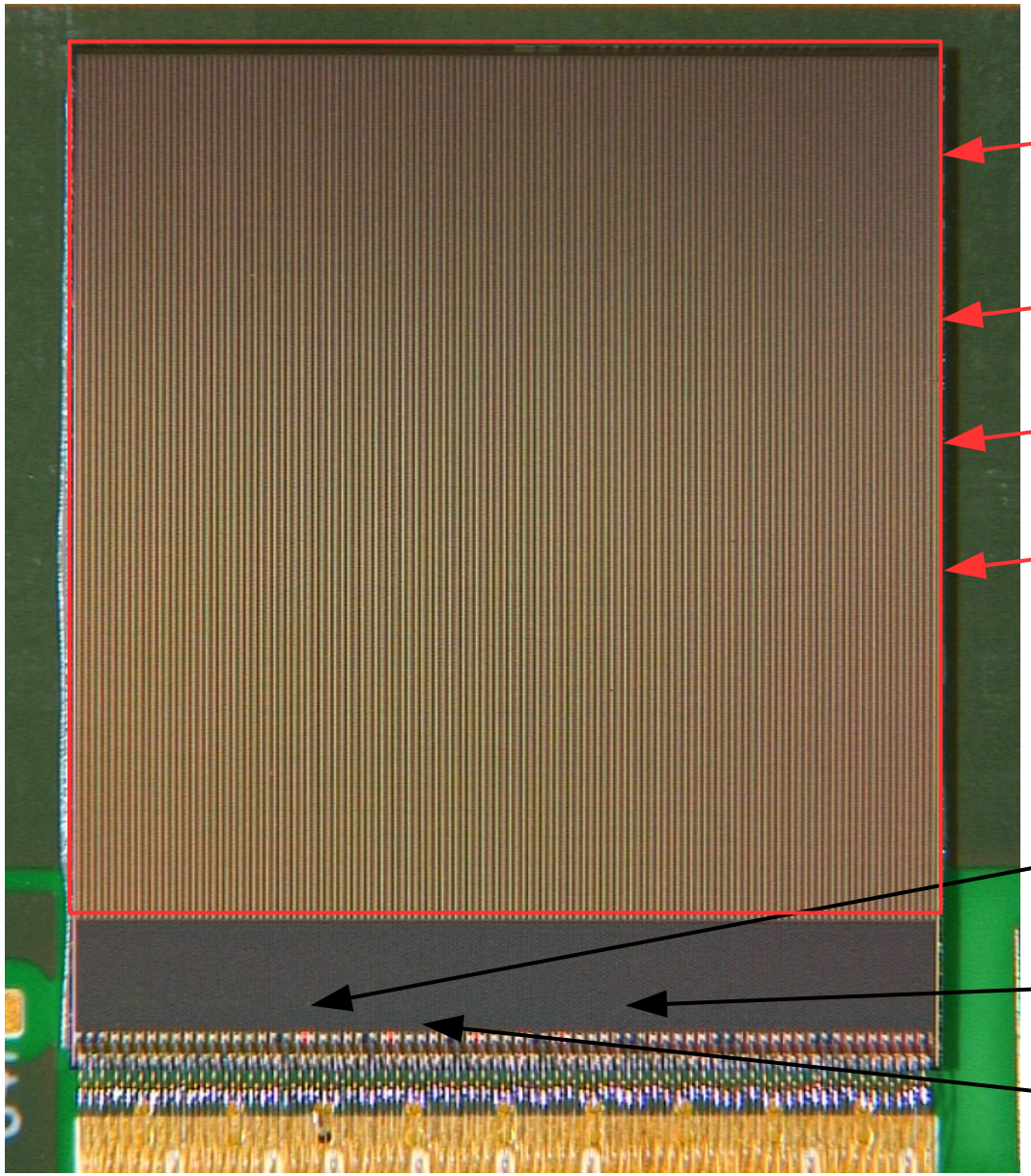
First debugging results



First signs of life



Tests performed so far



The pixel matrix resettable, readable and writable

Analog & Digital front-ends respond to test pulses correctly

Shutter/test pulse logic works.

Packet latency (low rate) corresponds to expected

Slow control responds, register R/W access works

PLL locked, running at 320 MHz

Timing and fast control working

First measurements

- Power:
  - Analog
  - Digital (IDLE), matrix clocking, time stamp bus
- DAC (work as expected)
- GWT eye diagram
- S-curves using analog test pulse
- Noise
- Threshold variation
- Super pixel packet latency

Power consumption (1.2V)

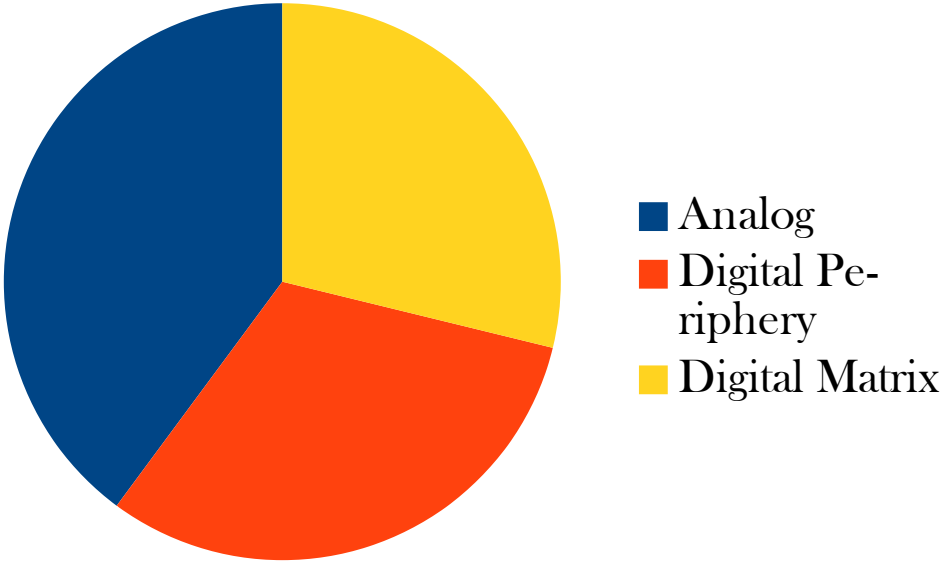
- Analog: 387 mA, 476 mW
- Digital:
  1. After chip power up: 374 mW
  2. Matrix clock enabled: 694 mW
  3. ToA counter enabled: 718 mW

Clock: +320 mW

ToA bus power +24 mW

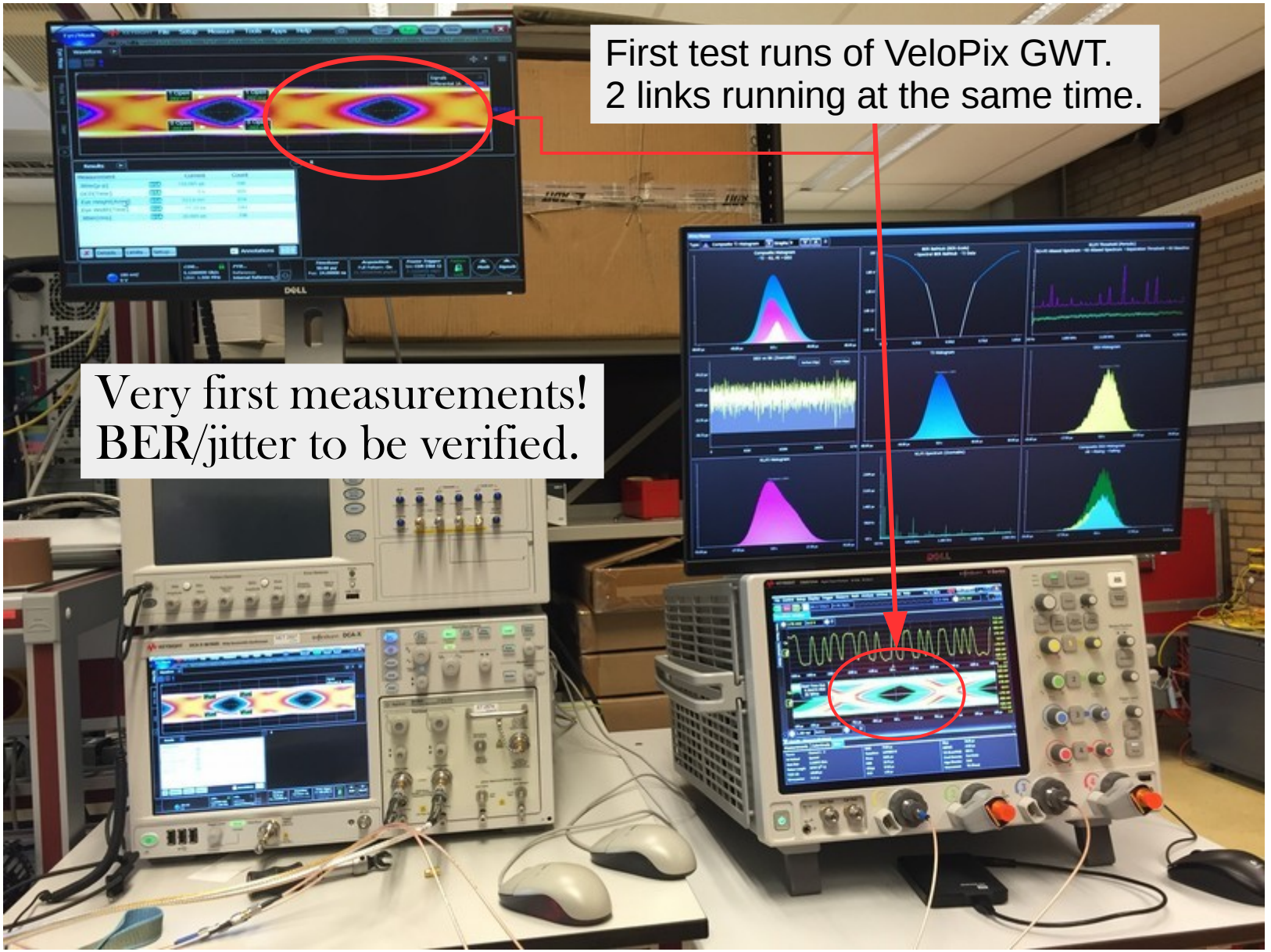
Total: 1.2 W (0.52 W/cm^2)

(Meets < 1.5 W/cm^2)

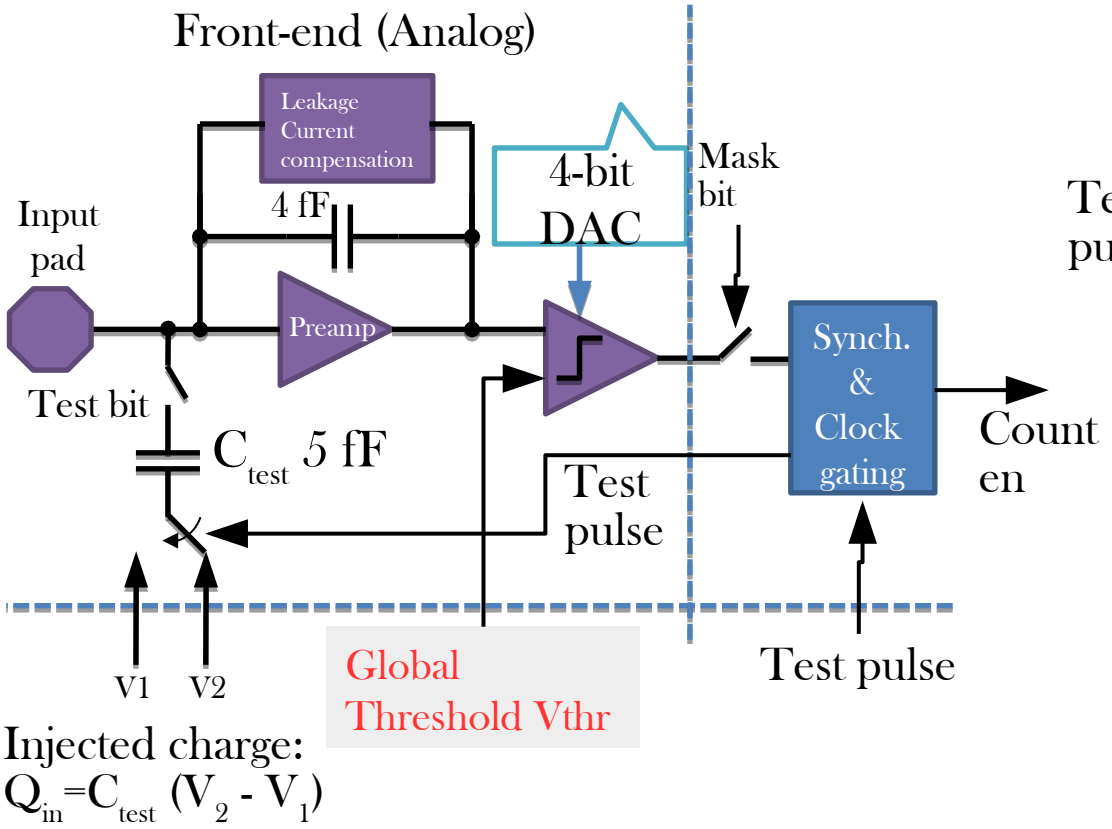


TODO: Measurement with high rate

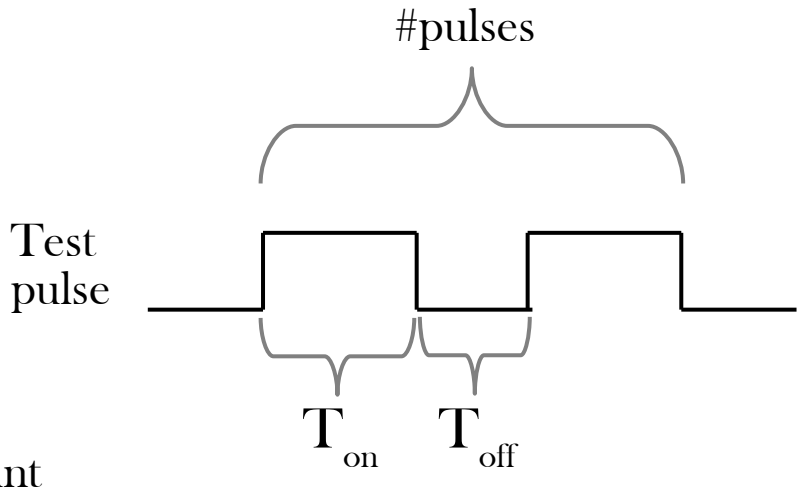
GWT Eye diagram @ 5.12Gbps

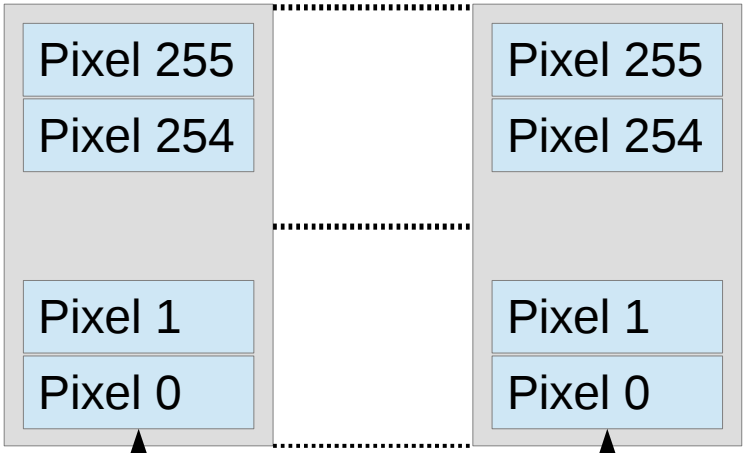


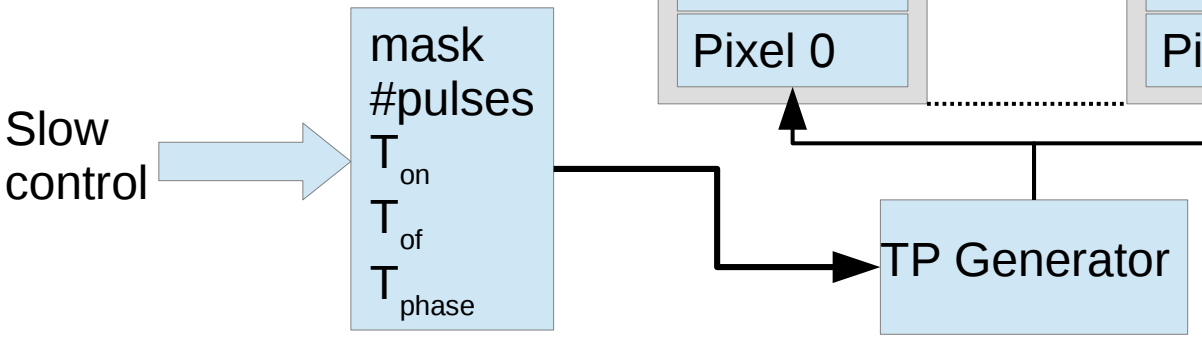
Measurements with test pulse



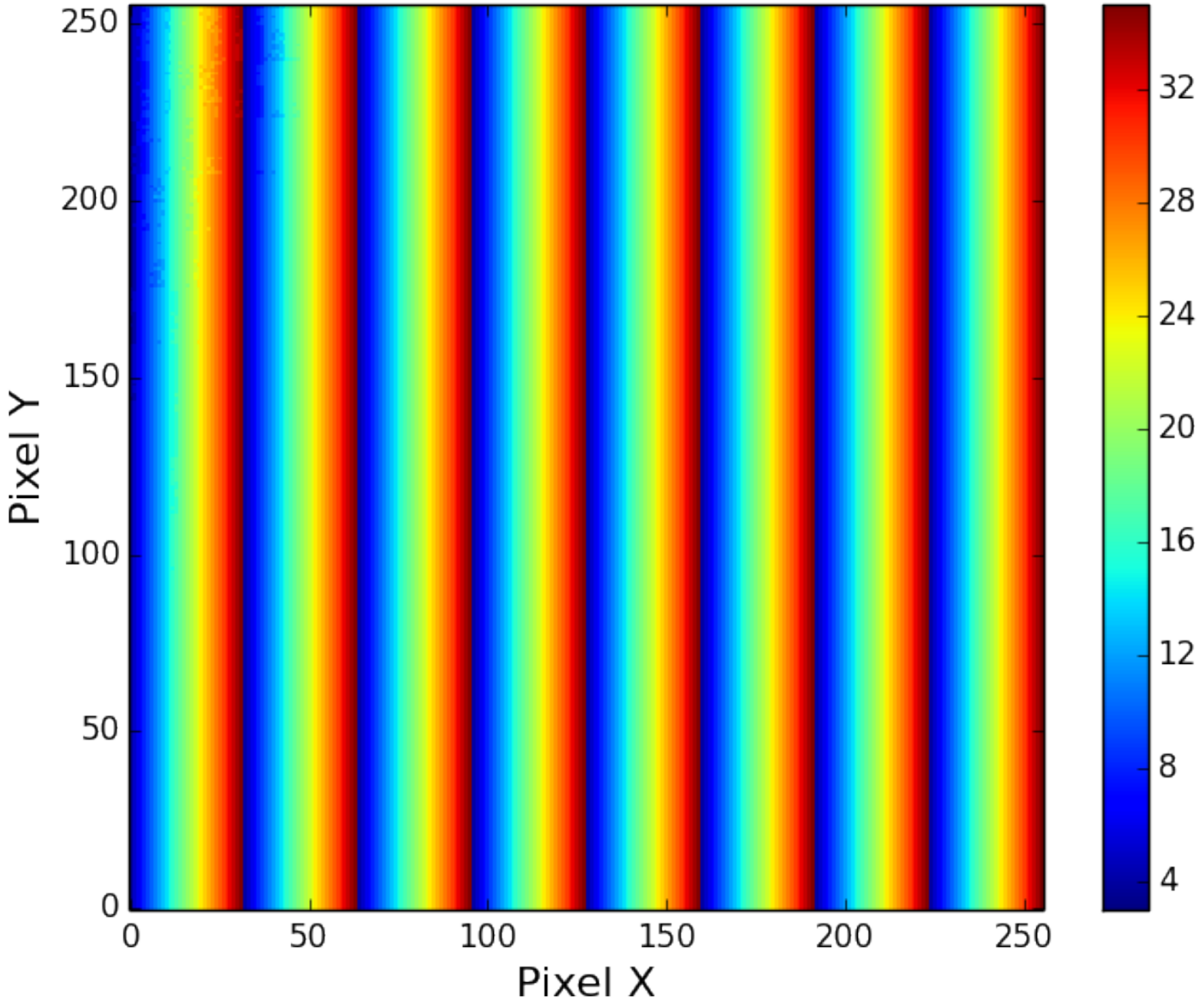
Injected charge:
$Q_{in}=C_{test}\ (V_2 - V_1)$

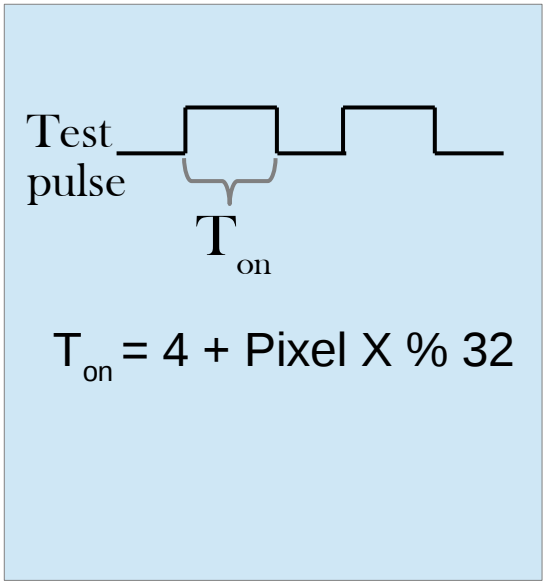






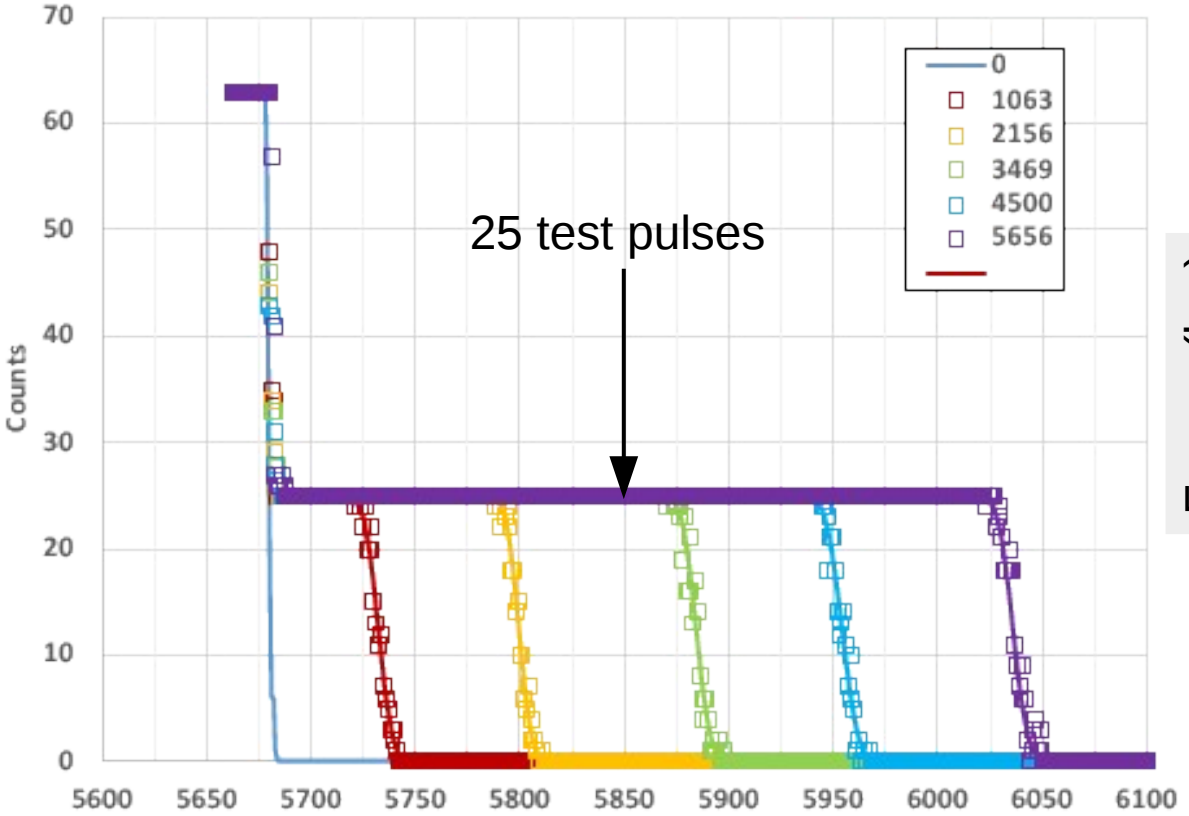
Digital: ToT mode

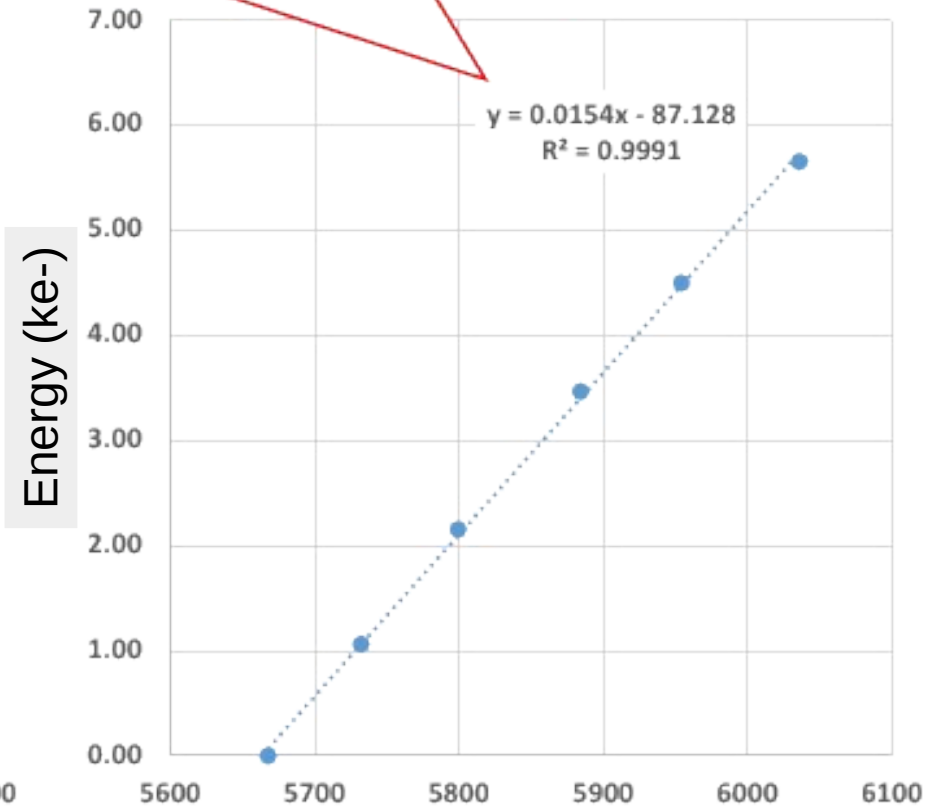




Analog test pulses in one pixel

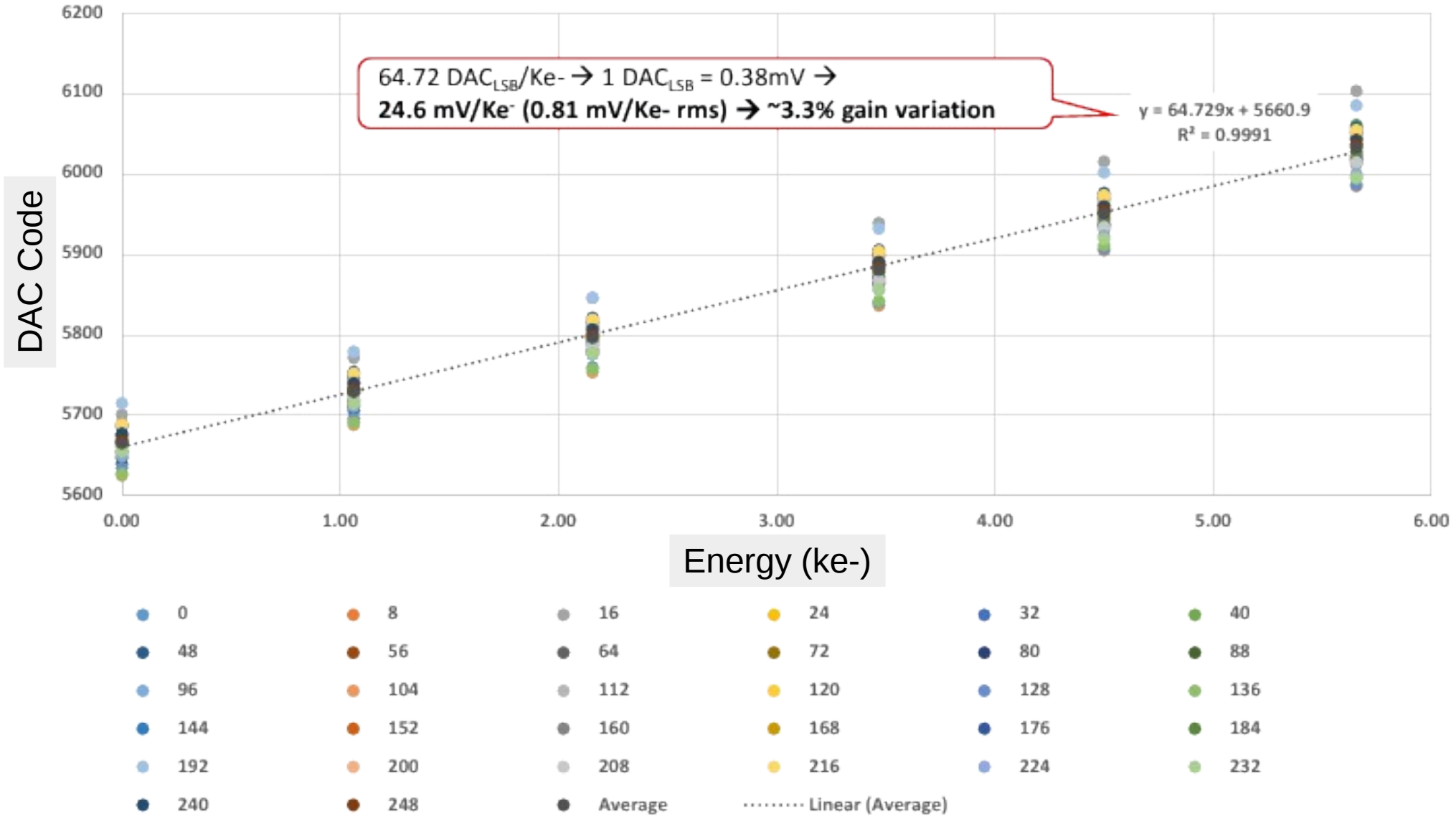
0.0154 ke-/DAC_{LSB} => 1 DAC_{LSB} = 0.38 mV => 24.6 mV/ke-



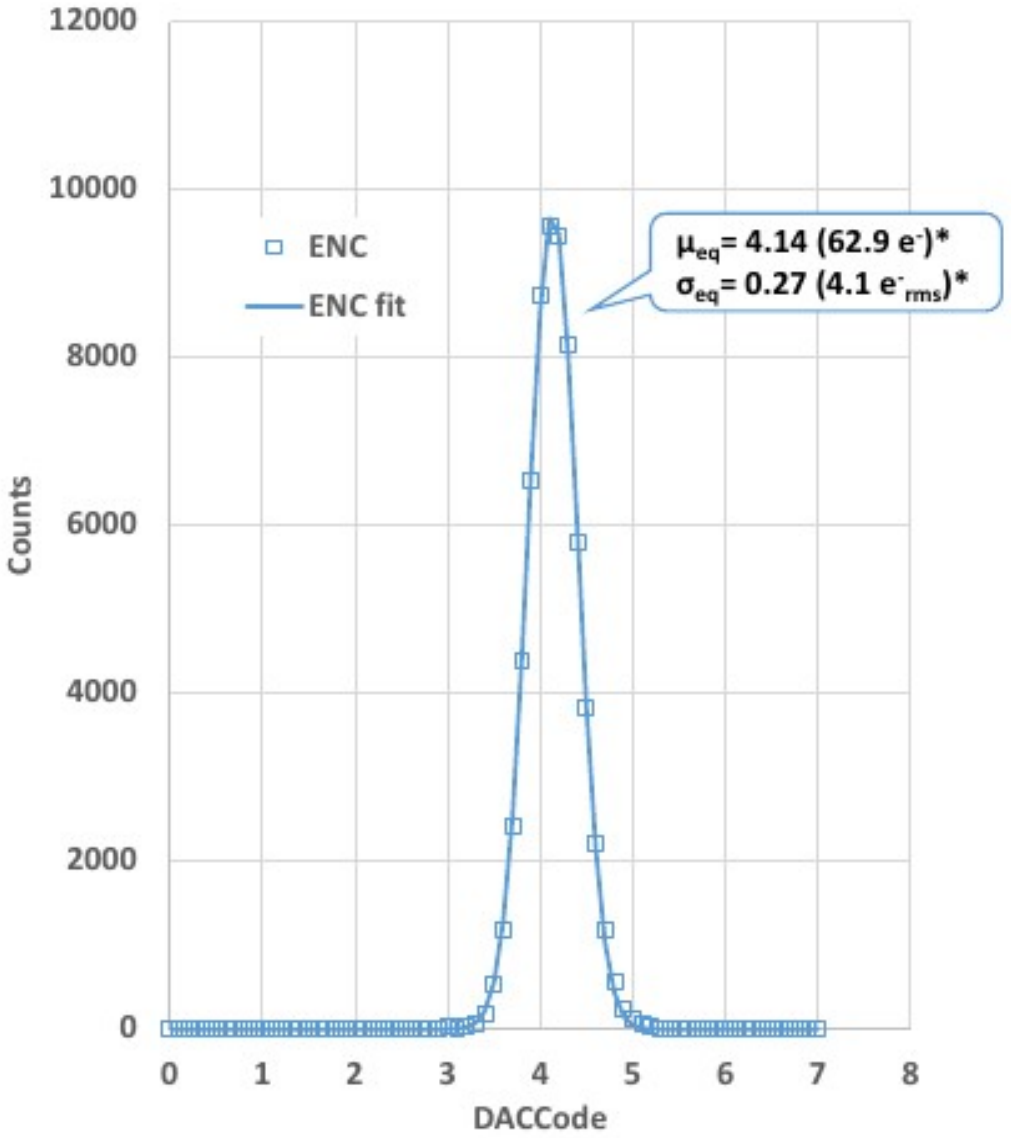


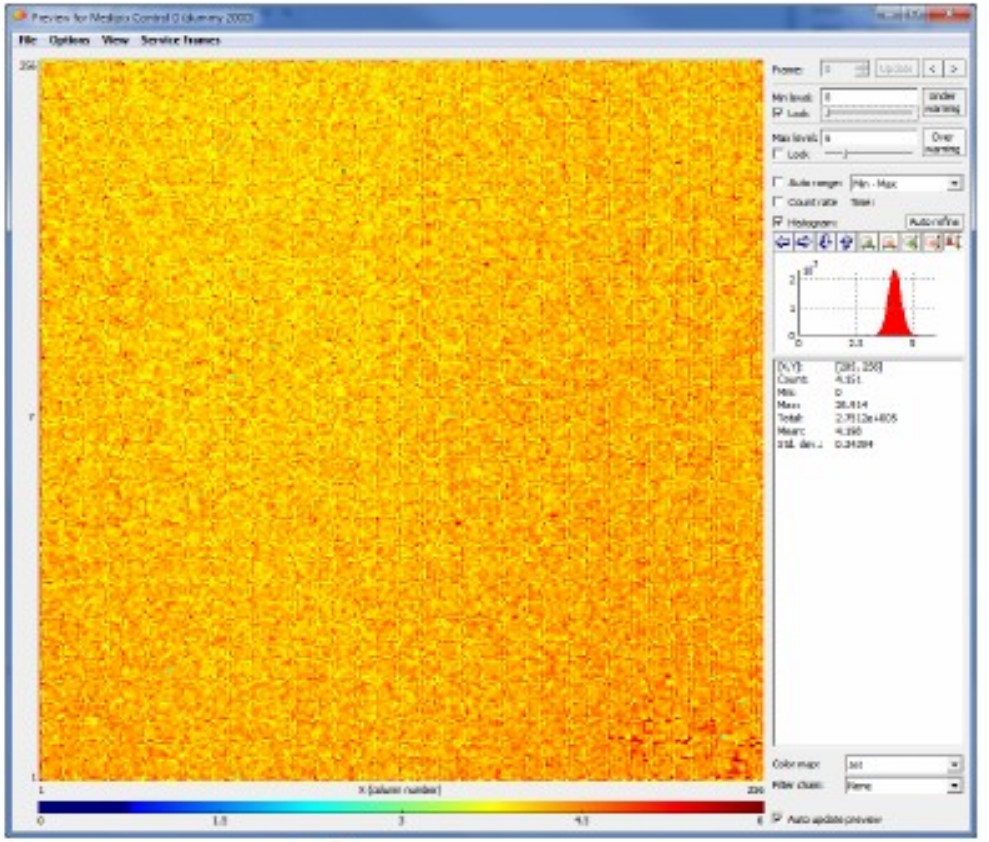
*Assuming Ctest=5fF

Test pulses in 32 pixels



Electronic noise (preliminary)

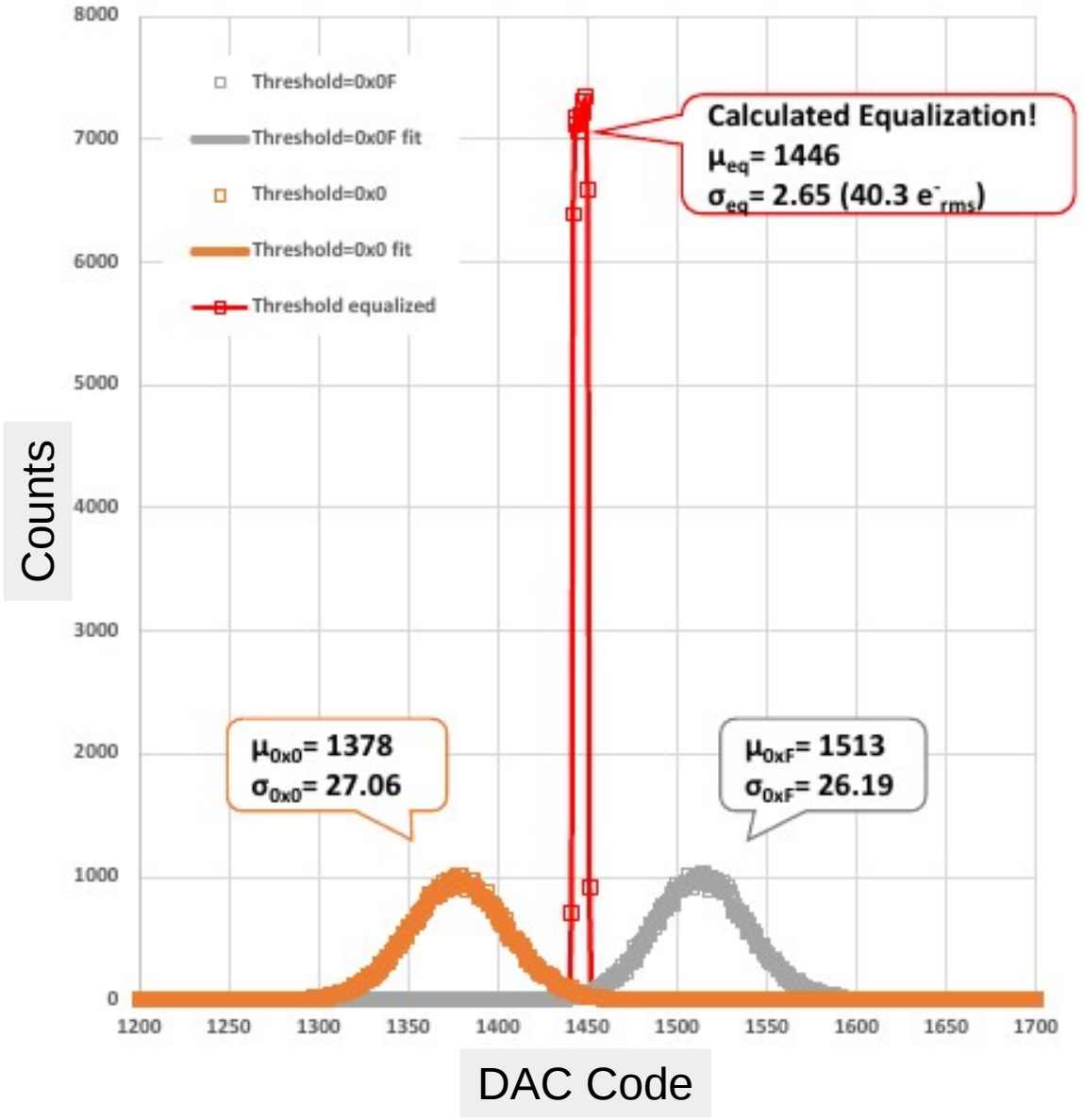


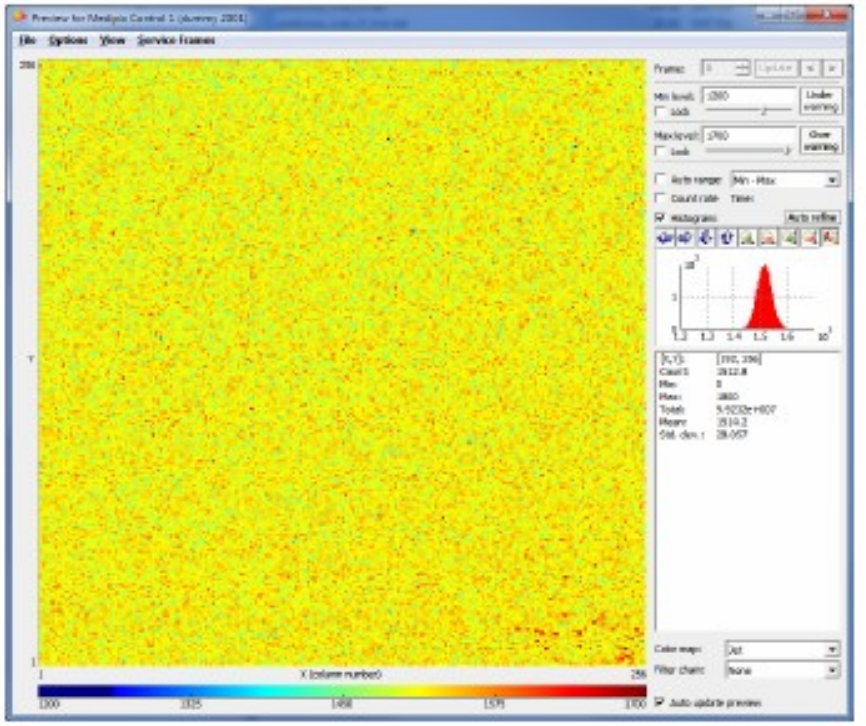


Measured ENC of all pixels
- Threshold scan over noise floor
- All pixels at code 0xF
- No systematics observed

*@gain of 25mV/Ke$^-$

Threshold equalization (preliminary)





Unequalised Threshold distribution:
- All pixels at code 0x0
- No systematics observed

*@gain of 25mV/Ke⁻

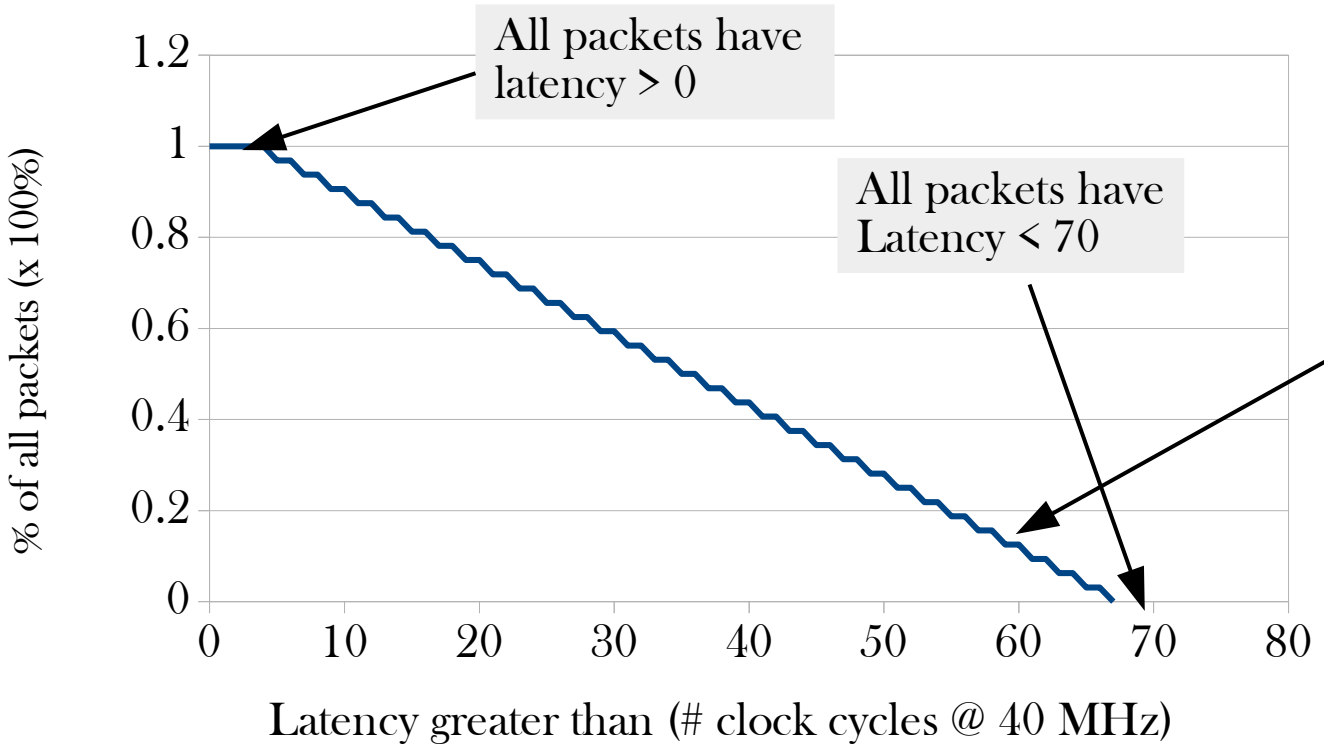
Summary of pixel measurements

Digital pixel front-end fully functional.
Responds correctly in ToT and Photon counting modes.
All measurements without sensor.

Pixel gain	~24.6 mV/Ke$^-$
Pixel to pixel gain variation	~3.3%
Pixel ENC	62.9 e-
Pixel to pixel threshold mismatch	410 e-rms
Pixel to pixel threshold mismatch calibrated (Threq)	40.3 e-rms
Expected minimum threshold $= 6\sqrt{ENC^2 + Threq^2}$	> 450 e-

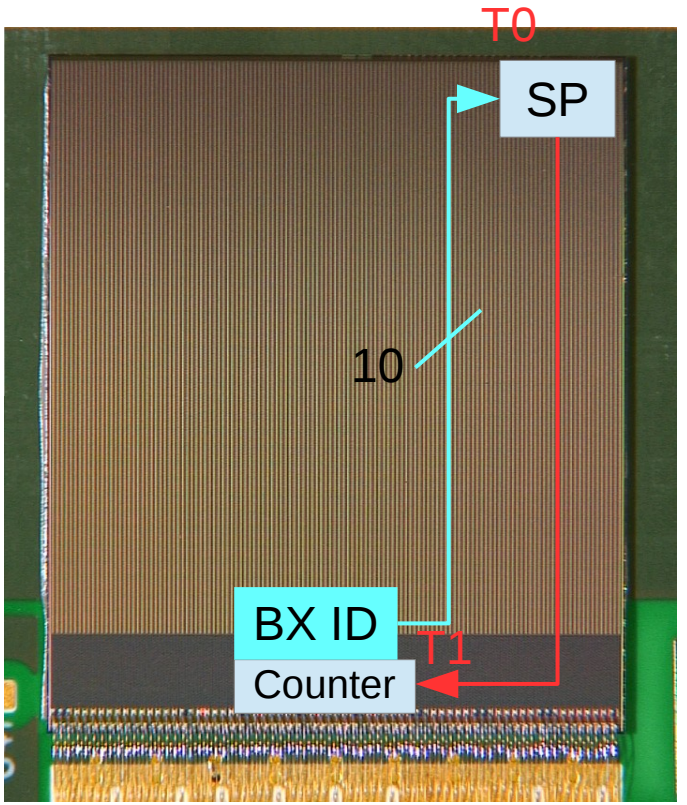
Threshold equalization only calculated not measured on chip
All measurements assuming Ctest=5fF

Super pixel packet latency (low rate)



Matches simulations. Indicates time stamping working as expected.

Latency: T1 - T0



Summary

- VeloPix ASIC, designed in 130nm CMOS, presented
- First silicon for debugging 7th September
- First results show the chip is alive and eyes open:
  - Power 1.2 W/ASIC, DACs working, pixels functional
  - Pixel: Gain ~25 mV/ke-, ENC 63 e-, no systematics
  - GWT serializer working, time stamping works
- Debugging and fine-tuning will continue in the following weeks:
  - Full DAQ chain tests, GWT BER and jitter
  - PLL characterization
- Production testing later this year at CERN

Thank you!

- List of contributors:
  - **ASIC designers:** Jan David Schipper, Vladimir Gromov, Sandeep Miryala, Xavi Llopart, Rafael Ballabriga, Winnie Wong, Tuomas Poikela
  - **Support, readout and testing:** Jerome Alozy, Martin van Beuzekom, Henk Boterenbrood, Bas van der Heijden, Jan Buytaert, Marco Daldoss, Edgar Lemos Cid,
  - **IP Blocks:** Stefano Michelis, Pedro Miguel Vicente Leitao, Rui De Oliveira

+ many others I forgot to mention…

Spares

Power routing and bump pads