ATLAS Phase-II-Upgrade Pixel Data Transmission Development

Marius Wensing on behalf of the ATLAS Collaboration
University of Wuppertal, Faculty of Mathematics und Natural Sciences
Contact: wensing@uni-wuppertal.de

Introduction

In the course of the HL-LHC upgrade (2024-2026) with expected luminosities of up to $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ ATLAS will perform the Phase-II upgrade. During this upgrade the complete Inner Detector of ATLAS will be replaced by the new **I**nner **Trac**k**e**r (ITk).

One possible layout for the ITk is shown in Figure 1. It consists of a pixel detector with five barrel layers and four end-cap rings and a silicon strip detector with four layers and six end-cap disks. This layout covers a volume up to 1 m radius around the interaction point and provides 9 space points up to $|\eta| \approx 4$. The active area of both detectors is built from about 200 m^2 silicon. The planned pixel size is $50 \times 50\,\mu\mathrm{m}^2$ in the pixel detector. The requirements on radiation hardness in this layout has also been simulated (see Figure 2). During the full operation time of the ITk detector the innermost layer has to withstand a total ionizing dose of about 50 MGy.

Also the ATLAS trigger system will be upgraded for Phase-II. Currently, there are two possible options how the trigger system for Phase-II will look like. The first option would be a two stage trigger system (L0 at 1 MHz/10 μs latency, L1 at 400 kHz/60 μs latency) with a hardware track trigger system. The hardware track trigger system would use data from the outer pixel layers and the strip detector as input for an L1 trigger decision. Another option is the full readout at an increased L0 rate (up to 4 MHz are under discussion) and a maximum latency of 25 μs. In this version the track triggering would be handled in software.

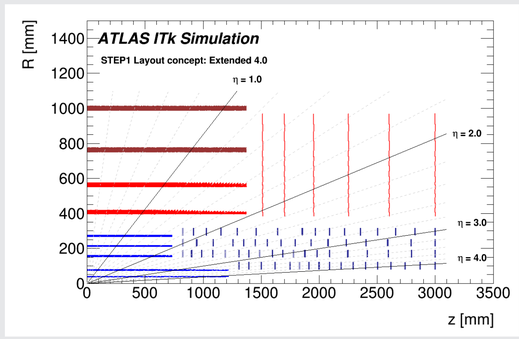

Figure 1: Possible ITk layout with 9 space points up to $|\eta| \approx 4$ consisting of a pixel detector (blue) and a silicon strip detector (red).

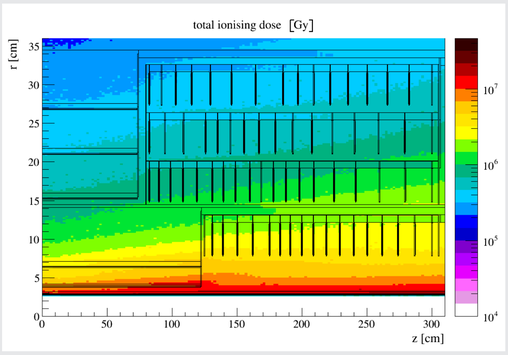

Figure 2: Simulation of the total ionizing dose in the ITk Pixel Detector volume after 3000 fb^{-1} of data taking.

Data transmission scheme

The data transmission scheme for the ITk foresees several stages of different cables and transmission technologies. The detector needs a bidirectional data link, where the downstream will carry the trigger and control signals (TTC) running at 160 Mbit/s. These signals are shared between a group of front-end chips. The upstream direction will carry the hit information from the detector at rate of about 5 Gbit/s. In the innermost layer of the detector each front-end chip will have a dedicated uplink towards the off-detector region. The data links of the outer layers will be shared between 2 or 4 front-end chips, as the bandwidth requirement per front-end chip decreases with distance to the interaction point.

A schematic view of this transmission scheme is shown in Figure 3. In total the cables will be about 90 m long. It is divided into three sections separated by patch panels (PP). On the stave flex cables, which are glued to the support structures, are used to transmit data signals and provide the supply voltage for the front-end chips. At the end of the stave (EoS, PP0) the flex cable is terminated. For reasons of the high radiation and to keep them accessible the opto-electrical converters cannot be placed in the detector volume but at the transition from the Inner Detector to the calorimeters (ID-endplate, PP1). The distance between the stave and the opto-electrical converters is about 5 to 7 m and will be bridged by copper cables. Finally, the connection to the off-detector readout hardware is done with about 80 m of optical fibres.

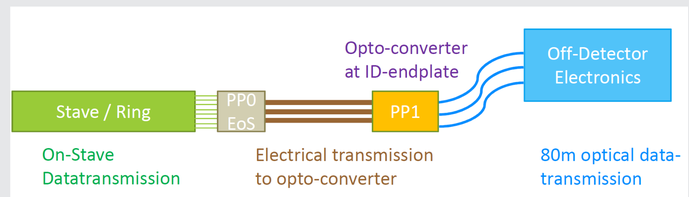

Figure 3: Data transmission scheme forseen to be used in the ITk Pixel Detector (drawing by T. Flick, University of Wuppertal).

Cables

Twisted Pair

The easiest solution to transfer differential signals is to use twisted pair cables. In these cables two conductors are twisted together, which reduces the impact of electromagnetic interference by canceling common-mode interferences. Figure 4 shows the profile of such a twisted pair wire evaluated for the ITk Pixel detector. The conductor in this cable has a diameter of 0.127 mm (36 AWG) and is shielded with 10 μm aluminum foil. In total it has a radiation length of $\mathcal{X}/\mathcal{X}_0 = 0.027\,\%$. During tests of a 1.15 m prototype a data rate of 6.2 Gbit/s has been reached.

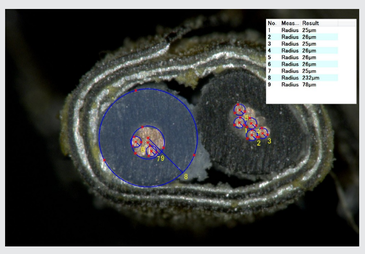

Figure 4: Photography of a cut through a 0.127 mm (36 AWG) twisted-pair cable shielded with 10 μm aluminum foil (picture by V. Fadeyev, University of California Santa Cruz).

Also the use of equalization techniques is under evaluation for the twisted pair cables. Figure 5 shows the eye diagram of a 2.5 m twisted pair cable prototype before and after equalization.

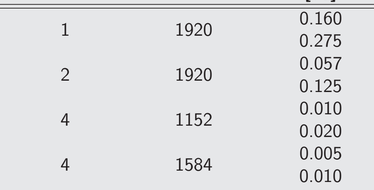

Figure 5: Simulation of the effect on the data transmission through a 2.5 m twisted pair prototype. (L. Flores, University of Glasgow).

TwinAx

The TwinAx cable is an enhancement of the twisted pair cable as it is a dual coaxial cable with a common shield. Therefore, it has much better transmission properties at the cost of more material inside the detector volume. For a 30 AWG Cu-clad Al TwinAx cable the radiation length is $\mathcal{X}/\mathcal{X}_0 = 0.076\,\%$ (smeared over the stave), which is a factor of 3 compared to the twisted pair cable. Figure 6 shows a photo and a labeled schematic of a TwinAx prototype.

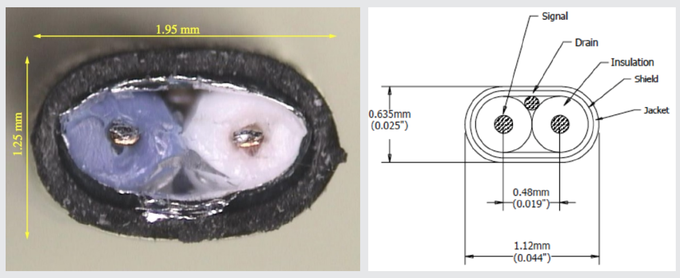

Figure 6: Photo and labeled schematic view of a cut through a TwinAx cable (M. Kocian, S. Dong, SLAC).

Different prototypes have been tested with a bit error rate tester to up to 10 Gbit/s over 6 m cable. Table 1 shows the results of the measurements. With these measurements it was proven that the TwinAx cables can be used for transmitting the data from the detector towards the opto-electrical converters. However, due to their large radiation length they must be combined with lightweight cables or flexes in the inner detector regions.

Table 1: Achieved data rates for different TwinAx versions and with different test patterns and signal optimizations (pre-emphasis and equalization).

AWG	length [m]	PRBS-31 [Gbit/s]			PRBS-7 [Gbit/s]		
		no opt.	pre-emph.	equalization	no opt.	pre-emph.	equalization
28	6	6.4	6.4	8	8	8	10
30	6	5	6.4	10	6.4	8	10
34	4	5	6.4	8	6.4	8	10

Flex cables

For the data transmission directly inside the ITk pixel volume flex cables will be used. These flex cables are directly glued to the mechanical support structures and carry the data signals as well as the module powering and the high voltage for the sensors. A sectional drawing through a flex is shown in Figure 7. The flex is constructed out of polyimide and designed to have a differential impedance 100 Ohms.

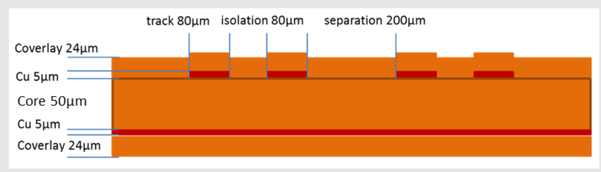

Figure 7: Sectional drawing through a stave flex cable (picture by N. Massol, LAPP)

Figure 8 shows a 1 m flex cable prototype. Also bit error rate measurements have been performed on flex cable prototypes, where a 1.2 m prototype has been rated up to 5 Gbit/s with a bit error rate of $5 \cdot 10^{-11}$.

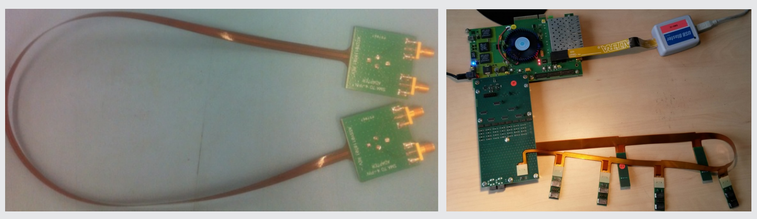

Figure 8: Prototype of a 1 m flex cable (left, picture by N. McFadden, University of New Mexico) and how the flex prototypes are being evaluated with a bit error rate measurement (right, picture by A. Rummler, LAPP)

Simulations

The ITk front-end chip will be designed to provide a maximum data rate of 5 Gbit/s. With this data rate and the assumption of 1 MHz trigger rate each event can eat up to 5000 bits on the data link. Into these 5000 bits the hit information of all connected front-end chips has to fit. Therefore, it is important to know how many hits per front-end chip are expected and how these are distributed over the front-end chip (see Figure 9). The occcupancy plot shows two different regions in the detector. Near the interaction point (z=0) we have less hits than in the forward regions (z=max.). However, the forward region has larger clusters allowing a better compression due to cluster-based encoding. Table 2 shows the results of two possible encoding schemes (hit-based and cluster-based encoding).

Summarizing the results from the simulations it is required to have different encodings for the different regions in the detector. And especially in the inner layers of the detector an additional compression will be needed to get the data out of the detector. The development of an adequate transmission protocol is a challenging task for ITk-DAQ development and the front-end design.

Table 2: Estimation of the available bits per hit and per cluster for the different ITk barrel layers (B0-B4) and end-cap rings (E0-E3) at a link bandwidth of 5 Gbit/s and 1 MHz trigger rate.

Layer/Ring	radius [mm]	front-ends per data link	number of data links	hit occupancy [%]	hits per event	bits per hit	cluster size	number of clusters	bits per cluster
B0 (z=0)	39	1	1920	0.160	215	24	6	36	139
B0 (z=max.)				0.275	370	14	29	13	385
B1 (z=0)	75	2	1920	0.057	77	33	5	16	157
B1 (z=max.)				0.125	168	15	24	7	358
B2 (z=0)	155	4	1152	0.010	13	97	1	13	97
B2 (z=max.)				0.020	27	47	12	3	417
B3 (z=0)	213	4	1584	0.005	7	179	1	7	179
B3 (z=max.)				0.010	13	97	10	2	625
B4 (z=0)	271	4	2016	0.003	4	97	1	4	313
B4 (z=max.)				0.006	8	313	8	1	1250
E0	80	2	408	0.055	74	34	4	19	132
E1	150	4	432	0.023	31	41	4	8	157
E2	213	4	384	0.013	17	74	3	6	209
E3	275	4	480	0.007	9	139	3	3	417

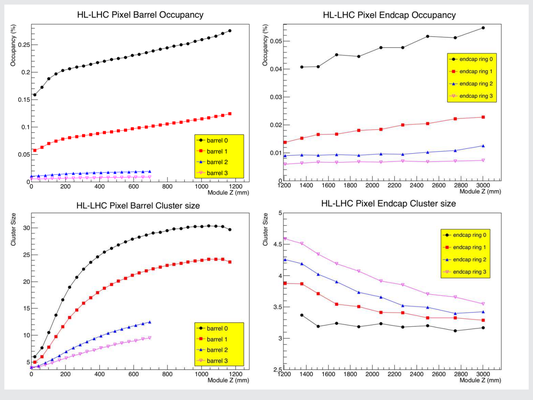

Figure 9: Simulation results for the hit occupancy and cluster size in the ITk barrel and end-cap region as a function of the distance to the interaction point along the beam-pipe. Simulations by S. Viel, M. Garcia-Sciveres (LBNL) and S. Banerjee (University of Louisville).

DAQ

The ITk Pixel Detector will have over 10000 data links each carrying a data rate of 5 Gbit/s. Due to the highly parallel structures in the readout system and the flexibility of easy reconfiguration FPGA-based solutions for the DAQ hardware are under evaluation. Currently, several laboratories are developing prototype readout systems to be used for testing the ITk prototype front-ends:

- YaRR: PCIe-based readout system (University of Wuppertal, LBNL)
- USBpix 3: USB 3.0-based readout system (University of Bonn)
- RCE 2: ATCA-based readout system (SLAC)
- FELIX: Commercial FPGA/40G-Ethernet-based readout system (ATLAS TDAQ group)

It is not yet decided how the final readout system will look like, but the developments from the DAQ prototyping will be used and scaled up to an ITk Pixel readout system.

Other topics

Other important topics not mentioned in this poster, but presented in other posters and talks during this conference:

- V. Wallangen, 65nm Receiver with Decision Feedback Equalization for Radiation Hard Data Link at 5Gbps, Poster
- L. Flores, High speed electrical transmission line design and characterisation
- D. Guo, Developments of two 4x10-Gbps radiation-tolerant VCSEL array drivers in 65 nm CMOS