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AIDA-CALICE DAQ interface

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AIDA-CALICE DAQ interface

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1 Introduction

1.1 Purpose

The purpose of this document is to provide a description of the DAQ interface between a master device and several low-duty-cycle detectors. This master device provides the synchronisation between the detectors. The document concentrates on the hardware interface. For the software interface an interface to a EUDAQ run control and the corresponding finite state machine and an interface to an event builder as well as an interface to a data quality monitoring framework like DQM4HEP is assumed. Only the protocol for the interface is described, the implementation of the master device in hardware can be based on several existing or planned devices like the CCC developed for CALICE, the GDCC developed for the CALICE SiECAL or the AIDA-2020 (mini-)TLU. In the following, the term “master CCC” will be used for this central master device.

For the phase when the detectors are open to record events the term “data acquisition” will be used, while it is assumed that during “readout" no further events can be recorded.

1.2 Example setup

The structure of the setup of a system for data acquisition and synchronisation of several low-duty-cycle detectors is discussed using the common running of three CALICE calorimeter prototypes in a testbeam as an example. A simplified block diagram of the setup is shown in Fig. 1.

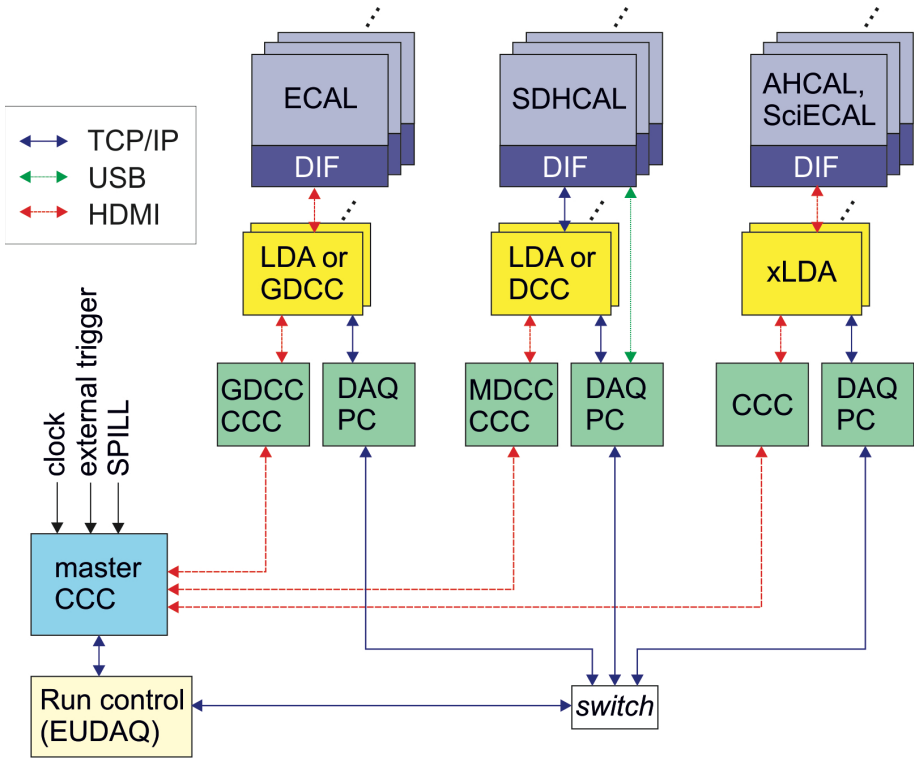

Fig. 1: testbeam setup of three CALICE prototypes

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Since the three CALICE detectors silicon ECAL, SDHCAL and AHCAL (the Scintillator ECAL is identical to the AHCAL in terms of DAQ interface) have stand-alone DAQ systems, a modular structure with a light-weight top-level DAQ is assumed, with minimal changes to the existing DAQs. However, if a device can perform the tasks of two separate devices (e.g. the master CCC and one of the detector CCCs), then a single device can be used. All CALICE detectors use a similar internal DAQ structure with: a central device providing the timing information for all detector layers (generically called “CCC" in the following); a device to fan out this information and to aggregate the data from several detector layers (LDA, GDCC, DCC or xLDA); detector interfaces (DIFs, typically one per layer) to communicate with the readout chips (ROCs); and a DAQ PC responsible for the configuration of the detector and for receiving and passing on the data to the central data storage. For the interface to the common DAQ mainly the CCC and the DAQ PC are relevant.

2 Task of the master CCC

The synchronisation of all detectors is ensured by providing all signals determining the detector timing from the master CCC to the detectors:

- the master CCC provides the following signals to the detectors: the clock, the “START" command of the data acquisition, the "STOP" command of the data acquisition and the external trigger signal. For testbeams, the clock frequency can be either 50 MHz (ECAL and SDHCAL) or 40 MHz (AHCAL and SciECAL), and the master CCC must be able to provide both frequencies at the same time, with the synchronous commands (START, STOP, trigger) aligned with both clocks.
- So called “BUSY” signals must be provided from the detectors to indicate that the respective detector is not ready (e.g. during readout).
- These BUSY signals of the detectors are collected from the master CCC.
- The master CCC uses the BUSY signals provided by the detectors to "START" and "STOP" the data acquisition: the data acquisition is stopped immediately after receiving BUSY from any of the subsystems, and the master CCC waits until the BUSY from all subsystems is cleared before starting the next data acquisition.
- When the master CCC sends the signal to STOP the data acquisition, the detectors must stop their data taking and read out their data.
- The master CCC also handles the external SPILL signal provided by testbeam facilities to indicate the presence of beam. The next start of the data acquisition is vetoed until the external SPILL signal indicates beam.

The master CCC can optionally receive an external clock, like a bunch clock provided by an accelerator.

All communication between the master CCC and the individual detector CCCs is based on HDMI cables with a custom protocol (see fig. 2 and table 1). The master CCC provides a clock to each detector on pair 1 of the HDMI lines. The master CCC communicates the START and STOP of the data acquisition by a level signal similar to a SPILL signal on pair 2 of the HDMI lines: raising the signal starts the data acquisition, lowering the signal stops it. In future, sending start_acquisition and stop_acquisition commands as fast commands according to the CALICE standard [1] on pair 2 is an alternative. The signal from an external trigger is provided by the master CCC on pair 3. The detectors provide their busy signals on pair 4. Pair 5 is a spare for communication from the detectors to the master CCC.

HDMI line pair	**signal**
1	clock
2	level signal indicating START and STOP of data acquisition, alternative: fast commands
3	trigger
4	BUSY
5	spare

Table 1: communication between the master CCC and the individual detector CCCs.

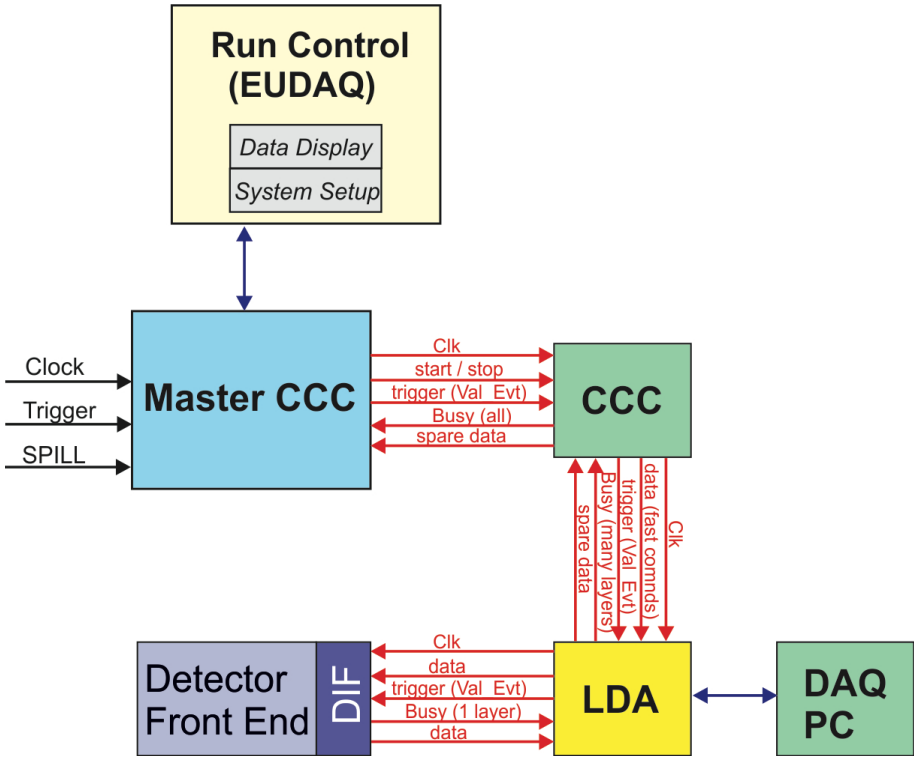

Figure 2: sketch of the communication between the master CCC and the individual detector CCCs.

3 Task of the run control

The run control ensures the synchronisation of the run start and run stop of all detectors. It also sends this information to the master CCC such that the master CCC can start and stop the data acquisition cycles. The run control provides a common run number for all detectors. In addition, the run control provides signals to start the initialisation and configuration of the detectors according to the interface described in the Implementation of a Finite State Machine for the EUDAQ framework [2].

As the CALICE detectors are operated in self-triggered mode, the data of all detectors must be stored in a way that a global time stamp can be derived that allows event building. The data storage can be handled by the PC running the run control, but can also be handled by several PCs.

4 Testbeam timings

The timing of a combined CALICE testbeam is shown in Fig. 3. It is discussed in more detail here including the communication inside of the individual detector electronics to explain the various conditions that may occur during the combined running.

The following events have to be taken into account:

1) The master CCC module starts a data acquisition cycle only when there is a valid external SPILL signal indicating the presence of beam. This signal is passed on by the detector CCC and the LDA to the DIFs which derive a corresponding signal for the detector ROCs.
2) As soon as one ROC is full, it issues a “memory full” signal to the DIF, and the DIF raises the BUSY to the detector CCC. The detector CCC passes the BUSY on to the master CCC. The readout procedure follows automatically after setting the BUSY for the master CCC.
3) The master CCC sends a STOP of the data acquisition when one detector sends a BUSY to the master CCC, no matter if the external SPILL signal is still active. This ends the data acquisition for all detectors, and they read out their data.

4) During long spills, the data acquisition is restarted from the master CCC while the external SPILL signal is still active.
5) The data acquisition is stopped from the DIFs after a defined time in order to prevent a discharge of the memory cells within the ROCs. Upon such a timeout, the DIFs send the BUSY signal to the detector CCC which passes it on to the master CCC.
6) In order to lower the power dissipation, some or all of the detectors can run in power pulsing mode. The individual detector has to ensure that the duty cycle does not exceed the value acceptable for this detector by sending a BUSY signal to the master CCC to inhibit the next data acquisition until the duty cycle is low enough.
7) The end of the external SPILL ends the current data acquisition (STOP command from master CCC). Afterwards, all detectors have to be read out.

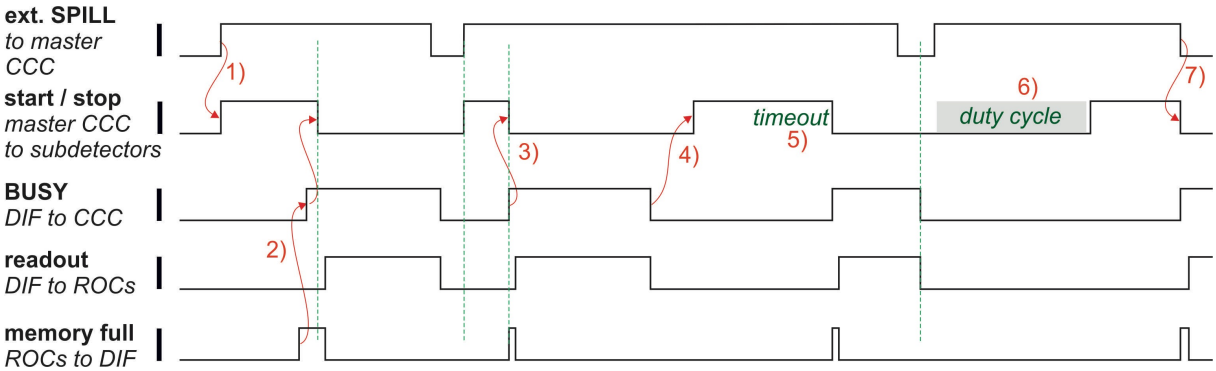

Fig. 3: General timing scheme for a combined CALICE testbeam.

4.3 Startup timing

Each detector may need a different time after receiving a START signal to be ready for recording events. In power pulsing mode, the START signal switches on the power supplies for the ROCs. Afterwards, a latency has to be applied in order to allow the supply voltages to settle down before the the actual active period can start. The necessary latency may differ between detectors.

In order to ensure that all detectors are open to record events at the same time, all detectors must be able to add a delay of up to a few ms between the signal they receive to START the data acquisition and the time when they start the actual active period.

4.4 ILC-like timing

In addition to the mode described above where each data acquisition cycle can take a different amount of time, a running mode with a fixed duty cycle (similar to the ILC bunch train structure) should be possible. For this, the master CCC should be able to provide a (configurable) fixed time structure of the START and STOP data acquisition signals, consisting of data acquisition windows of a few ms and long (100-200 ms) times for readout in between. It would be desirable to have two options in this mode: 1) a BUSY signal of one detector ends the data acquisition for all detectors, or 2) the BUSY signal is ignored and the data acquisition ends only at the end of the foreseen time window. In this case, the information which detector was BUSY for which time needs to be recorded. In both cases, the data acquisition is not restarted before the long readout time window is over.

5 Remarks

Since the readout and DAQ systems of the sub-detectors will likely be subject to changes in the next years, also the combination of the DAQ systems might require according adjustments. Future updates of this document are therefore possible. The future developments of the sub-systems as well as the impact on the common DAQ should be presented in the context of the corresponding AIDA-2020

work packages: WP 14 for calorimeters and WP 5 for DAQ. This document reflects the status as of July 2016.

Bibliography

[1] Marc Kelly, ”Calice LDA Docs” Version 1.2, Manchester 2008, available at http://www.hep.manchester.ac.uk/u/mpkelly/calice/lda/Calice_LDA_Overview.pdf

[2] Beryl Bell, "Implementation of a Finite State Machine for the EUDAQ framework"