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Instrumentation Buses for High Energy Physics, Past, Present and Future

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Over the past three decades high energy physics experiments have become progressively larger and more complex. Advances in electronic component technology played a massive role in this process, but the landmark development which enabled the ever growing quantities of detector data to be extracted was that of the instrumentation bus. This paper emphasises the fact that, while bus specifications continually improve, the essential qualities of the original concept have proved invaluable allowing inestimable economies of scale as well as the melding of devices from different institutional and commercial cultures into integrated structures.

I. INTRODUCTION

Detector read-out and data acquisition systems in particle physics experiments nowadays are based almost invariably on some kind of bus or dataway. The vast amount of data acquired and to be treated has made this unavoidable. Internationally recognized standards initially developed by the research community, such as CAMAC or FASTBUS, or those from industry, such as VME, have become commonplace in physics experiments. These standards specify a (backplane) bus with attendant connector and contact assignments, signal and timing standards, module access and data transfer protocols, as well as card sizes, crates, power supplies, etc., and, often, standard software routines.

The driving forces behind the introduction and standardisation of buses for use in high energy physics experiments have been multifold. There is firstly of course the evolution of electronics technology, of which the high energy physics community has traditionally been a front line explorer, then there is the increase in luminosity of the accelerators, leading to the need for finer granularity of the detectors and consequently to an increase in signal processing channels, and finally the fact that electronics originating from many different laboratories and companies must be able to coexist and function efficiently in the same experiment.

In this paper we will look back at the past of instrumentation buses and the lessons we learned from it, analyze the present, and conclude with a glance at the future.

II. THE PAST

The need for bused modular data acquisition systems began to be felt in high energy physics research from the beginning of the sixties when advances in component miniaturisation coupled with a growing sophistication in detector readout needs led to configurations of ever increasing numbers of counters or "scalers". These counters received pulses from coincidence circuits and ADCs. The ADCs measured the amplitude of detector-pulses or time-to-amplitude converted (TAC) signals. The greater part of the electronics in these experiments however was at the front end, in the form of amplifiers, discriminators, coincidence circuits, etc., to process signals from mainly scintillation counters. The first modular system standards designed to cover specifically this area were the NIM System[1], drawn up by the AEC Committee on Nuclear Instrument Modules (NIM) in the USA, and the ESONE System[2] by the Committee for European Standards on Nuclear Electronics (ESONE). Both specifications were first published in 1964.

Over the years the NIM System has found widespread application in all areas of nuclear research and many other domains, and is still alive and well today. It provides thoroughly specified mechanics, power supplies and backplane connectors, front panel signal levels and connectors, but no backplane bus. However, even with a standard as mature as NIM, innovation can still occur as has been proven by the recent adoption of the IEEE-GPIB[3] as the standard NIM Digital Bus[4].

The ESONE System never became popular, partly because by the mid-sixties the first minicomputers had arrived on the market and had been integrated "on-line" into the experiments, primarily to read-out the above-mentioned counters. With an increasing number of these devices to be read-out many laboratories and companies had developed and implemented bus systems of their own brand. This obviously led quickly to confusion and inefficiency, both in research laboratories and industry.

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In 1966 the ESONE Committee therefore decided to set up a working group to define a standard modular computer-controlled bus system, which was first published in 1969 as CAMAC[5]. Inspiration for the design of this system specification was found in many laboratories, but in particular at the AERE at Harwell, England, as a follow-up to the earlier "7000" system[6]. The initial CAMAC specification has been refined and upgraded in the course of the years in collaboration with the AEC-NIM committee. It has found very wide acceptance in nuclear research and other fields, in particular in industrial controls. A wide range of modules is still available from industry in this standard.

The CAMAC specification is based on the technology of the end of the sixties, i.e. discrete transistors and the first TTL circuits. As a host, a single digital controller or minicomputer was foreseen. After an initial period of stability a variety of upgrades became unavoidable, driven by ambitions of the experimenters and advances in technology. To emphasize the evolutionary forces a number of these upgrades were rapidly commercialized, such as the concepts of multiple controllers in CAMAC crates[7], multiple hosts for up to fifty crates[8], extended address modes[9], etc.

The inefficiency of CAMAC to read-out sparsely distributed data was judged unacceptable at CERN and elsewhere when track detectors such as multiwire proportional chambers (MWPC) and driftchambers started to be used in experiments. A new style of CAMAC crate (ROCC) and branch (ROBD) controller[10] was introduced at CERN, which greatly enhanced the system read-out speed by skipping in its scan those channels, modules and crates without valid data. This improvement was found insufficient when after ≈ 1975 the number of wires or sensors in these detectors increased further, and the bandwidth of CAMAC became the limitation. A number of CAMAC derivatives were designed and implemented on a large scale. These provided much higher bandwidth by using an ECL backplane and a simplified protocol while retaining CAMAC mechanics[11].

The advent of the microprocessor offered the opportunity to introduce multiple masters or processors into systems and a number of in-house solutions started to appear in laboratories. Consequently, in 1976 it was judged that the time was ripe to review the situation and to define a new standard. This new standard should retain the best characteristics of CAMAC, completed by useful aspects of the derivatives, and be based on leading edge technology.

Work on a new standard had started independently on both sides of the Atlantic, by working groups of the ERDA-NIM Committee, and of the ESONE Committee. After a while these working groups joined forces and ideas, which resulted in the publication in 1983 of the first FASTBUS specification[12] in the USA and in Europe, which evolved into the definitive specification in 1986[13].

At the time when CAMAC was specified (1969) no other bus standard was in existence, nor were there any microprocessors. During the seventies a variety of 8 bit microprocessors became available, but none of them came with a bus system which was of real interest to nuclear electronics. When 16 bit processors came to the market they were immediately accepted by designers of FASTBUS systems. In particular, the Moto-

rola 68000 processor family proved extremely popular. The suitability of this processor family for bus-oriented developments was further illustrated by the publication and commercialisation of the VME Standard[14], tailored specifically to this series of devices. VME is not generally considered very suitable for front end electronics, but has found application in trigger and other processors in experiments.

III. THE PRESENT

The instrumentation standards which we find in particle physics experiments today are CAMAC, FASTBUS, NIM and VME. CAMAC continues to be used wherever adequate, because of available equipment and expertise in this standard. New developments in CAMAC are rare, and aim in general at complementing existing CAMAC systems. However it should be mentioned that manufacturers still sell an appreciable volume of CAMAC modules.

FASTBUS is found in most of the major experiments throughout the world, at BNL, CERN, FNAL, KEK, Los Alamos, SLAC, TRIUMF, etc. It was designed with the needs of these experiments in mind and it has proven to meet them well in practice. The system has been completely specified and engineered, including such mundane items as crate, power supplies and cooling. Software is not forgotten and is offered as a coherent set of Standard Routines[15]. The system is being used for the full range of applications in the physics world. It is particularly suitable for front-end electronics because of its large board size, but also for processors, memories, trigger systems, etc. The strong points of FASTBUS have turned out to be the large board size, the multicrate architecture, and intrinsically high speed.

Contrary to earlier doubts expressed by some potential users, FASTBUS, taking into account all overheads including bus interfacing, powering, cooling, footprint, etc., has proved to be quite a bargain with respect to CAMAC and VME. Manufacturers offer ADCs and TDCs in FASTBUS at an appreciably lower price per channel than in CAMAC and, furthermore, the price to power such a channel in a FASTBUS crate is more than three times less.

The VMEbus (VERSA module Europe) was conceived as a single crate bus for applications with the family of Motorola 68000 microprocessors. It is the Eurocard compatible variant of the original VERSAbus[16]. It has found application in particle physics experiments mainly for data acquisition and trigger systems. Its small board size gives no gain over CAMAC in front end electronics. The absence of a multicrate or system specification has also tempered its popularity, although a proposal for an intercrate connection (VICbus)[17] has now been submitted.

The cost of electronics has grown to approximately 30% of the budget of present day experiments. At least 90% of this money is spent on electronics at the front end, and the remaining 10% is invested in the data acquisition and trigger system. Therefore it is vitally important that experiments do obtain the optimum economic solution for the front end electronics while, of course, satisfying the essential technical requirements.

IV. THE FUTURE

The future of instrumentation buses in particle physics experiments will continue to be governed by the requirements of the experiments, defined in the light of available electronics technology. This technology has now advanced to a point where Application Specific Integrated Circuits (ASIC) have become feasible for the greater part of the detector signal processing chain, including time (TDC) and amplitude (ADC) digitizers as well as buffer memories. The small dimensions and the low power consumption of these ASICs make it possible to mount them directly on the detectors. This will cause a major change in the architecture of read-out and data acquisition systems as compared to the present, where in the majority of the cases only preamplifiers are mounted on the detectors. This technology has also made it feasible to plan detectors of very fine granularity and 10^6-10^7 sensor channels for experiments at the next generation of accelerators and colliders such as the Large Hadron Collider (LHC) in Europe and the Superconducting Super Collider (SSC) in the USA. These machines have a very high luminosity (10^{33}-10^{34} particles/cm²/sec⁻¹) and a close particle bunch spacing ($\approx$ 15 ns), giving 10^8-10^9 events sec⁻¹, where each detector channel produces at least 1 byte of raw data per event, resulting in 10^{14}-10^{16} bytes sec⁻¹ for the complete detector. Finally only 10-100 events sec⁻¹ of 1 Mbyte will be retained after multilevel triggering and filtering. To handle this high signal and event rate a wide bandwidth is needed for both the signal processing, the read-out and the data acquisition system. The cost of the electronics for these experiments is estimated at 50% of the total budget.

Where will the place of instrumentation buses be in this new scenario? It seems very unlikely that a classical bus will be required for the part which is mounted on the detector, i.e. for the front end. There may be a role for the FASTBUS cable segment or the Scalable Coherent Interconnect (SCI)[18] in the lower-level trigger system, which is generally assumed to be installed on the detector. The SCI is a newcomer in this field. It is a very high speed point-to-point link which should allow data transfers of at least 1 Gbyte sec⁻¹. Prototype systems are in evaluation.

The connection between the electronics on the detector and the data processing part off the detector will require high speed links. The FASTBUS cable segment and the SCI are candidates for this function based on either twisted pair copper cables or optical fibres.

The data processing part off the detector must be capable of handling an input data rate of approximately 100 Gbytes sec⁻¹, to select finally the few events of interest. The system to house this activity must offer the possibility of parallel processing in addition to a wide bandwidth. Candidates here are FASTBUS, Futurebus⁺, and SCI or a combination of these. Futurebus⁺ is another new standard[19]. It is a non proprietary

bus. Its specification has taken a long time to reach a conclusion, but has benefitted from the experience gained with VME, Multibus II and FASTBUS. Datawords can be chosen as wide as 256 bits, thus making it possible to target at a bandwidth of 3,2 Gbyte sec⁻¹. Commercial products are expected in approximately two years.

There seems to be no major role for CAMAC, NIM and VME in the plans for future experiments at LHC and SSC, however these standards will continue to be invaluable in the more classical fields of experimentation.

V. REFERENCES

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