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# MAPS development for the ALICE ITS upgrade

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ABSTRACT: Monolithic Active Pixel Sensors (MAPS) offer the possibility to build pixel detectors and tracking layers with high spatial resolution and low material budget in commercial CMOS processes. Significant progress has been made in the field of MAPS in recent years, and they are now considered for the upgrades of the LHC experiments. This contribution will focus on MAPS detectors developed for the ALICE Inner Tracking System (ITS) upgrade and manufactured in the TowerJazz 180 nm CMOS imaging sensor process on wafers with a high resistivity epitaxial layer. Several sensor chip prototypes have been developed and produced to optimise both charge collection and readout circuitry. The chips have been characterised using electrical measurements, radioactive sources and particle beams. The tests indicate that the sensors satisfy the ALICE requirements and first prototypes with the final size of $1.5 \times 3\,\mathrm{cm}^2$ have been produced in the first half of 2014. This contribution summarises the characterisation measurements and presents first results from the full-scale chips.

KEYWORDS: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; Radiation-hard electronics

## Contents



## 1 Introduction: motivation and experiment specifications

The ALICE ITS upgrade is motivated by several new objectives, such as increasing the collision rates up to 50 kHz for Pb-Pb and 200 kHz for pp collisions, improving the impact parameter resolution by a factor 3 or even more below 1 GeV/c, and improving standalone tracking efficiency and $p_T$ resolution. For instance, the impact parameter resolution to be achieved at 400 MeV/c is 50 $\mu$m in both $r\phi$ and $z$ directions [1]. To satisfy these requirements, it is planned to replace the ITS with a new tracker consisting of 7 layers of MAPS, including 3 inner layers and 4 outer layers [1]. The first layer will be placed closer to the interaction point (22 mm compared to the present 39 mm) and the granularity will be increased reducing the pixel size from 50 $\mu$m $\times$ 425 $\mu$m to about 30 $\mu$m $\times$ 30 $\mu$m. Table 1 reports the pixel chip specifications. A power consumption well below 100 mW/cm$^2$ would allow for a substantial reduction of the detector material budget.

During the last decade, MAPS which integrate the sensor and the readout chip in one silicon wafer, have been explored for particle physics experiments with promising results [2, 3]. MAPS provide a low production cost and allow a significant improvement of spatial resolution and signal-over-noise ratio (S/N) for a given power consumption. Traditional sensors collect signal charge by drift, achieving a tolerance to non-ionizing radiation in excess of $10^{15}$ 1 MeV $n_{eq}$/cm$^2$. In MAPS signal charge is often collected primarily by diffusion, and therefore may be trapped more easily, resulting in a lower tolerance to displacement damage. For ALICE MAPS are a viable solution as radiation requirements are modest (table 1). The TowerJazz 180 nm CMOS imaging sensor technology has been selected for the sensor chip fabrication. The gate oxide thickness of 3 nm gives robustness to Total Ionizing Dose (TID). This technology offers a deep pwell, as shown in figure 1. The collection diode is the nwell-epitaxial layer (epi-layer) junction. The deep pwell shields the other nwells different from the collection electrode from the epi-layer, preventing them from collecting signal charge, which then would be lost for readout. This allows implementing PMOS transistors and hence full CMOS in the in-pixel circuit. High resistivity epi-layers ($> 1$ k$\Omega$ cm) with different thicknesses (18 $\mu$m–40 $\mu$m) are available. The results obtained from the small scale prototypes after TID and Non Ionizing Energy Loss (NIEL) irradiation indicate sufficient radiation tolerance for the expected levels in the ALICE ITS upgrade [4].

**Table 1**. Design specifications of PIXEL Chip [1].

| *Parameter* | *Inner layer* | *Outer layer* |
|---|---|---|
| Max. silicon thickness | 50 $\mu$m | |
| Intrinsic spatial resolution | 5 $\mu$m | 10 $\mu$m |
| Chip size | 15 mm $\times$ 30 mm ($r\phi \times z$) | |
| Max. dead area on chip | 2 mm ($r\phi$), 25 $\mu$m ($z$) | |
| Max. power density | 300 mW/cm$^2$ | 100 mW/cm$^2$ |
| Max. integration time | 30 $\mu$s | |
| Max. dead time | 10% at 50 kHz Pb-Pb | |
| Min. detection efficiency | 99% | |
| Max. fake rate | $10^{-5}$ | |
| TID radiation hardness[a] | 700 krad | 10 krad |
| NIEL radiation hardness[a] | $10^{13}$ 1 MeV $n_{eq}$/cm$^2$ | $3 \times 10^{10}$ 1 MeV $n_{eq}$/cm$^2$ |

[a] Include a safety factor of ten.

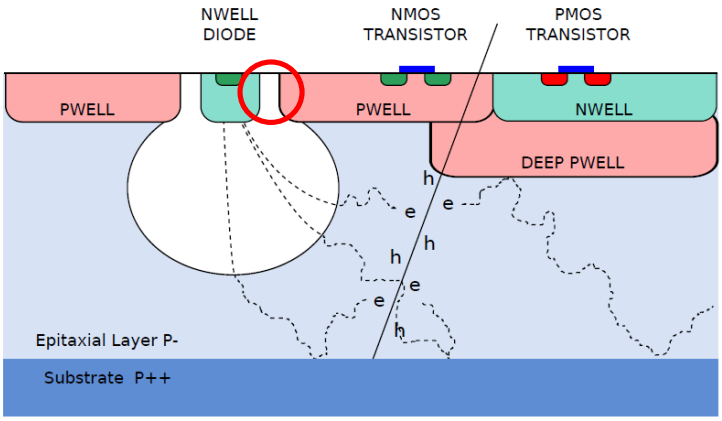
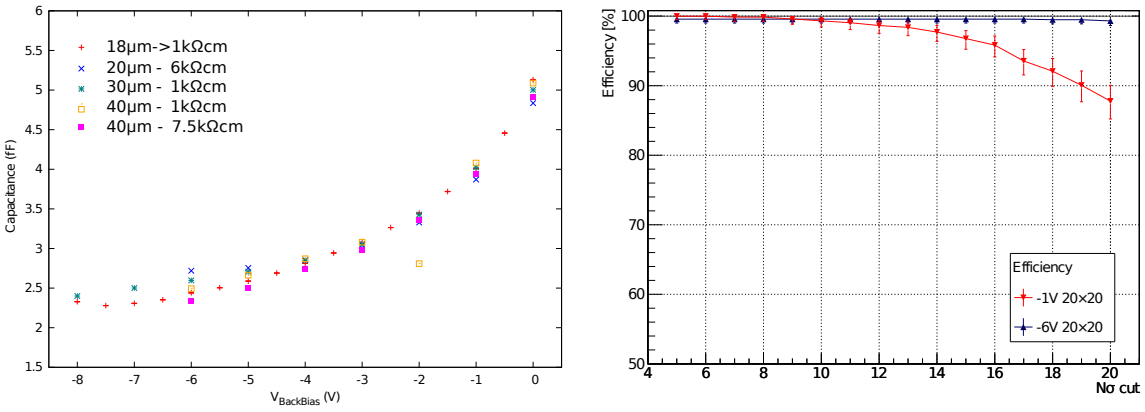



**Figure 1**. A deep pwell shields the nwell which contains the PMOS transistors, preventing it from collecting signal charge from the epitaxial layer instead of the nwell as charge collection electrode.

## 2 Chip development for the ALICE ITS upgrade

Three chip architectures are under development for the ALICE ITS upgrade. MISTRAL and ASTRAL are based on a rolling shutter readout structure. The difference between them is that MISTRAL uses an end-of-column discriminator, while ASTRAL uses an in-pixel discriminator [5]. In the ALPIDE (ALice PIxel DEtector) architecture, a low power binary front-end (40 nW) is combined with a data-driven readout, to reduce the power consumption below 50 mW/cm$^2$. The integration time is defined by the front-end shaping time and it is decoupled from the readout time. The ALPIDE architecture aims for an integration time of 4 $\mu$s to reduce the pile up probability and a small readout time to increase the detector readout capability. This paper will concentrate on the ALPIDE development.




(a) (b)

**Figure 2**. (a) shows the input capacitance as a function of the substrate bias for different resistivities and thicknesses of epitaxial layer. (b) shows the detection efficiency versus the input capacitance, tested at DESY with a 4 GeV/c electron beam.

### 2.1 Small scale prototypes

The Explorer [6, 7] test chip is used to optimise the sensor. The main sensor parameters are the starting material, the substrate reverse bias, and the collection electrode geometry (size of the diode and the spacing between the nwell and the surrounding pwell). The amplitude of the signal at the circuit input is equal to the ratio between the signal charge (Q) and the input node capacitance (C). Therefore, reducing the input capacitance will increase the front-end input signal, and allow for a lower analogue power consumption for a given signal over noise ratio and signal bandwidth [8]. Figure 2(a) illustrates that increasing the reverse substrate bias from 0 V to $-6$ V, the input capacitance decreases from $\sim 5$ fF to 2.5 fF, with minor difference between different starting materials for different variants of epi-layer resistivities and thicknesses. Test results confirm that the lateral spacing between nwell and pwell (as shown in red circle of figure 1 and figure 4) dominates capacitance. As expected the signal charge increases with increasing epi-layer thickness, but it was found to spread over too many pixels for thicknesses larger than 30 $\mu$m because the epi-layer is not fully depleted [9]. Figure 2(b) shows more margin in detecting efficiency can be obtained with reverse substrate bias illustrating that sensor optimisation including input capacitance has a direct system impact. A second small scale prototype pALPIDEss, with a pixel array of 512 rows by 64 columns and pixel pitch of 22 $\mu$m, was used to characterise the low power front-end and the hit-driven readout circuit [10, 11], and study the noise and threshold distributions.

### 2.2 Full scale prototype (pALPIDEfs) architecture

The first full scale prototype (pALPIDEfs) was designed with the objective to start the study of system level and integration aspects. The chip measures 15 mm $\times$ 30 mm and contains a pixel array of 512 rows by 1024 columns with a pitch of 28 $\mu$m. The in-pixel signal processing chain is shown in figure 3(a): the front-end is a high gain amplifier/comparator consuming about 40 nW [10]. The signal charge is collected by the collection electrode, the input node is reset by the diode

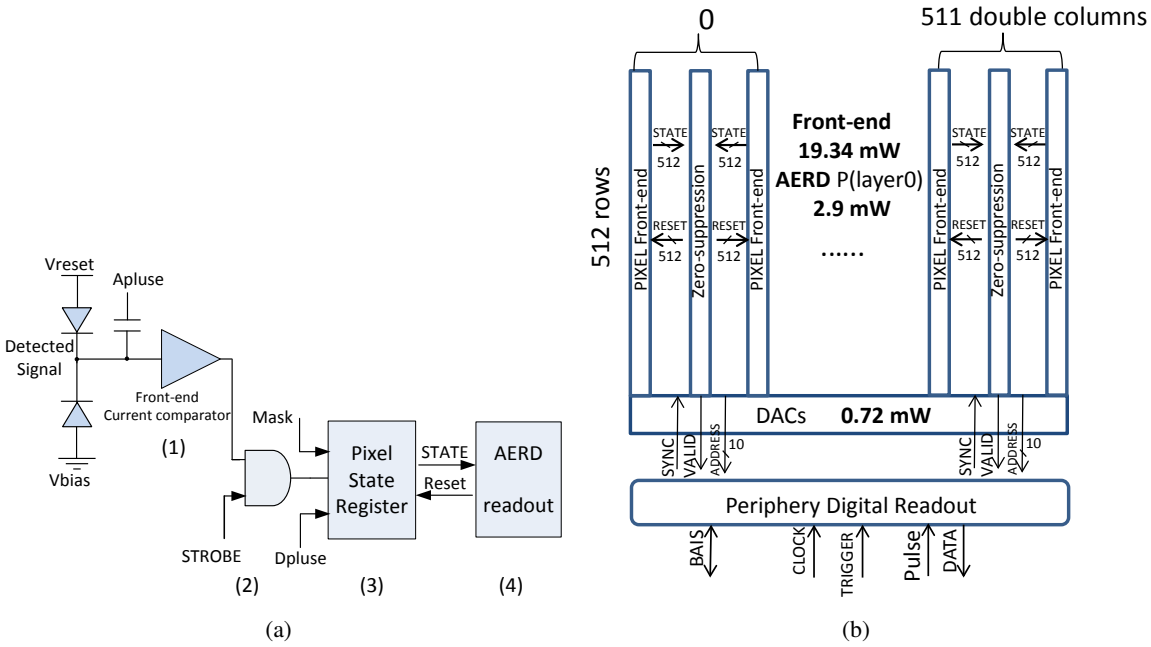
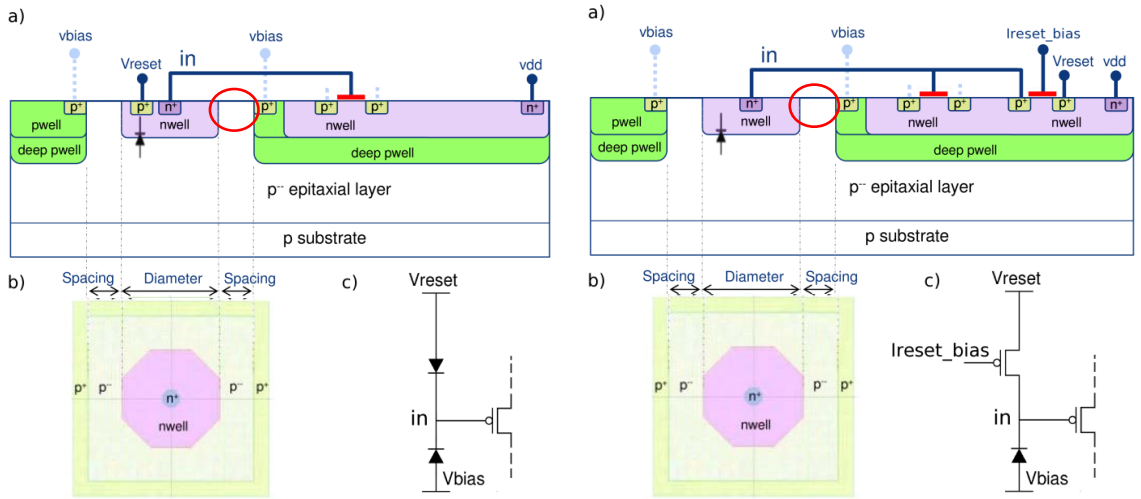



**Figure 3**. (a) In-pixel structure: (1) binary front-end; (2) readout enable logic gate; (3) in-pixel digital memory; (4) part of the readout structure. (b) pALPIDEfs matrix readout architecture.

connected to a static voltage bias Vreset, adjustable using an on-chip DAC. A negative voltage can be supplied to the substrate through Vbias to increase the depletion volume, allowing to reduce the input capacitance and to increase the drift collection component. The peaking time of the front-end ranges between 1 $\mu$s to 2 $\mu$s with a total pulse duration of 4 $\mu$s [10, 11]. The front-end peaking time is matched with the STROBE signal latency: in this way the front-end is used as an analogue memory and data is written into the pixel state register only when the STROBE is asserted. In the current prototype only one in-pixel state register is used, but a multi-event buffer inside the pixel is foreseen to reduce the dead time for next prototypes. Two configuration registers in each pixel are used to enable it for electrical pulsing (analogue Apulse and digital Dpulse), and to mask it if needed. The pixel state register is read out by the Address Encoder and Reset Decoder (AERD) circuit arranged per double column. The AERD circuit transfers only the relevant pixel addresses to the chip periphery. Every clock cycle the hit pixel with the highest priority is read out and then reset, so that the next one can be treated in the next clock cycle until all hit pixels have been read out. The readout time is therefore proportional to the number of hit pixels. The readout is controlled at the chip periphery with a signal synchronous with the clock (SYNC in figure 3(b)). In the current prototype the speed of the AERD is 10 MHz, and from the test results shown in section 3, the AERD circuit works as expected. The speed will be increased to 40 MHz in the next version. Figure 3(b) shows the pixel matrix readout circuit and the periphery circuitry. The pixel array is organised in double-column and contains the hit recording, the data storage and the zero-suppression readout processing circuit. Each double-column consists of 1024 analogue channels located along its two sides and connected to the AERD readout circuit in the middle. The whole matrix has been divided into four sectors, each of them contains 512 rows by 256 columns.




(a) Diode reset. (b) PMOS reset.

**Figure 4**. Sensor cross section, layout and schematic for diode reset and PMOS reset schemes.

Each sector has either a different sensor diode layout or a different reset mechanism. As one can see in detail in figure 4, each nwell collection electrode has the same width of 2 $\mu$m. The spacing between nwell and pwell is 1 $\mu$m for sector 0, 2 $\mu$m for sectors 1 and 2, and 4 $\mu$m for sector 3. The pixels in sector 2 are equipped with a diode reset, the others with a PMOS reset. The pixel array occupies around 93% of the chip area. DACs are implemented at the end of the column to provide voltage and current references to the pixels and to control the threshold of the front-end. An external biasing override is possible. In order to decrease the readout time, the whole matrix is divided into 32 regions to be read out in parallel. A digital readout circuit located below the DACs compresses the cluster information in the column and implements a loss-less data compression de-randomizing circuit. In this prototype, parallel CMOS I/O data transmission off chip instead of a high speed communication link is used. The power consumption of the pixel array is approximately 25 mW; the power consumption of the AERD readout is 3 mW assuming the maximum expected hit occupancy in the inner layers. The DACs consume 0.72 mW. Presently memories are clocked continuously even if they are not accessed all the time. Avoiding this and only clocking the memories when they need to be accessed, reduces memory power from 211 mW to only 0.7 mW and total digital periphery power from 313 mW to 102 mW. Therefore a power density of about 28 mW/cm$^2$ for the pixel matrix and digital periphery is achievable (with the exception of the power consumption of the high speed serial link, which will be included in future designs). Flex cables transmit power and data signals to the pixel chips, requiring bump bonding over the chip instead of wire bonding at the chip edges. Due to technology constraints the bond pads need to be designed with the top two metal layers. It has been verified that the presence of bond pads over the pixels does not significantly affect their performance.

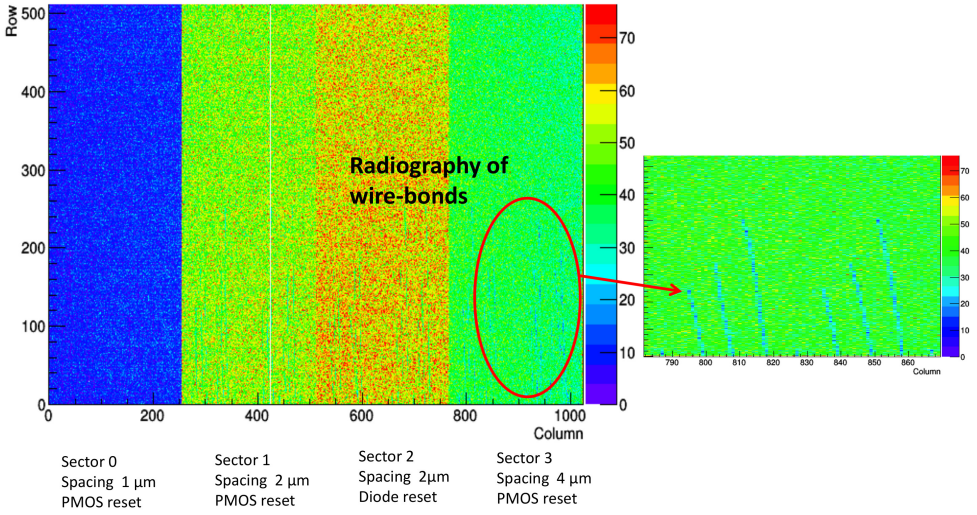
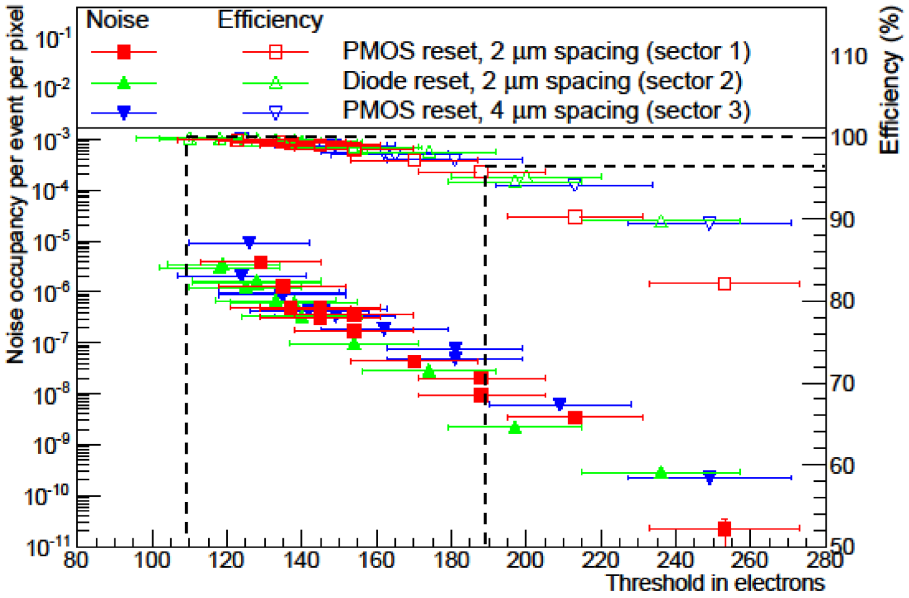


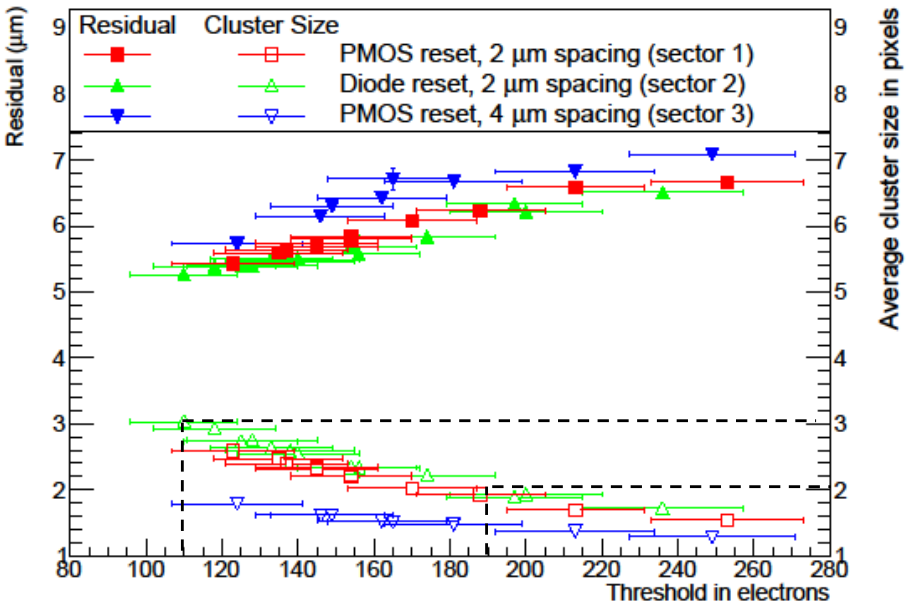

**Figure 5**. Hit map of the pALPIDEfs chip under $^{55}$Fe X-ray exposure.

## 3 Test results of pALPIDEfs

A pALPIDEfs chip with an epi-layer thickness of 18 $\mu$m and total silicon thickness of 50 $\mu$m has been tested. The hit map under $^{55}$Fe X-ray exposure is shown in figure 5. The band structure corresponds to the differences in the pixel design. Wire-bonds were used for the first tests and they are visible in the plot. A telescope of 6 or 7 planes of pALPIDEfs prototypes with a spacing of 18 mm was used for a beam test at CERN PS using a 6 GeV $\pi^-$ source which has an energy loss slightly larger than MIPs (Minimum Ionizing Particles). Wafers are delivered by the foundry at full wafer thickness (thick), some of these were thinned to 50 $\mu$m before dicing (thin), and a mixture of the two thicknesses was used in the telescope. The arrangement consists of 3 reference planes (thick, thin, thin), the DUT (Device Under Test, thin) and other two (thin, thick) or three (thin, thick, thick) reference planes. About 1–2 tracks were recorded per read out event. The tracks are fitted using a broken line fit [12]. The expected hit density in the experiment is about 36 hits/cm$^2$ for the innermost layer and 0.3 hits/cm$^2$ for the outermost layer of the detector [1]. Tests with different hit density levels are currently in progress. Figure 6 shows noise occupancy and detection efficiency, and cluster size and residuals versus input charge threshold. The fake hit rate is below $10^{-5}$ for a threshold value larger than 120 $e^-$ with masking 20 noisy pixels. The detection efficiency is above 99% for a threshold below 160 $e^-$ also without reverse substrate bias. The residual is $\sim 5.5\,\mu$m for thresholds below 120 $e^-$. From simulations we obtain a MCS (Multiple Coulomb Scattering) contribution of 3 $\mu$m, which leads to a spatial resolution less than 5 $\mu$m. The average cluster size is below 2 for threshold values larger than 160 $e^-$. Figure 6(b) illustrates that the cluster size decreases for increasing threshold settings and vice versa. The detection efficiency and the fake hit rate satisfy the sensor chip specifications (table 1). The good resolution of the telescope allowed a characterisation of the detection efficiency and the cluster size as a function of the position of the particle hit within a pixel. This was done in figure 7 and 8 for two different thresholds, 109 and 188 electrons, indicated by dashed lines in figure 6. Figure 7(a) illustrates that for the 109 $e^-$ threshold where the efficiency is 100%, the efficiency is independent from the particle hit position



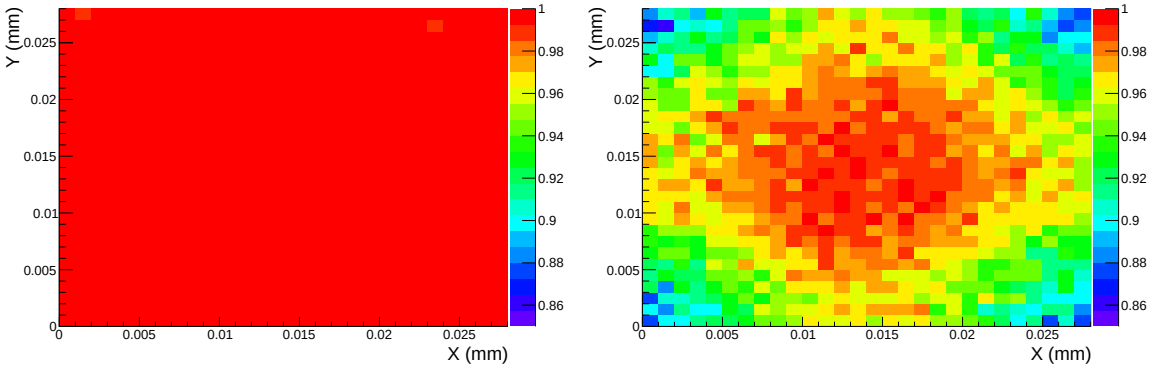

(a) Noise occupancy and detection efficiency.




(b) Residual and average cluster size.

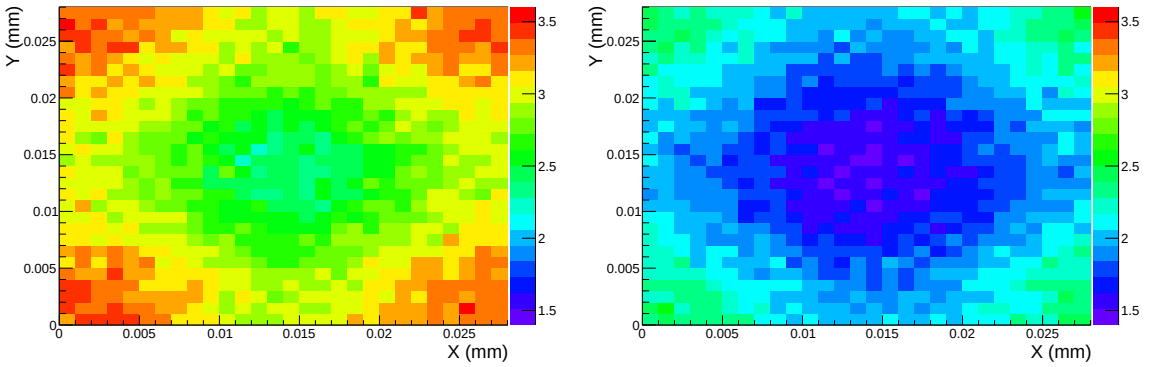
**Figure 6**. Noise occupancy, detection efficiency, residual and average cluster size of sectors of 1 to 3, beam test results by using a 6 GeV $\pi^-$ source.

within the pixel. Figure 7(b) shows that for the 188 $e^-$ threshold, where the efficiency starts to degrade, this is more pronounced at the corners of the pixels where charge sharing between pixels is more predominant. Figure 8 shows for the two example thresholds that as expected cluster size is smaller if the pixel is hit at or near the center, and larger for hits near the pixel corners, where the probability for charge sharing is larger.




(a) Test with threshold of $109 \pm 15\,e^-$. (b) Test with threshold of $188 \pm 17\,e^-$.

**Figure 7**. Detection Efficiency as a function of the hit position within the pixel of sector 1, beam test results by using a 6 GeV $\pi^-$ source.




(a) Test with threshold of $109 \pm 15\,e^-$. (b) Test with threshold of $188 \pm 17\,e^-$.

**Figure 8**. Cluster Size as a function of the hit position within the pixel of sector 1, beam test results by using a 6 GeV $\pi^-$ source.

## 4 Conclusions and outlook

The ALICE ITS upgrade has adopted MAPS for its implementation. The ALPIDE development aims to reduce the power consumption and the integration time by an order of magnitude below the specifications, using a low power binary front-end (40 nW) and a data-driven readout. We expect to reach a power consumption of $\sim$ 100 mW/chip or 20–30 mW/cm$^2$ in the final chip. Test results before irradiation of a first large scale prototype (pALPIDEfs) are very promising. The beam test illustrates very good position resolution and detection efficiency. Reverse substrate bias provides more operation margin. Further optimisation is foreseen on the collection electrode to reduce the analogue power and achieve a lower charge detection threshold, and on the pixel array readout circuit (AERD) to increase the readout speed. More functionalities will be included on-chip such as a serializer and LVDS driver for high speed data transmission.

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