Timing distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

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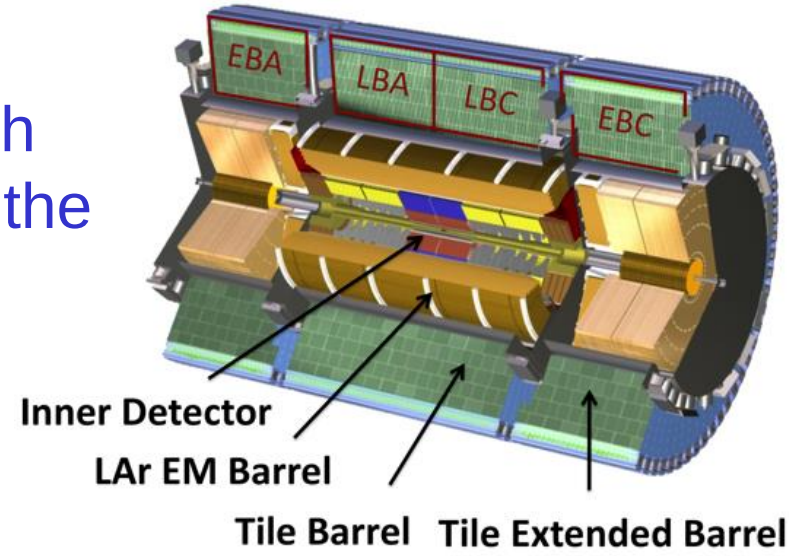
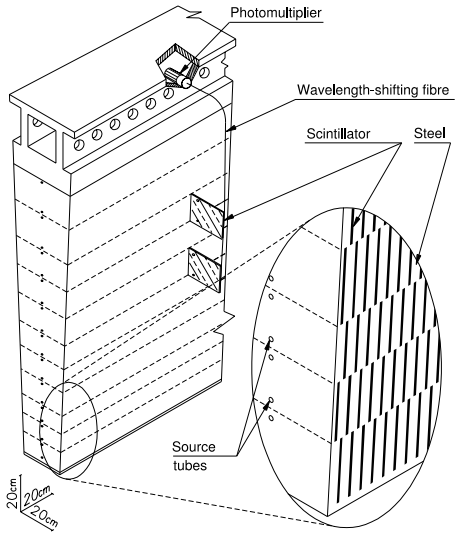
Tile Calorimeter

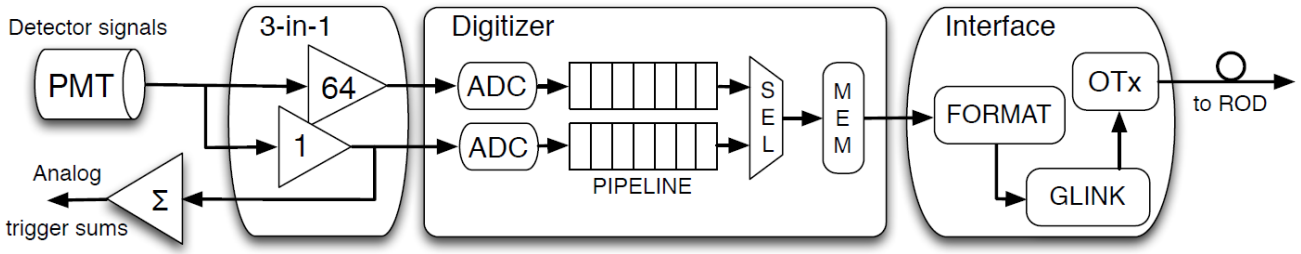
- Segmented calorimeter of steel plates and plastic scintillator which covers the most central region of the ATLAS experiment
  - 4 partitions: EBA, LBA, LBC, EBC
  - Each partition has 64 modules
    - One drawer hosts up to 48 Photo Multiplier Tubes (PMTs)
  - Light produced by a charged particle passing through a plastic scintillating tile is transmitted to the PMTs
  - Signals coming from PMTs are digitized and stored in the front-end electronics upon the reception of a Level-1 accept
  - Around 10,000 readout channels



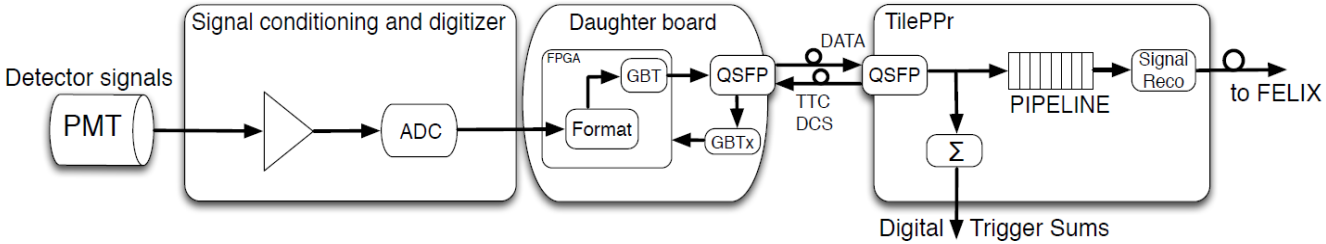


Tile Calorimeter Phase II

Present front-end electronics



Equivalent electronics for phase-II upgrade

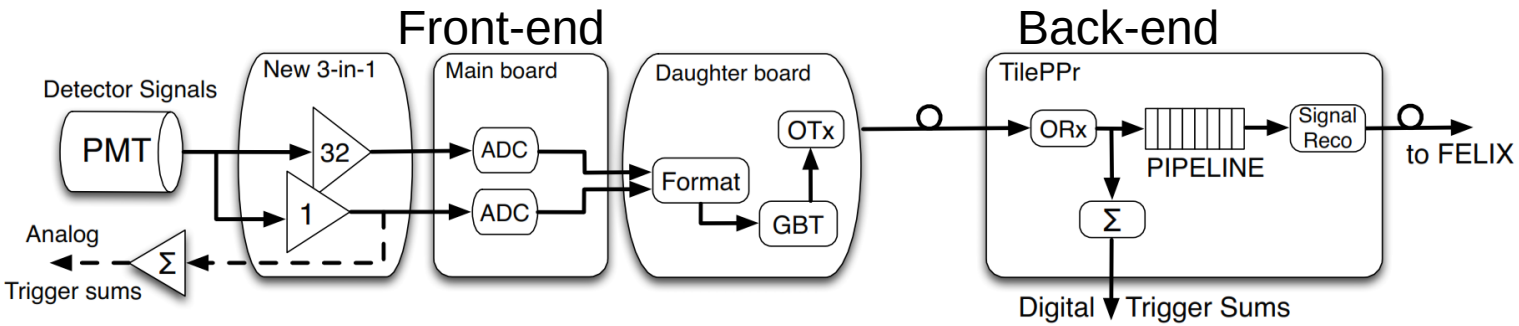


	Present	Phase II
Total BW	~205 Gbps	~40 Tbps
N. Fibers	256	4095
BW/mod.	800 Mbps	160 Gbps
Nb. boards	32	32
Nb. crates	4 (VME)	4 (ATCA)
In BW / board	6.4 Gbps	1.28 Tbps
Out BW / board$_{DAQ}$	2.56 Gbps	40 Gbps
Out BW / board$_{L1/L0}$	Analog	500 Gbps

- LHC plans to increase the instantaneous luminosity by a factor 5-7 around 2027
- Major replacement of the readout electronics
  - Higher reliability and robustness of electronics reducing single point failures
  - New readout architecture to provide digital trigger information at low latency for L0/L1 trigger systems with improved granularity
    - Pipelines, de-randomizers memories, TTC distribution moved to the back-end electronics
  - Higher radiation tolerance of electronics

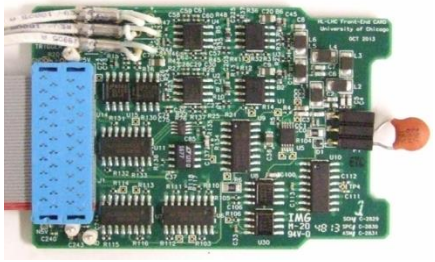
Demonstrator project and plans

- Evaluation the new readout schema and trigger system interfaces
  - TileCal demonstrator module is operative in our labs at CERN
- Plans for the demonstrator project
  - Test beam in 2015 and 2016
  - Possible insertion of one demonstrator module into the ATLAS at the end of 2016
  - Insertion of more modules during LS2 depending of the demonstrator results and performance
- Readout architecture for Phase II but keeping backward compatibility with the current system
  - Tile PreProcessor will interface the current TTC system (or FELIX) with the new front-end electronics
  - Back-end electronics will send Level 1 selected events to the current RODs
  - Provide analog trigger signals to the present trigger system



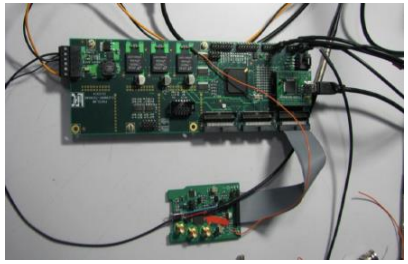
FE- Very front-end boards

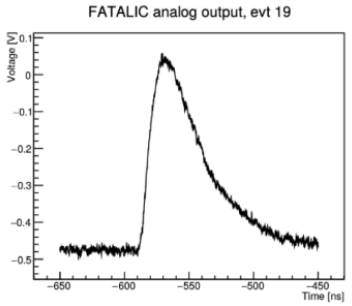
- 3-in-1 Cards: Based on current 3in1
  - Provides 3 analog signals: 2 x LG + 1 x HG
  - Calibration circuitry
  - Improved noise and linearity
  - Design ready and qualified
  - **Selected option for the Demonstrator as this option provides analog signals to the current trigger system**



3in1 card

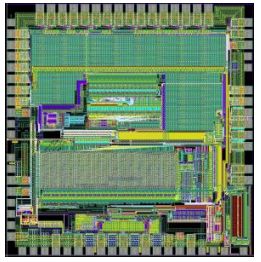
- FATALIC: Combined ASIC solution
  - Current conveyor and three shaping stages
  - 3 different gain ratios (1, 8, 64)
  - Integrated 12-bit pipelined ADCs
  - Tested during the last Test Beam → Shows good performance





FATALIC

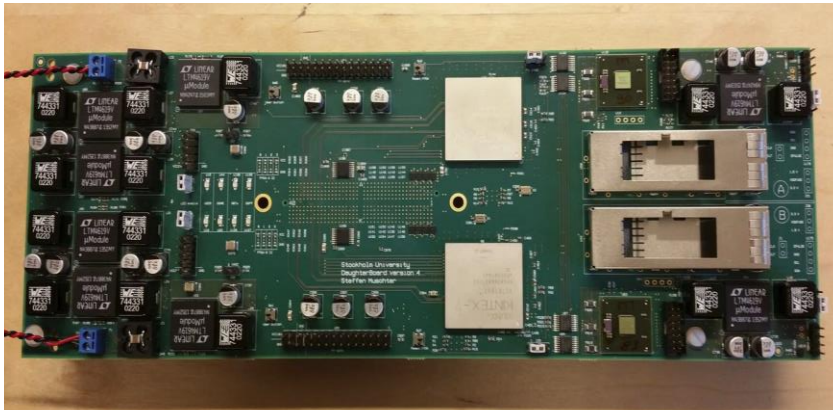
- QIE: Charge Integrator and Encoder
  - Current splitter with four ranges and gated integrator
  - 6-bit flash ADC at 40 MHz operation
  - 17 bit dynamic range in 10 bits
  - Integration in a FEB and DAQ development during the Q2 of 2016
  - To be tested during the next Test Beam (June 2016)



QIE chip

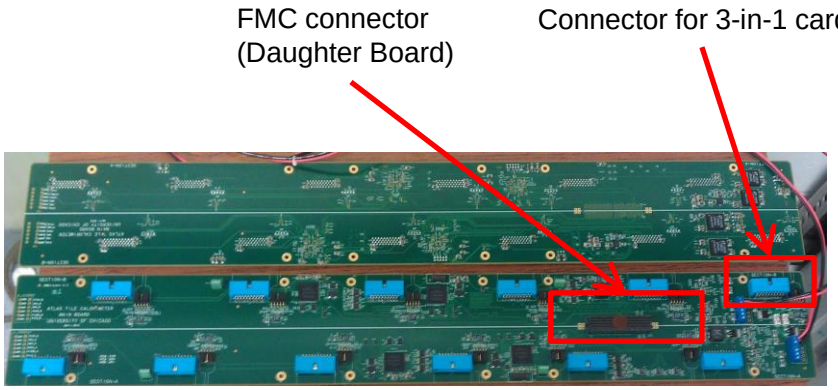
Daughter Board + Main Board

- High speed communication between front- and back-end electronics
  - Preserves 2-fold redundancy
  - Reception of timing and control commands
  - Transmission of digitized data to the BE
    - 12 channels x 2 gains every 25 ns
- Daughter Board v4
  - 2 Xilinx Kintex 7 FPGA
  - 2 QSFP module
    - 2 x 40 Gbps (up to 10 Gbps per lane)
  - 2 GBTx chips
    - One GBTx per QSFP+
    - Allows remote programming and operation from the BE



Daughter Board v4

- Main Board
  - Demonstrator → Version for modified 3-in-1 cards
- Functionalities
  - Digitize signals coming from 12 modified 3-in-1 cards
    - High and Low gain
    - 12 bits, 40 MSPs
  - Digital control of the front-end boards using Altera Cyclone IV
  - Routes the digitized data from the ADCs to the DB
    - 400 pin FPGA Mezzanine Connector (FMC)
    - 2 x LVDS at 560 Mbps per ADC
  - Low power voltage distribution
    - Divided into two halves for redundancy

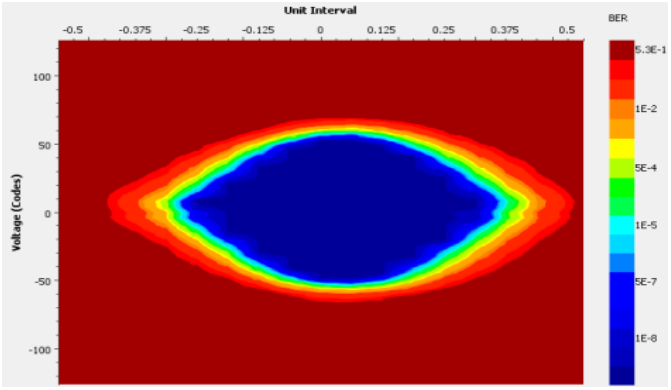


Main Board for 3-in-1 cards

TilePPr prototype

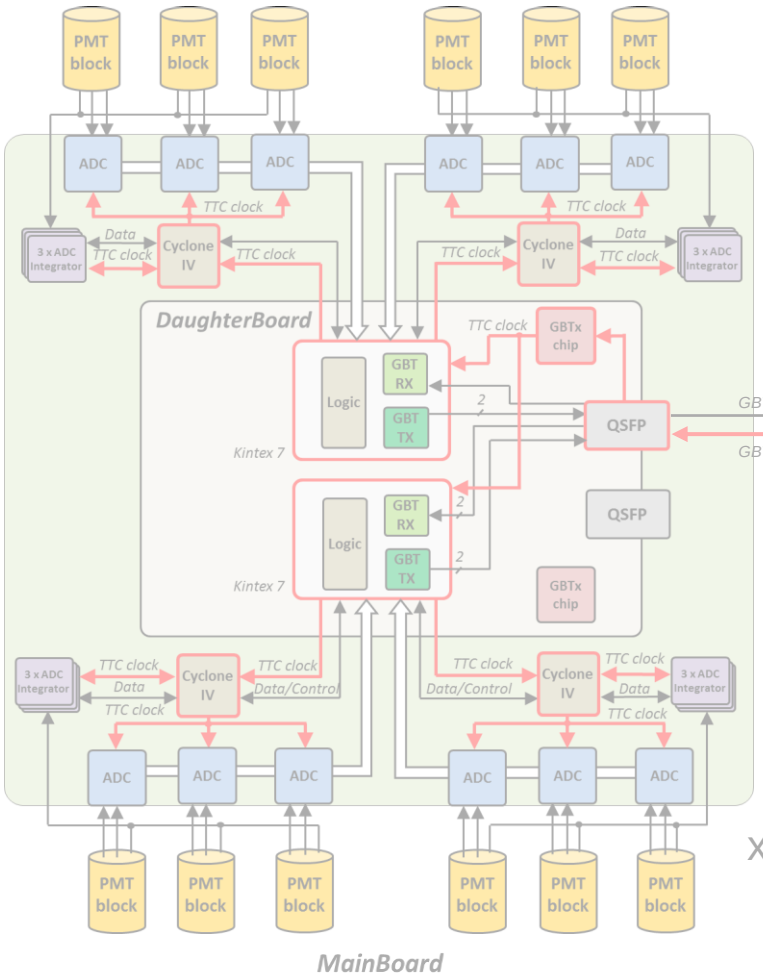
- Represents 1/8 of the final TilePPr module for the ATLAS Phase II Upgrade
- Double mid-size AMC form factor
  - ATCA carrier / µTCA
- Virtex 7 + 4 QSFPs (Readout)
  - Readout and operation of 1 complete TileCal module
  - Timing and command distribution to the FE
  - Interface with FELIX system
  - Energy and time reconstruction algorithms
- Kintex 7 + Avago MiniPOD TX (Trigger)
  - Evaluation of the interfaces with trigger systems and latencies between systems
  - Trigger data preprocessing algorithms
- DDR3 memories, FMC, GbE ports, PCIe, ...
- System has been successfully tested
  - BERT showed no errors during 115 hours
  - $5 \cdot 10^{-17}$ for a confidence level of 95%
  - 16 links at 9.6 Gbps with PRBS31 pattern

TilePPr prototype



Eye diagram at 9.6 Gbps (GTX)

Timing BE - Demonstrator



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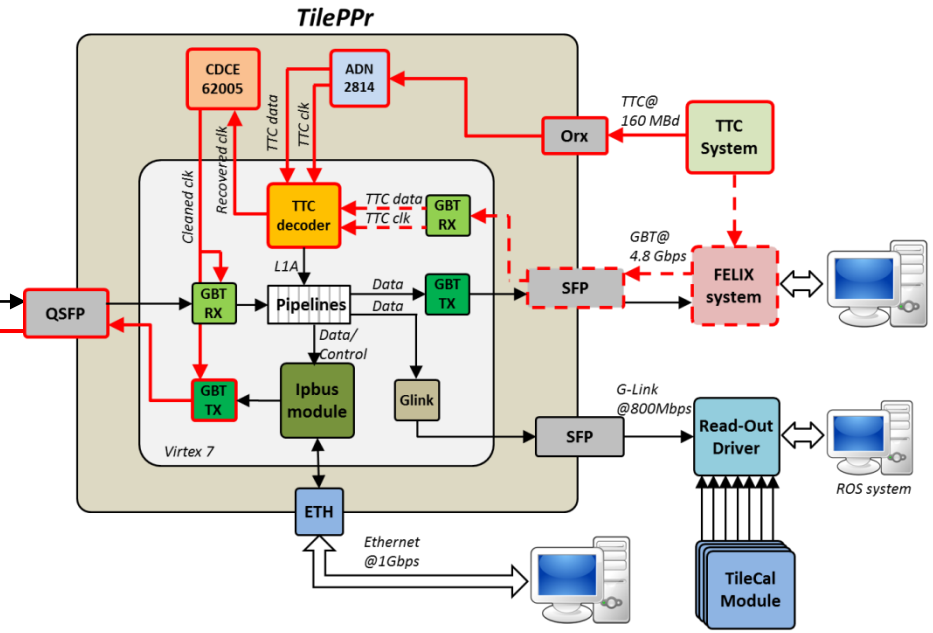
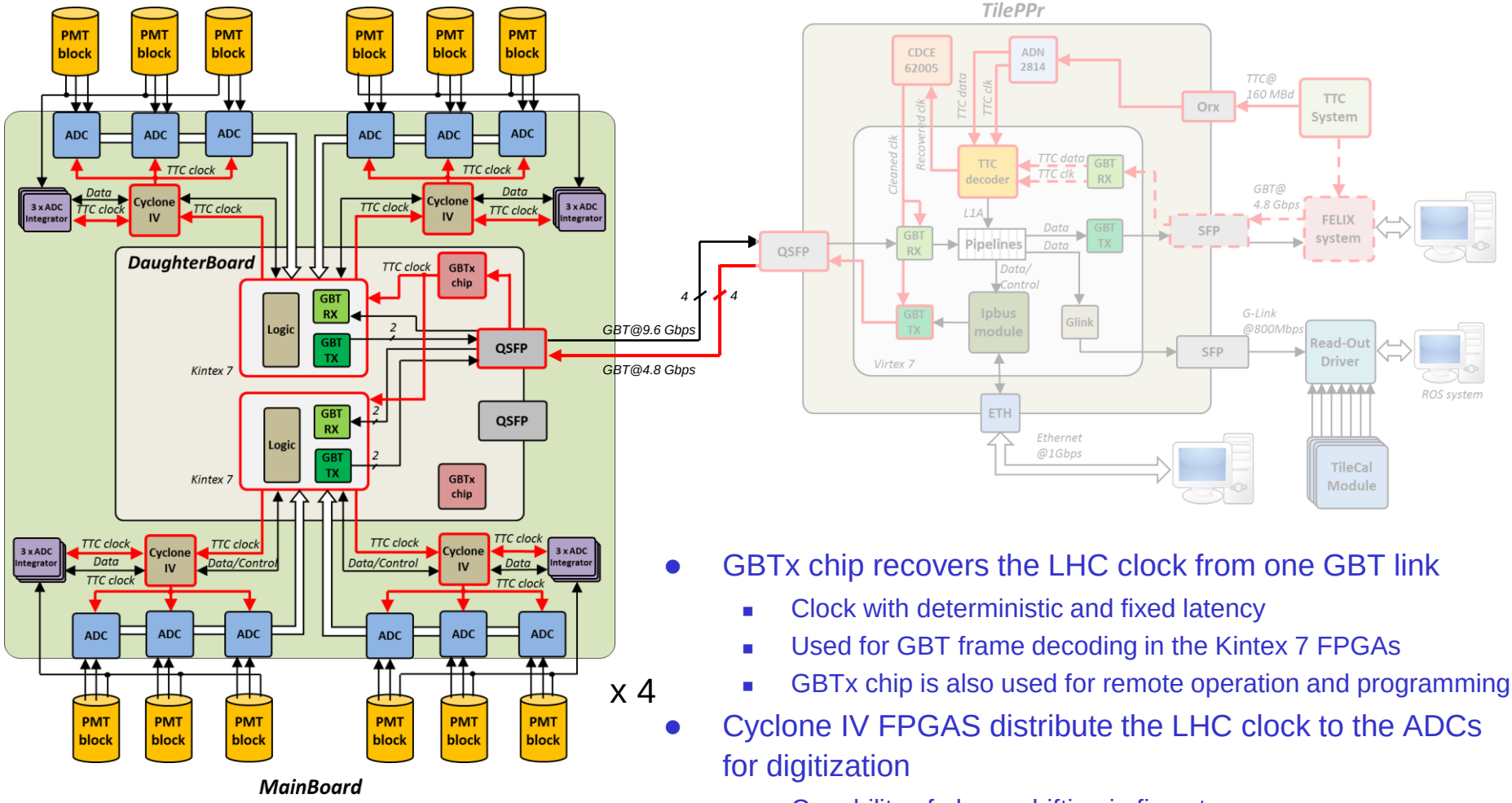


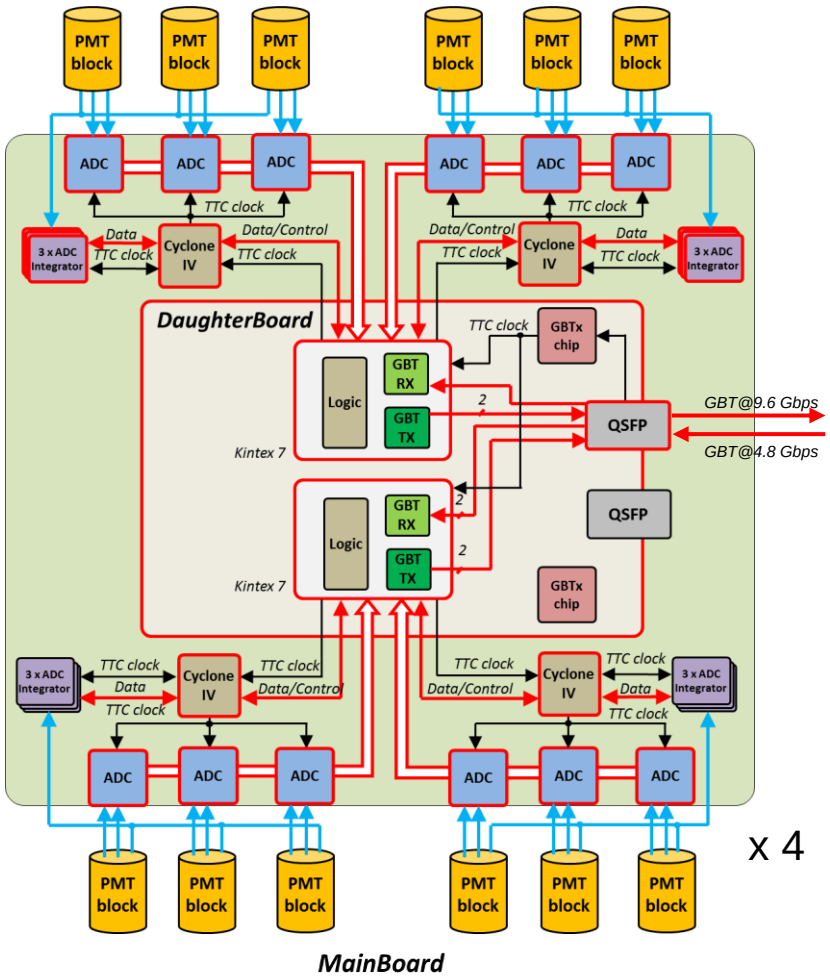
- TTC system provides FE configuration commands, LHC clock, and trigger signals
  - FELIX: clock is recovered through the GTX transceivers (FPGA)
  - Legacy TTC system: clock is recovered using a dedicated chip (ADN2814)
- External jitter cleaners chips are used to improve the quality of the recovered clock
- Clock is sent to the FE embedded with the data/commands
  - Downlink @ 4.8 Gbps
  - Transceivers configured in deterministic and fixed latency mode

Timing FE - Demonstrator



- GBTx chip recovers the LHC clock from one GBT link
  - Clock with deterministic and fixed latency
  - Used for GBT frame decoding in the Kintex 7 FPGAs
  - GBTx chip is also used for remote operation and programming
- Cyclone IV FPGAS distribute the LHC clock to the ADCs for digitization
  - Capability of phase shifting in fine steps
- Commands are received through the other three GBT links in the uplink – GBT@9.6Gbps

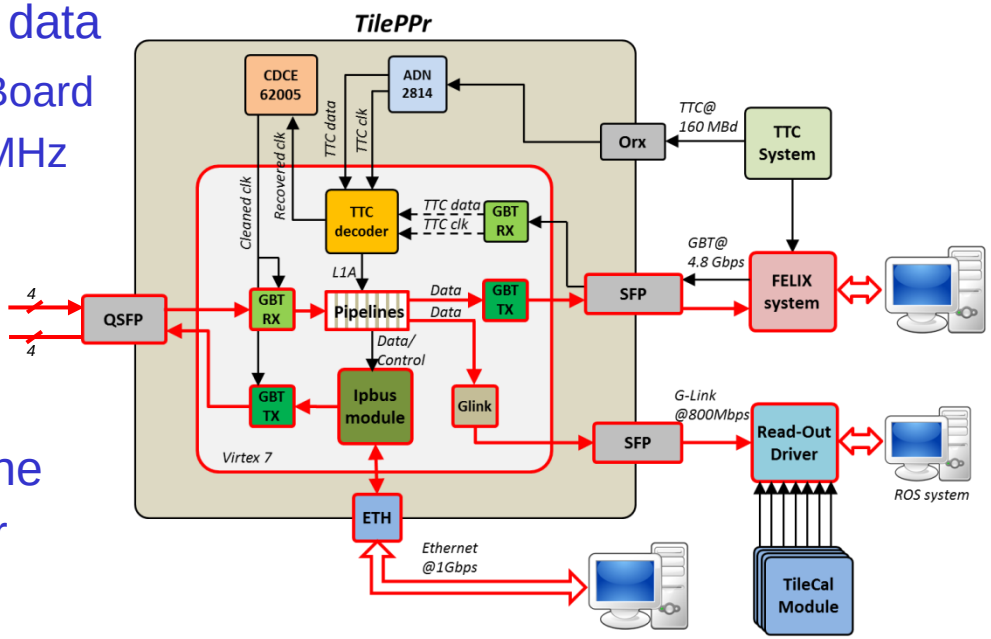
Dataflow FE - Demonstrator



- Front-end electronics transmits the digitized data to the back-end electronics for every bunch crossing
- No memory buffers in the front-end
- Each Kintex 7 FPGAs deserializes the data coming from 6 ADCs at 560 Mbps
- Event data is packed in a GBT frame with other monitoring info (HV, FE status, etc)
- Commands are decoded in the Kintex 7 FPGA and distributed to the MainBoard
  - Front-end boards settings
  - ADC configuration
  - HV electronics configuration
- Analog sums of the low gain signals coming from the PMTs are transmitted to the current trigger system for decision
  - In order to keep backward compatibility with the legacy trigger system

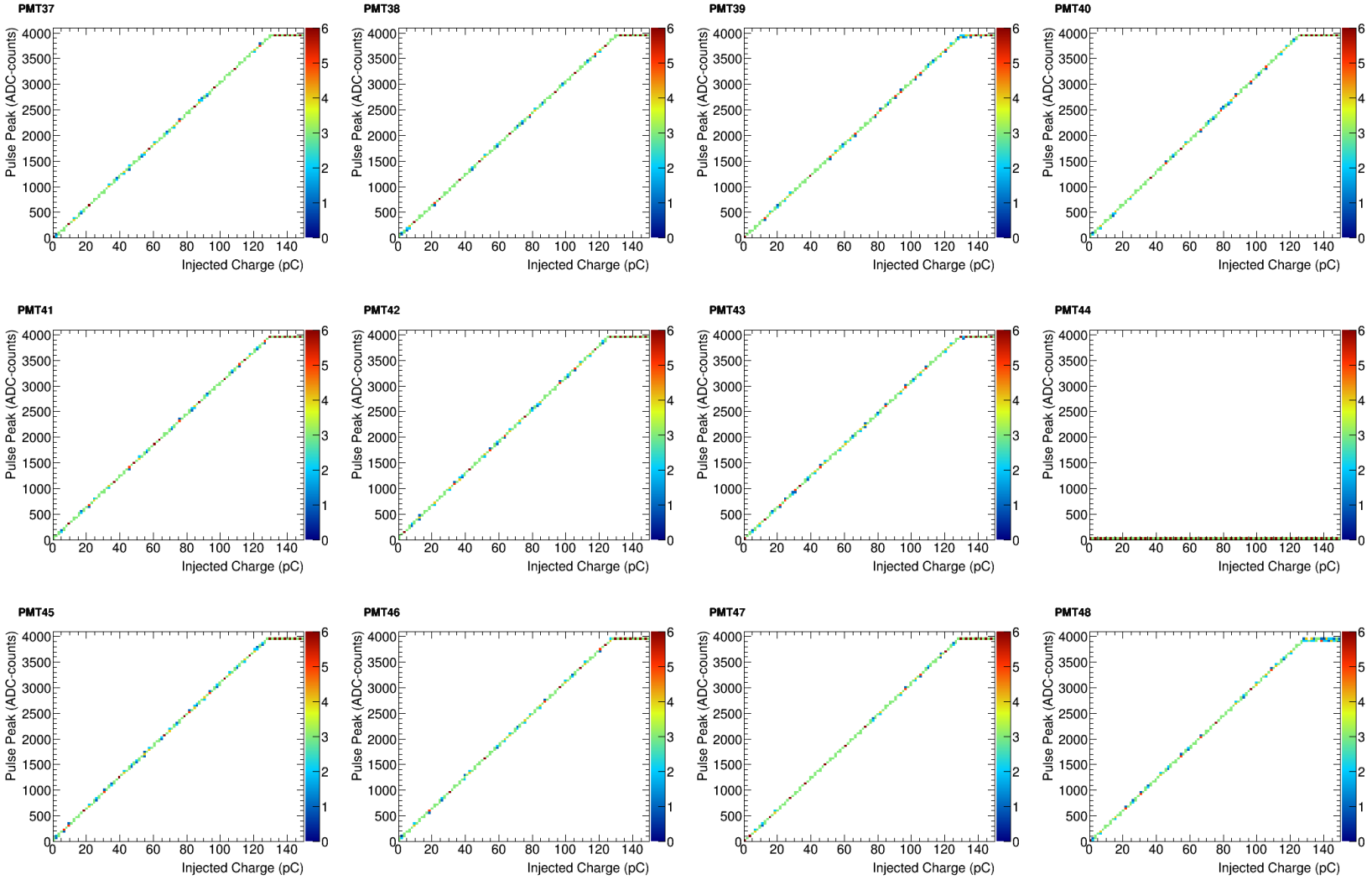
Dataflow BE - Demonstrator

- Continuous decoding and reception of data
  - 4 GBT links @9.6 Gbps per DaughterBoard
  - 12 bits x 12 channels x 2 gains @ 40 MHz
- Data is stored in circular pipelines
  - Samples with 2 gains x 48 channels (1 TileCal module)
  - 12.5 µs depth memories
- Selected event data is transmitted to the readout systems after a Level-1 trigger signal is received
- Three independent readout paths
  - FELIX system prototype: Phase II
    - 1 GBT link@4.8Gbps
    - 32 samples x 2 gains @ ~20 kHz
  - Legacy Read-Out Drivers: Backward comp.
    - 1 G-Link@800 MBps
    - 7 samples x 1 gain @100kHz
  - IPbus protocol via Ethernet: Monitoring
    - 32 samples x 2 gains



- Remote control / monitoring
  - Front-end boards configuration
  - High Voltage electronics
  - FPGAs status
  - Temperatures

Charge injection linearity test



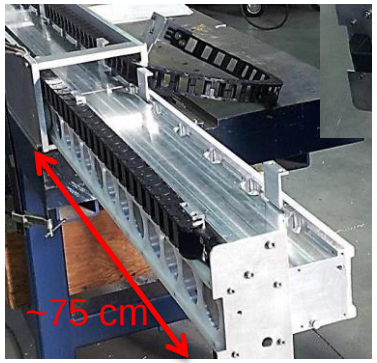
Summary

- R&D projects for ATLAS Phase II Upgrade includes the implementation of a new readout architecture:
  - Complete redesign of the front-end and back-end electronics for Phase II Upgrade
  - New trigger and readout strategies with new trigger algorithms
  - No buffers in the front-end electronics → all data readout at LHC frequency
  - LHC clock is distributed embedded with the downlink data
- Tile Demonstrator electronics project
  - Possibility of installing a TileCal demonstrator at the end of this year
  - Functional prototypes of front- and back-end electronics
  - Implemented redundancy in all front-end elements

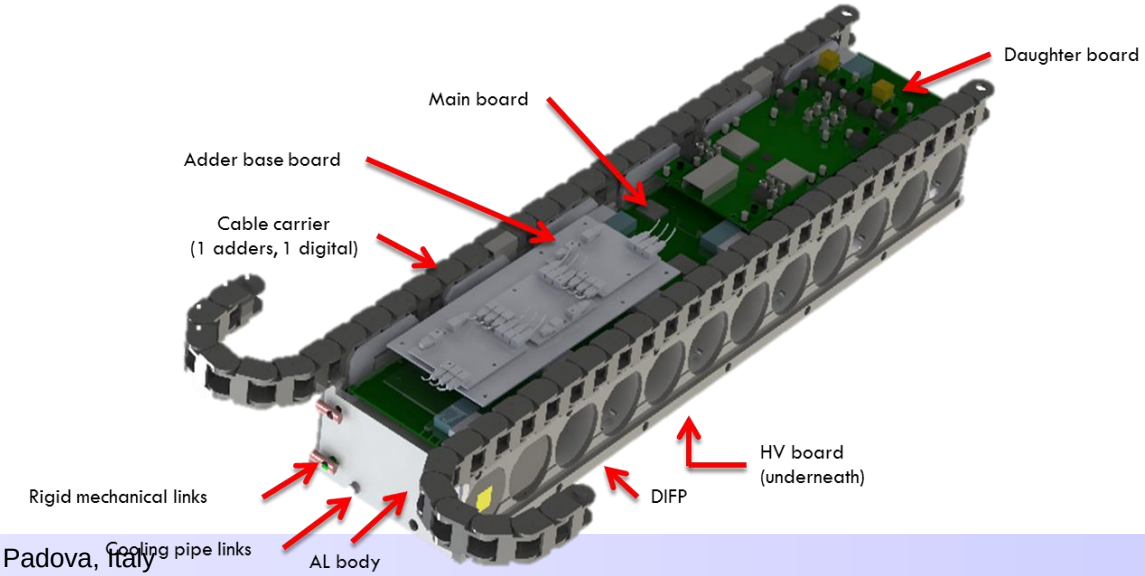
BACK-UP

Mini-drawers/Mechanics

- New design was made to replace the present super-drawers
  - Improve the operation, maintainability and handling
  - Internal cooling
  - Flexible cable trays
- Each module (drawer) will host 4 mini-drawers
  - 12 front-end boards and 12 PMTs
  - 1 Main Board + 1 Daughter Board with 2 QSFP+ modules
  - 1 HV regulation board: 1 out of 2 different options
  - 1 adder base board + 3 adder cards (only for the demonstrator)



Mini-drawer with cable carriers



TilePPr prototype

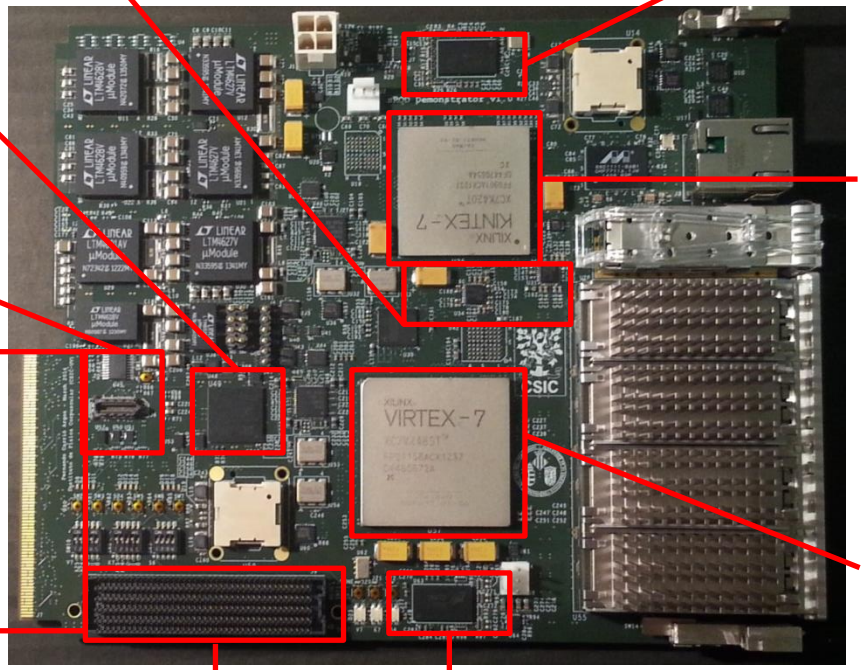
Xilinx Spartan 6
- Slow control capabilities (Clock management)
- Read back status of the system(IPMI port)

Module Management Controller (MMC)
- Power connection management
- IPMI protocol

AMC connector
- 12 V power connection
- Slow control path
- High-speed communication path with the carrier board / µTCA crate (GbE, PCIE, custom protocols)

2 x CDR IC
- ADN2814
- Clock/data from TTC

DDR3 512MB



Xilinx Kintex 7 FPGA
- XC7K420T
- 28 GTX transceiver @ 10 Gbps
- Data preprocessing
- Communication with Level 1 trigger system

Xilinx Virtex 7 FPGA
- XC7VX485T
- 48 GTX transceiver @ 10 Gbps
- Communication with FE electronics
- Data processing

DDR3 512MB

FMC connector
- Expansion funcionalities: ADC boards, test boards, ...

TilePPr prototype

TOP
BOTTOM

Power Modules
- Linear Technologies
- Low noise

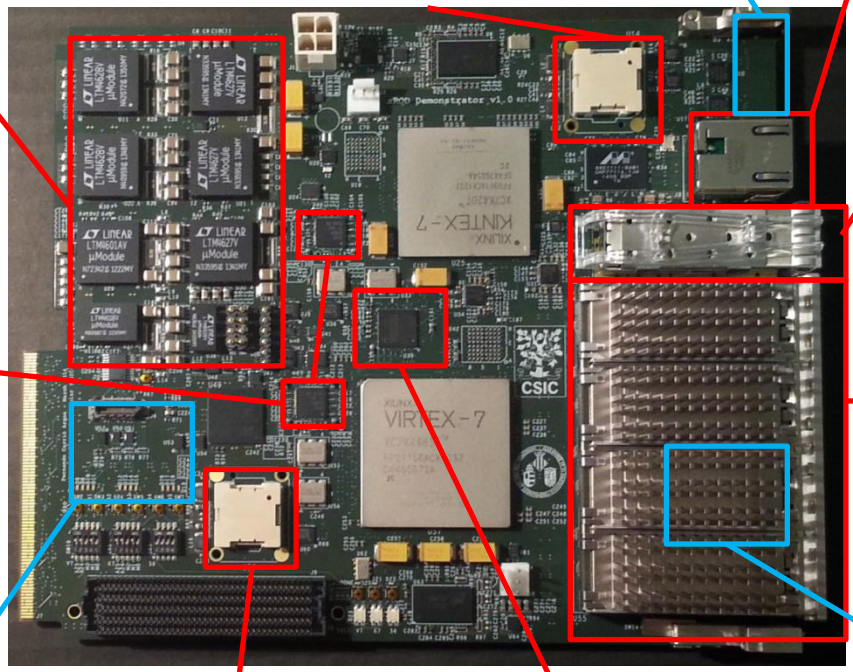
Jitter cleaners
- TI CDCE62005
- Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Power supervisory IC
- LT LTC2977
- Power sequencing
- Protection
- Current, voltage, temp.

MiniPOD TX
- 12 x 10 Gbps
- L1 trigger communication

UART-USB ports

Ethernet port
- 10/100/1000 Mpbs
- PC communication



SFP module
- TTC reception
- Communication with current DAQ system

4 x QSFP modules
- FE communication
- Each module at 40 Gbps
- Total max. BW: 160 Gbps

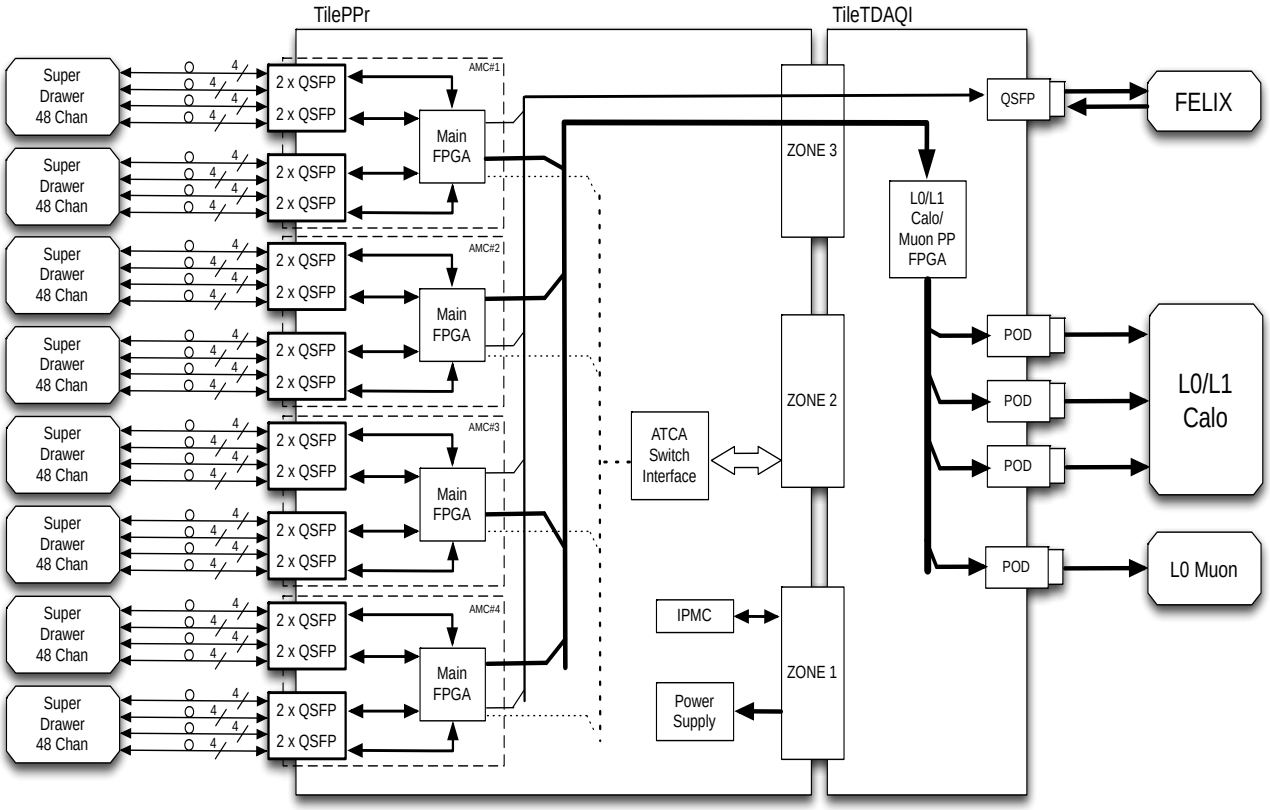
JTAG programmer

MiniPOD RX
- 12 x 10 Gbps
- Test purposes

Clock generator
- LMK03806B
- 10 diff outputs
- Low jitter

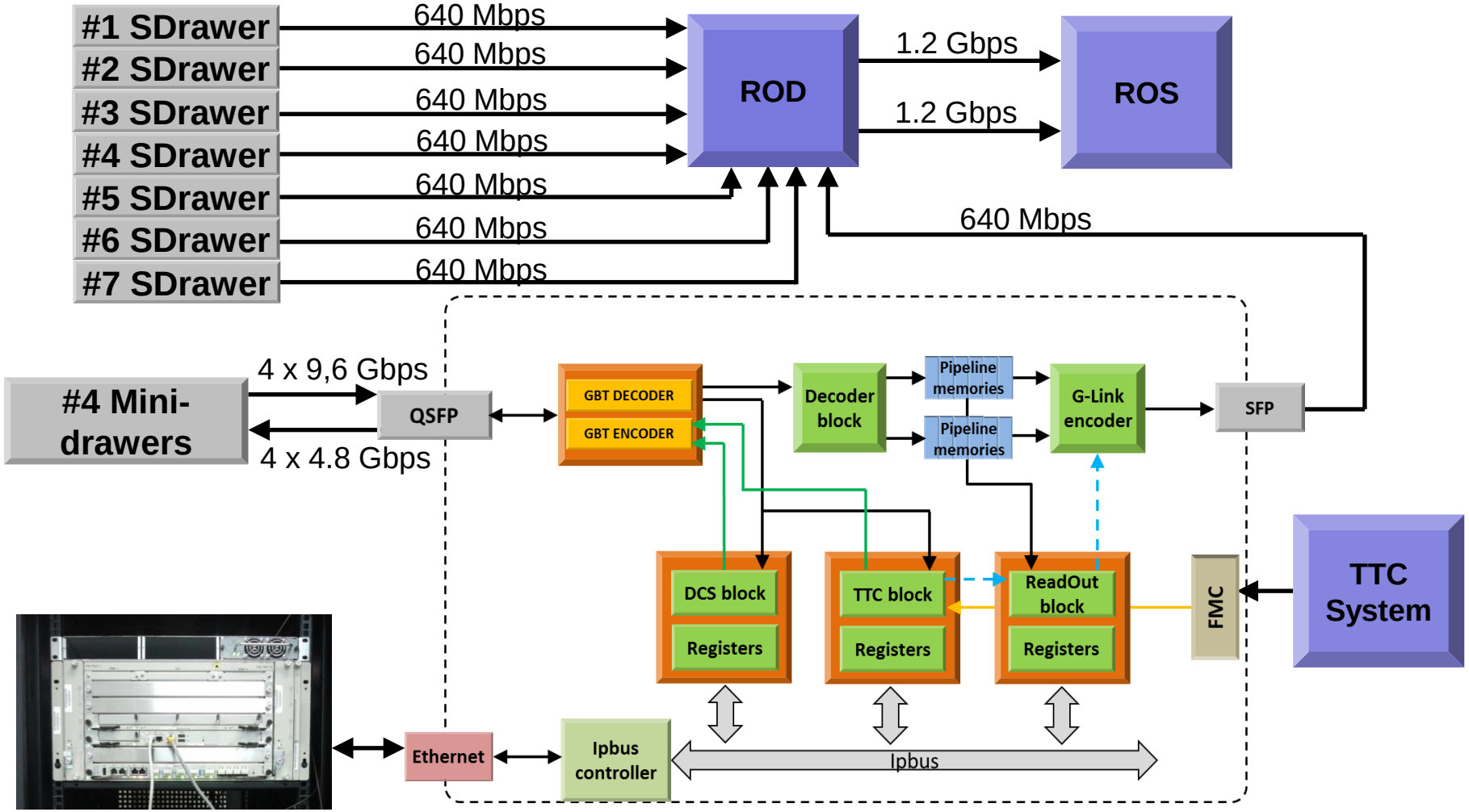
TileCal PreProcessors

- 32 TilePPr boards in ATCA format
  - ATCA carrier + 4 AMCs
  - Xilinx Kintex UltraScale
  - Implementation of L0 buffers
  - Real-time energy and time reconstruction algorithms
- 32 TileTDAQ-I
  - Rear Transition Module (ATCA)
  - Xilinx Kintex UltraScale
  - Preprocessed trigger data
  - Interface with L0Calo, L0Muon and FELIX system



Test Beam setup

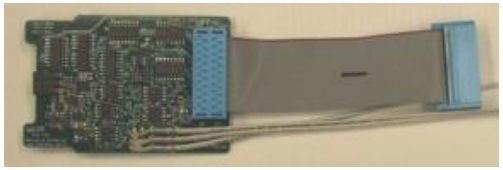
Readout schema - Demonstrator



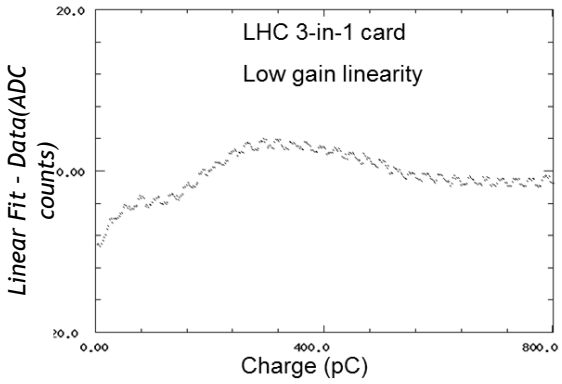
Firmware block diagram per Mini-drawer

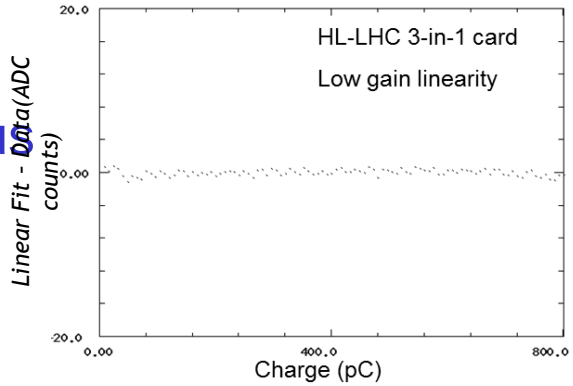
Front-End Board 1: Modified 3-in-1 cards

- Design based on the original 3-in-1 cards
  - Discrete COTS components
- Selected for the Demonstrator project
  - Unique option which can provide analog output to the Level-1 trigger
- Reception and shaping of PMT signals
  - Fast signal processing
    - 7 pole LC shape: 50 ns FWHM shaping time
    - Bi-gain readout: gain ratio of 16
    - Digitization in Main Boards using 12-bit ADC
  - Slow signal processing
    - Integrator to read out Cesium calibration data
  - Charge injection calibration and controls
- Better linearity and lower noise than previous version
- Status:
  - Prototype tested using COTS components
  - Passed radiation tests



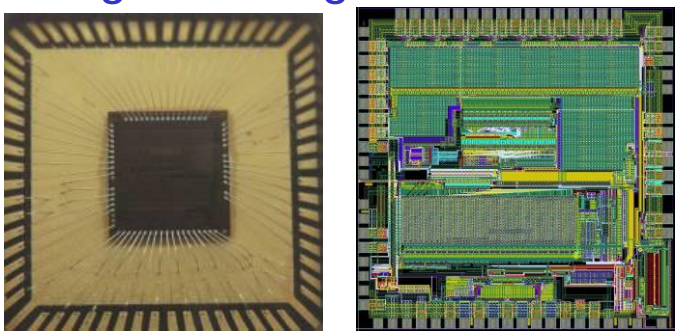
Modified 3-in-1 cards



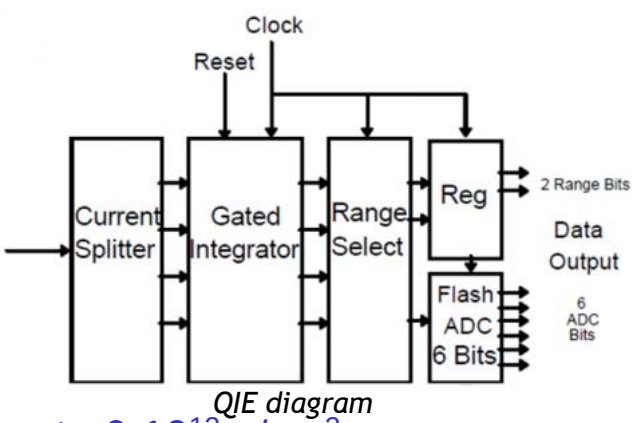


Front-End Board 2: QIE

- Charge (Q) Integrator and Encoder (QIE) chip from Fermilab
- Current splitter with multiple ranges and gated integrator with on-board flash ADC
  - Needs 4 clock cycles to acquire data
  - 40 MHz operation
  - 17 bit dynamic range in 10 bits
    - 6 bit ADC value
    - 2 bit range (4 different gain ranges)
    - 2 bits CAPID
  - Dead-timeless digitization
    - No pulse shaping
  - Also includes
    - Charge injection for calibration
    - Integrator for calibration with source
- Status:
  - 20 chips in hand, another 40 coming
  - Passed noise, dynamic response and TDC te
  - TID test up to 50 kRad showed good results
  - No Single Event Upsets in Shadow Register up to $6 \cdot 10^{12}$ p/cm^2



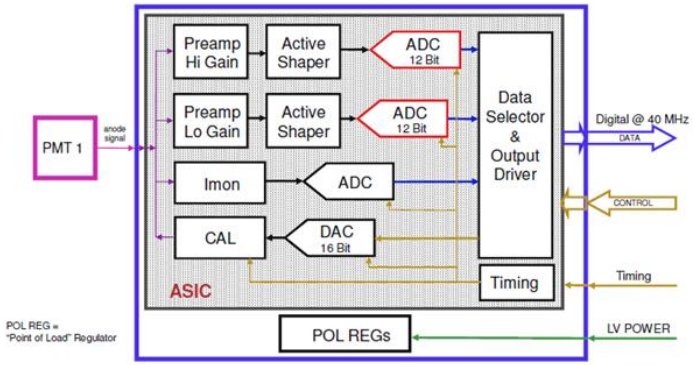
QIE 10.5



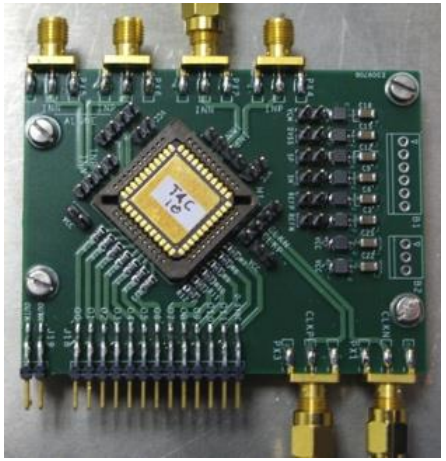
QIE diagram

Front-End Board 3: FATALIC

- Combined ASIC solution: FATALIC 3 + TACTIC
  - FATALIC 4 will include both ASICs
  - IBM CMOS 130 nm technology
- FATALIC 3 main features:
  - Current conveyor
  - Shaping stage with 3 different gain ratios (1, ϭ, 64)
  - 80 MHz operation
- TACTIC ADC main features:
  - 12-bit pipelined ADC
  - 40 MHz operation
- Status:
  - First prototypes of FATALIC 1 and 2 validated
  - Testing FATALIC version 3
  - Designing second version of TACTIC



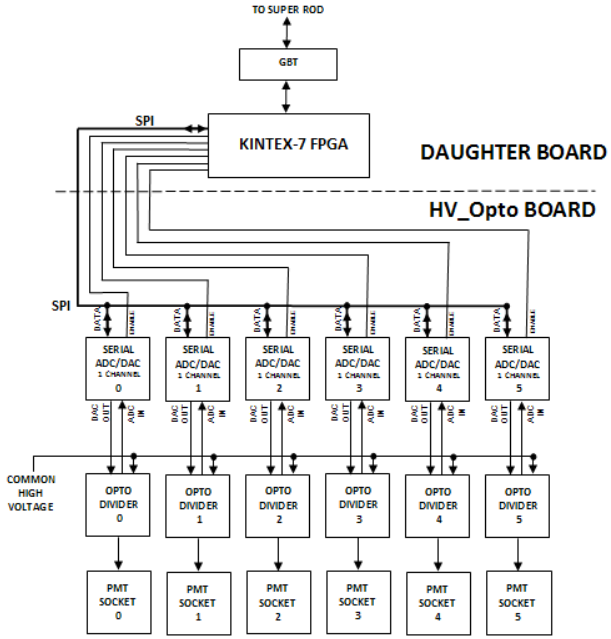
Conceptual Design of FE-ASIC Front-End Board

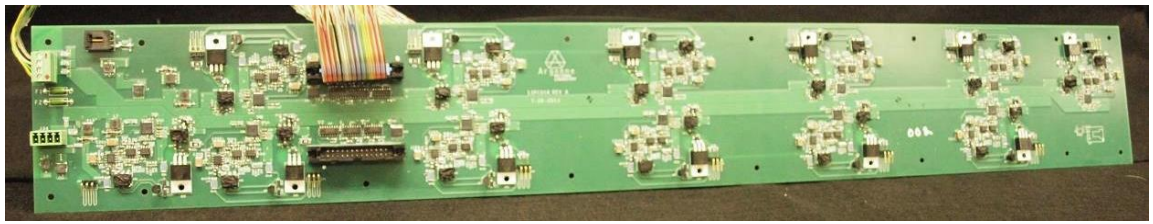


TACTIC ADC v1

High Voltage power distribution

- High Voltage system provides high voltage to the PMTs based on COTS components
- Front-end regulation board (HV Opto) based on the present design
  - Controlled by the daughter-board (Kintex 7) using SPI protocol
    - Switching on/off individual PMTs
    - Control of HV settings
  - Communication with the Detector Control System via the sROD using the GBT protocol
- Status
  - First HV Opto has been produced
    - Radiation testing in March 2014
  - Regulated HV distributed via 100 m long multi-conductor cables



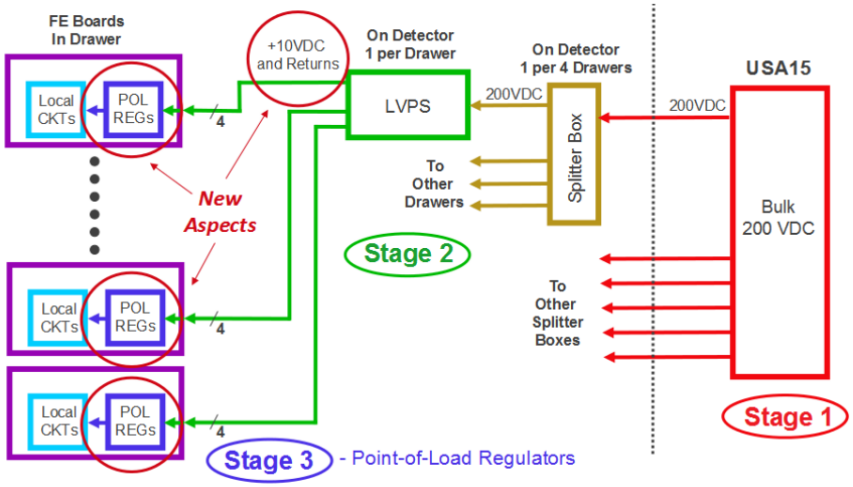


First prototype of HV_Opto board

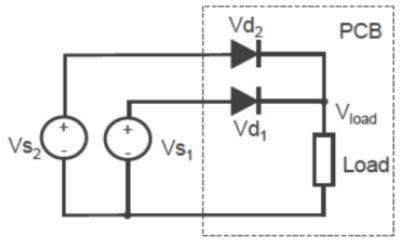
Prototype for radiation tests

Low Voltage power supplies

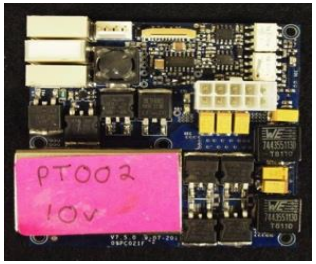
- Three stage power distribution schema
- Stage 1: bulk 200V_{DC} PS in USA15 (off-detector)
  - Provide power to four drawers (16 mini-drawers)
- Stage 2: LVPS boxes in front of drawers (on-detector)
  - New design includes 8 separate bricks which provides only +10V up to 20A
  - Each brick feeds half mini-drawer
    - Redundancy is possible using diodes OR
    - Requires a factor 2 in the current output
- Stage 3: Point-of-Load regulators
  - Point-to-point connection from brick to Main Boards
  - Diode OR provides power to the Main Board in case one brick dies
  - Completed TID tests on 5 COTS regulators
  - Non-Ionizing Energy Loss (NIEL) and Single Event Upset (SEU) tests in March 2014



3-stage power diagram



Redundancy



V8.0.1 brick