The data acquisition system for a fixed target experiment at NICA complex at JINR and its connection to the ATLAS TileCal readout electronics

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Abstract. Today's large-scale science projects have always encountered challenges in processing large data flow from the experiments, the ATLAS detector records proton-proton collisions provided by the Large Hadron Collider (LHC) at CERN every 50 ns which results in a total data flow of 10 Pb/s. These data must be reduced to the science data product for further analysis, thus a very fast decisions need to be executed, to modify this large amounts of data at high rates. The capabilities required to support this scale of data movement is development and improvement of high-throughput electronics. The upgraded LHC will provide collisions at rates that will be at least 10 times higher than those of today due to it's luminosity by 2022. This will require a complete redesign of the read-out electronics and Processing Units (PU) in the Tile-calorimeter (TileCal) of the ATLAS experiment. A general purpose, high-throughput PU has been developed for the TileCal at CERN, by using several ARM-processors in cluster configuration. The PU is capable of handling large data throughput and apply advanced operations at high rates. This system has been proposed for the fixed target experiment at NICA complex to handle the first level processes and event building. The aim of this work is to have a look at the architecture of the data acquisition system (DAQ) of the fixed target experiment at the NICA complex at JINR, by compiling the data-flow requirements of all the subcomponents. Furthermore, the VME DAQ modules characteristics to control, triggering and data acquisition will be described in order to define the DAQ with maximum readout efficiency, no dead time and data selection and compression.

1. Introduction

High energy physics experiments are confronted with the challenge of handling the volume of data recorded by particle detectors. One of such detector is the ATLAS Detector of the Large Hadron Collider(LHC), which records proton collision at about 50ns resulting to data output rate of about 10 Pb/s, with the anticipated upgrade of the detector to about ten times its previous recording energy which is about 6.5TeV (13 TeV collision energy), the data output rate would increase [1].

The TileCal detector which is a sub-detector of the ATLAS detector used to measure energy and position of hadrons [2], the scintillating tiles of the detector produce light when particles from collision crosses them, light are converted to analogue signal by the photo-multipliers and to digital signals by digitizers. The particles bunch crossing frequency in ATLAS experiment results in millions of particles event per seconds and in turns a large volume of digital signals.
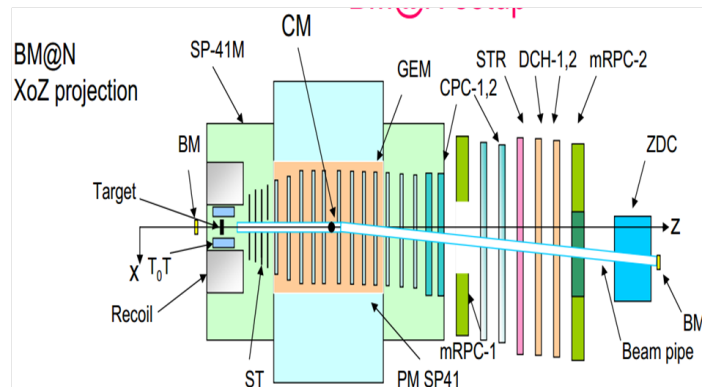
Figure 1. BM@N Setup (XoZ projection)[3].

In order to handle this data, high throughout electronics are developed. These electronics are high performance system, capable of selective reading and performing basic reduction and data filtering. A Processing Unit with 4 advanced micro X-Gene system on chip (SoC) was has been developed to either operate as a standalone device or a supporting device to other FPGA based system (sROD) in ATLAS experiment.

The Baryonic matter at Nuclotron (BM@N) project in the Nuclotron-Based Ion collider Facility (NICA) at the Joint Institute of Nuclear Research (JINR); is an experiment proposed to the study of AU+AU collision, with beam energy of up to $\sqrt{S_{NN}} = 11 GeV/n$ (Giga electron volts/particle) [3]. The proposed particle detectors (the BM@N detector Fig. 1) will be used to record particle produced by the fixed target experiment, by combining high precision track measurement with time-of-flight information for particle identification and total energy measurement for event characterization.

The BM@N detector has different sub-detectors, strategically positioned around targets to make different observations of the fixed target experiment. According to the BM@N letter of intent the BM@N setup will contain approximately 370000 channels of the front-end electronics, the sub-detector front-end electronics pre-amplify signals generated from observations. These signals are sent to the data acquisition (DAQ) system for digitization, compression and selection by high-throughput electronics (PU). The PU developed for TileCal in the ATLAS experiment will be used for First level processes (data check, flow control, zero suppression and integrity check), sorting distribution and Event buffering.

2. General purpose ARM-based Processing Unit
The challenge posed by High Volume throughput computing (HVC) and desire to handle this challenge with cost effective technology has led to the development of a processing unit Fig. 2 (schematics) from low cost ARM system on chips (SoCs). The PU design with several ARM processors in cluster configuration, this arrangement enhance the performance of the PU to be able to process at least 40 GB/s (Gigabits/s) of raw data fed through the I/O interface (PCI-Express , XAUI or bonded SFP+Connectors) [4]. This PU can be used for different high-level functions on the high-throughput raw data processing, such as spectral analysis and and online histogram monitoring.

3. BM@N Detector overview
Fig. 1 shows the schematic setup of the experiment, the setup combines different sub-detectors to observer different physics phenomena of the fixed target experiment.
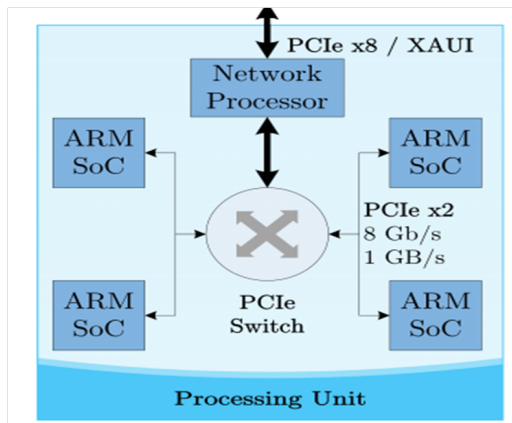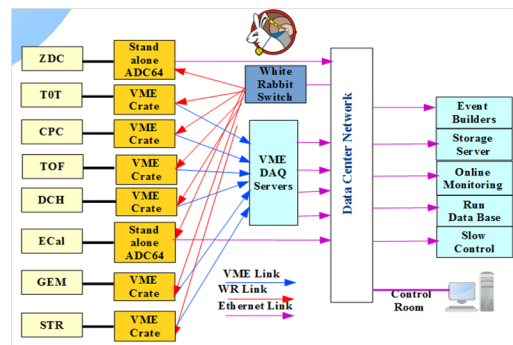
Figure 2. Schematics of the PU [4].

Figure 3. BM@N DAQ System.

- The Gaseous Electron Multipliers (GEM) detectors has twelve planes located downstream of the target inside the analyzing magnet (0.8T magnetic field) are designed to measure charge track multiplicity for particle identification.

- The time-of flight detector (TOF) are based on multigap resistive plate chamber (mRPC). The set up uses two TOF: the outer and inner TOF (mRPC-1) detector and the near TOF detector (mRPC-2).

- Fast Start detector (T_0T) is installed close to the target, the detector is designed to form T0 and L1 centrality trigger. The (T_0T) is a Cherenkov detector with time resolution of about 30ps, it can be combined with the multiplicity counter (MC) to L0-triggr signal.

- The Straw tubes (ST) for intermediate tracking.

- Drift chamber (DC) the setup uses two DC planes situated outside the magnetic field, they are use as intermediate trackers.

- Zero Degree Calorimeter (ZDC) is designed for collision centrality analysis by measuring the energy of forward going particle. it helps with central event selection at trigger level during data taking.

- Cathode pad chamber (CPC) is one of the tracking systems, it provides additional precise space coordinates of particles based on center of gravity measurement.

- Electromagnetic Calorimeter (ECal), designed to measure the spatial position and energy of particles in the fixed target experiment.

4. Data Acquisition and Trigger system overview

The BM@N trigger and data acquisition system (TDAQ) (Fig. 3) can be decomposed into three logical parts: the DAQ subsystem itself, the fast control and the trigger (FC+TU) subsystem: which intent to produce and handle the synchronous signals and the slow control (SC) system. For simplification of the interaction between DAQ elements, provision of standalone working mode for each sub detectors, easy reconfiguration of active sub-detector and easy hardware replacement, the DAQ hardware units are functionally subdivided into hierarchy by logical level along the data stream. The levels of the DAQ system comprise the Front End module of each sub-detector (FEM),Sub-event builder of subcomponents (SubEvent), Event Buider (EvB), Pool level and storage level.

4.1. Brief Description of the VME modules

- **ADC:** ADC are the waveform digitizer, they take continuous instant samples of input pulse signal at a fixed rate and output a complete digital representation of the signal. It is a 64-channel 12-bit with signal processing core module, with 62.5 Million sample per event with and Ethernet interface, it is designed to perform data readout by single fibre-optical link and capable of time and obtain synchronization by the white Rabbit switch.

- **TDC:** The time to digital converter is a time interval instrument; it is also know as a Time-Of Flight digitizer. it records the time-stamp of input pulses of particles. The main features are time stamping, multihit and trigger matching capability. The module is based on HPTDC chip developed at CERN, with a VME64X interface and VMEDAQ TTC bus (clock, trigger).

- **TQDC:** The TQDC is an FPGA based module, a multi-hit time-stamping TDC and also a waveform digitizer. it is used to measure pulse arrival time, charge and purse shape.

- **FVME2:** FVME2 is a 6U Master for the Data Acquisition system, the module automatically readout other VME module in chained mode. It is majorly a VME system controller with SFP serial link (800 Mbps or 2.5 Gbps M-Link).

- **FVME2TM/FVME2TMWR:** FVME2TM is the Trigger, Timing and Control Module for the VMEDAQ system, it has onboard time generator. It takes spill and trigger input used for data acquisition.

- **CTF:** CTF6 is the central trigger distributor equipped with white rabbit node core, the module is designed with 1 to 6 clock (125MHz LVDS clock) and trigger.

4.2. Data Acquisition system

The BM@N experiment uses the VME Data acquisition system standard, with the capability of run control, online data display, instant status monitoring and testing, automatic detection and configuration of modules. The VME crates host the BM@N readout module (ADC, TDC and TQDC), the VME controller modules (FVMEs) and the clock and trigger modules (FVMETMs). The BM@N modules digitize analogue signals (waveform and time) from dedicated sub-detectors, they store data in buffer for read out to the VME server over the VME link, The VME server is connected to the data network via 1Gb Ethernet link.

The central data center network hosts a general purpose processing unit which is capable of implementing data check, flow control, zero suppression and event building.

4.3. Trigger system

The FVME2TM/WR are the VME crates trigger modules, they have onboard 41.667 MHz clock generator used for trigger and time control. They receive input for spill and trigger from the central trigger processor and distribution, spill signals indicate the start of event, it is used as a gate for the data acquisition.

The LI trigger (Fig. 4) is a low latency signal (about 5 to 10 microseconds), it is distributed by CTF modules, generated by L1 trigger processor(CTF L1TP) and transmitted via high speed serial links. L1 trigger is required for modules equipped with ASICs (HPTDC), it is used to initiate a process that time-stamped and move data entries in modules to their buffers for L2 trigger. The L2 trigger (Fig. 5)signals are high latency digital signals (about 10 to 100 microseconds), implemented over the white rabbit network, used for selective readout from devices buffer.

5. Data Structure

Fig. 6 shows the Raw data format of the BM@N DAQ system. Raw data is stored as its is generated from the hardware; the minimal quantum of data is 4 bytes (32 bits). In the data
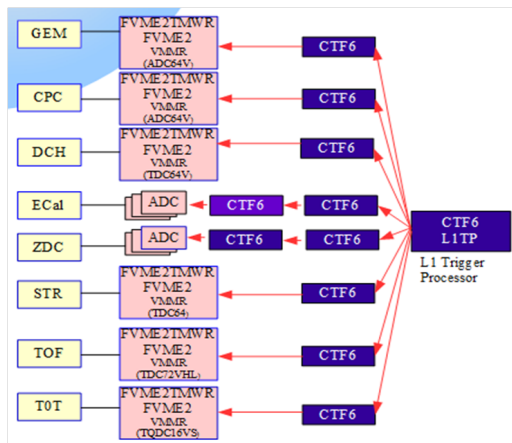
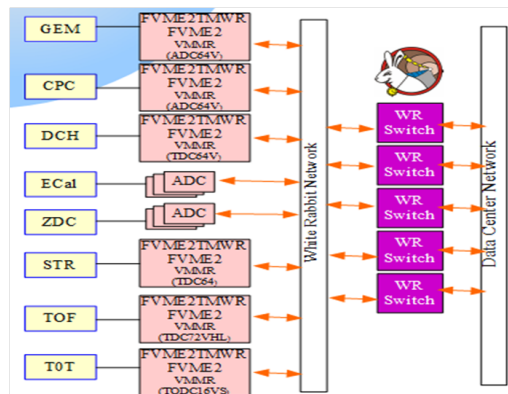**Figure 4.** L1 trigger

Figure 5. L2 trigger

stream raw data are split into spills, beginning with spill header (SHDR) and ending with spill trailer (STRL). The data in between the SHDR and STRL are sequence of zero or more events. Event begins with event header (EHDR) and ends with event trailer (ETRL), the data between EHDR and ETRL are sequence of module data block. Module data also starts and ends with module header (MHDR) and module trailer (MTRL), module data is any number of words of data, each module has their specific raw data format with module header comprising of slot number and module ID used to identify the slot and specifies the module a set of data is coming from.

The stand alone ADCs use M-stream waveform digitizer data format, data contain channels being read out in current event. The M-stream produces two types of data: the subtype 0 and subtype 1. The subtype 0 consist of a mask of channels being read out, they are used for zero suppression and basic reduction during data processing while the subtype 1 consist of waveform digitized data fragments as its payload.
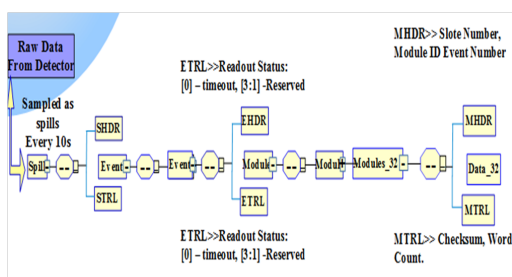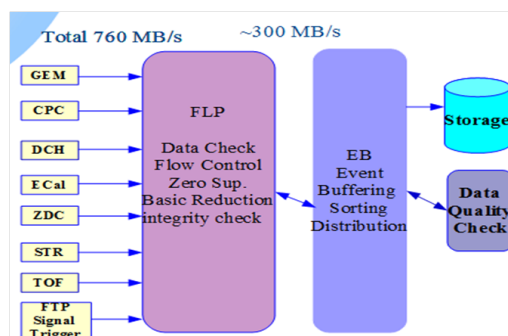

Figure 6. Raw data format

Figure 7. Data flow

6. BM@N data flow and event size

Fig.7 shows the DAQ system data flow, analogue signals from each sub-detector are amplified and digitized by dedicated front-end electronics. Raw data from waveform digitizer (standalone ADCs) are read uncompressed at high speed as compared with time digitizers (TDCs and TQDCs) to the first level process (FLP). The first level process is to reduce data flow by eliminating unimportant data, integrity check and zero suppression with nontrivial algorithms.

Table 1. BM@N Event size for 2017.

Detector	Readout card	Geometry	DAQ CH	occupancy	Bytes/ch	Bytes/Event
CPC	ADC64V	2*9129/64	285	3.84	4	4400
DHC	TQDC64V	2*2048	4096	0.06	4	1500
ECAL	ADC64	9*360	3240	0.30	44	44000
GEM	ADC64	96000/64	1500	3.34	4	23000
STR	TDC64V	2*6*450	5400	0.06	4	1700
TOF	TDC72V	2*2*1536	6144	0.06	8	3700
ZDC	ADC64	104	104	0.03	44	1400
Trigger	TQDC16V		1	1	100	100
Others			1	1	500	500
Total						80,000

A high performance PU is being developed for this purpose, the PU would be equip with 4 advance micro X-Gene system on chip (SoC) processors to enhance the performance.

Table 1 shows the estimated event size of 2017 BM@N experiment, data harness at trigger rate of 10kHz.

7. Conclusion

The total data rate from the frontend modules to FLP is about 760 MB/s, after the first level processing data would be reduced to 300MB/s at event building. Because of the rate of volume of data an high-throughput PU will be developed to handle data reception, flow control, integrity check and zero suppression at high speed with no dead time.

References

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