Performance of the cold powered diodes and diode leads in the main magnets of the LHC

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Abstract. During quench tests in 2011 variations in resistance of an order of magnitude were found in the diode by-pass circuit of the main LHC magnets. An investigation campaign was started to understand the source, the occurrence and the impact of the high resistances. Many tests were performed offline in the SM18 test facility with a focus on the contact resistance of the diode to heat sink contact and the diode wafer temperature. In 2014 the performance of the diodes and diode leads of the main dipole bypass systems in the LHC was assessed during a high current qualification test. In the test a current cycle similar to a magnet circuit discharge from 11 kA with a time constant of 100 s was performed. Resistances of up to 600 μΩ have been found in the diode leads at intermediate current, but in general the high resistances decrease at higher current levels and no sign of overheating of diodes has been seen and the bypass circuit passed the test. In this report the performance of the diodes and in particular the contact resistances in the diode leads are analysed with available data acquired over more than 10 years from acceptance test until the main dipole training campaign in the LHC in 2015.

1. Introduction

The main dipole (MB) and quadrupole magnets (MQ) of the LHC are actively protected by quench heaters and passively protected by a parallel bus bar circuit with a cold diode, operated in superfluid helium at 1.9 K [1].This protection system provides a fast decay of current in a specific magnet in case of a quench, while the 2.5 km long circuit of up to 154 series connected magnets is protected with an energy extraction system that allows a current decay time constant of 30 to 100 s. The bypass circuit is designed to supporting an exponentially decaying current from 13 kA with a time constant of 120 s for the dipole circuit and 50 s for the quadrupole circuit, during which the energy deposited in the diode is 1.7 MJ and 0.72 MJ, for a dipole and quadrupole diode respectively [2]. Not only the diode wafer itself, but the full by-pass circuit including bus bar and its connections need to withstand the current during decay.

The first design of the diode bypass dates back about 25 years and most of the more than 2100 diodes have been produced and qualified 10 to 15 years ago [2]. The diodes have been qualified and tested in multiple ways, but only since October 2014 over 800 diodes have been used for the purpose they were designed for, namely the protection of the main LHC magnets during magnet quenches.

The goal of this paper is to review the diode performance over the life time so far, including changes applied since the acceptance tests. Section 2 describes the diode stack and its critical components. In section 3 an overview of the powering and measurement history of the diodes is given. In section 4 the performance of the diode wafer is discussed and in section 5 to 7 the performance of the different bolted and clamped contacts are discussed. In section 8 an overall conclusion of the diode performance is given.

2. Diode stack and connections
Considering that the copper bus bars and copper heat sinks are well designed for their task, the diode stack has four critical electrical parts:

1.   The diode pack that includes the diode wafer, clamped between small copper heat sinks
2.   The contact surface between heat sink and diode pack with contact resistance $R_{C,HS-D}$
3.   The contact surface between the heat sink and bus bar with contact resistance $R_{C,HS-BB}$
4.   The contact between bus bar from the diode and the bus bar coming from the magnet
     a.   For the dipole these are called the "half-moon" connections with contact resistance $R_{C,HM}$
     b.   For the quadrupole stacks special connection plates connect the bus bar on the magnet side with the bus bar from the diode, having two contact resistances $R_{C,BB-CP}$

Parts 1 to 3 are part of the diode stack and normally the contacts and parts remain untouched during the lifetime of the diode and are always part of all the tests with current. Part 4, the contact between diode stack and magnet, is only made at the moment the diode is connected to the magnet, and was not part of the acceptance tests in any of the test stations.
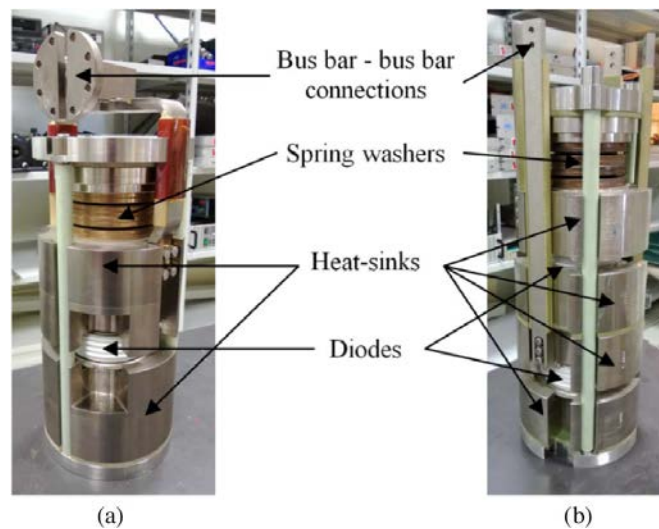
Figure 1. Picture of a (a) dipole diode stack and a (b) quadrupole diode stack.

3. Diode powering and measurement history
Acceptance tests have been performed on all diodes, focusing on forward voltage V_f, reverse voltage V_r and the diode wafer and heatsink temperature during discharge [2]. During those tests $R_{C,HS-D}$ was measured directly while $R_{C,HS-BB}$ and $R_{C,HM}$ and $R_{C,BB-CP}$ were not measured. In 2011 a quench propagation test in a small segment of the LHC revealed sudden, persistent and significant increases in resistance in diode leads. This led to rigorous investigation of the diode leads and diodes. In all cold powering tests the forward voltage was measured on the diode directly with local voltage taps, including those installed in the LHC. Table 1 list the history of all powering tests carried out on a substantial number of diodes as well as the corresponding diode and operating characteristics up to the Hardware commissioning (HWC) in 2015.

 Both MQ and MB stack types have identical diodes designed for a current of 13 kA. The MQ diodes have a smaller heat sink volume, designed for a decay time constant of 50 s, compared to 120 s for MB diodes. The Copper Stabilizer Continuity Measurement (CSCM) was designed to qualify LHC bus bar,

interconnections and diode bypass at non-superconducting conditions 20 K. After the first Long Shutdown (LS1) of the LHC, all main dipole circuits (RB) have been qualified in 6 runs up to 11.1 kA, qualifying them for equivalent LHC energy of 6.5 TeV. Figure 2 shows the current profiles used during the acceptance tests and the CSCM test as well.

Table 1. List of powering tests performed with the characteristics of the tests. B identifies the dipole diodes and Q the quadrupole diodes.

Test type	Acceptance test ENEA	Acceptance test CERN	CSCM type test	Warm test during LS1	CSCM 2014-15	LHC HWC 2015
Diode Type	MB & MQ	MB & MQ	MB & MQ	MB & MQ	MB	MB
T (K)	4.5	4.5	~20	~300	~20	1.9
Period	Up to 2005	2005-15	April 2013	2013-14	2014-15	2014-15
Number of stacks tested	> 1232 MB > 392 MQ	> 100 MB > 60 MQ	154 MB 47 MQ	1232 MB 392 MQ	1232 MB	> 800 MB
Current (A)	13000	13000	9000	10	11100	Up to 11100
V_f	Yes	Yes	Yes	Yes	Yes	Yes
V_r	Yes	Yes	No	No	No	No
$R_{C,HS-D}$	Yes	Yes	Yes*	MB: Yes* MQ: Yes	Yes*	Yes*
$R_{C,HS-BB}$	No	No	Yes*	MB: Yes* MQ: Yes	Yes*	Yes*
$R_{C,HM}$ $R_{C,BB-CP}$	No	No	Yes*	MB: Yes* MQ: Yes	Yes*	Yes*
References	[2]	[3]		[4]	[5]	

*the resistance is not directly measured, but the full diode lead resistance is measured.
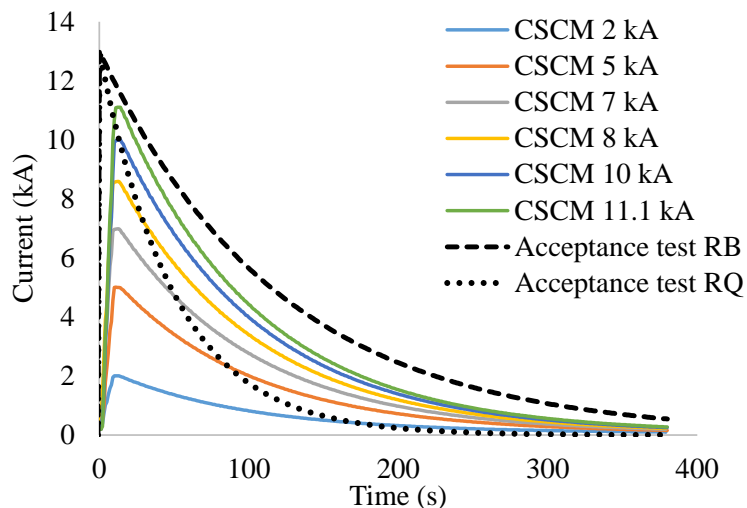

Figure 2. Current decay profiles during the 6 runs of the CSCM tests for dipole circuits compared to the acceptance test current profile for the MB and MQ diodes.

## 4. Performance results of diode wafers

During the acceptance tests, all diodes were tested at 13 kA with a time constant of 120 s for 8 to 10 times. Only 2 % of the diode stacks were rejected because of wafer defects like revers bias voltage V_r and 0.3 % because of a change in forward bias characteristics [2]. After installation of the diodes on the magnets, no failure of the diode wafer has been observed. During the CSCM type tests in 2013, a particular and repeatable feature of the diode opening at rather low current was observed in 13 % of the tests. The CSCM test has a particular powering scheme allowing the power converter to accommodate the strong change in inductance of the circuit when the diodes, parallel to the magnets, opens. In Figure

3 the voltage during 7 runs over the same quadrupole diode is shown with the current in the circuit. The current first only flows in the resistive magnet and is later shared between parallel circuit of diode and magnet. The opening voltage varies from run to run due to small variations in temperature. After opening about 1 kW of heating power warms the diode wafer temperature and V_f reduces due to temperature increase. In 6 out of 7 cases, an unexpectedly low voltage is recorded shortly after opening, which lasts about 10 seconds, followed by a return of V_f to its expected level. With the known $V_f(T)$ relation the voltage dip indicates a temporarily higher temperature of the wafer than expected. The dip is explained by a local turn on of the wafer with local heating, before the full diode turns on. In all observed cases V_f at high currents behaved normally and this feature is therefore not seen as a threat to correct diode functioning.
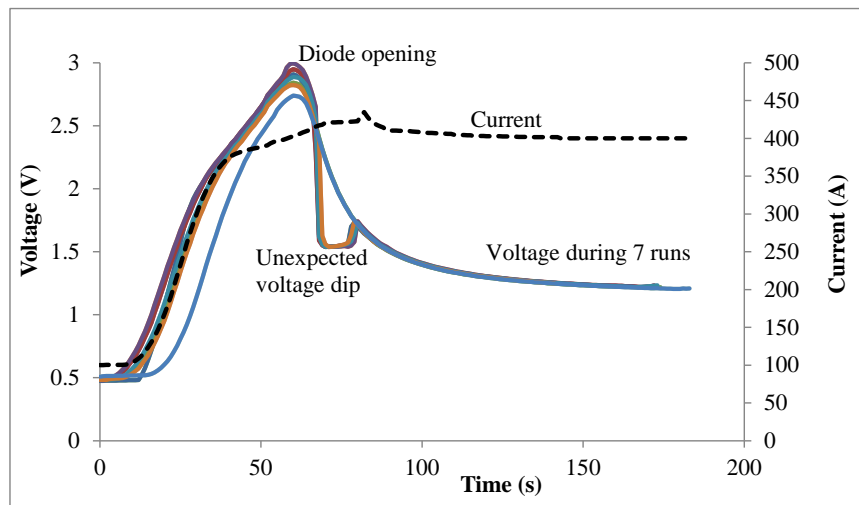
Figure 3. Voltage over the quadrupole diode in B11L3 during the CSCM type test at about 20 K. The dashed line shows the current in the circuit.

In 2014-15 the CSCM test on all 1232 main dipole bypass diodes was performed successfully and all diodes by-pass circuits proved operational [5]. A characterisation of the wafer is made by measuring the voltage at the end of the decay when the current reaches 1 kA. In Figure 4, the voltage for 25 % of the diodes is shown for the 6 CSCM runs. With the $V_f(T)$ the temperature range of the diode wafers is calculated and no outlier has been observed.
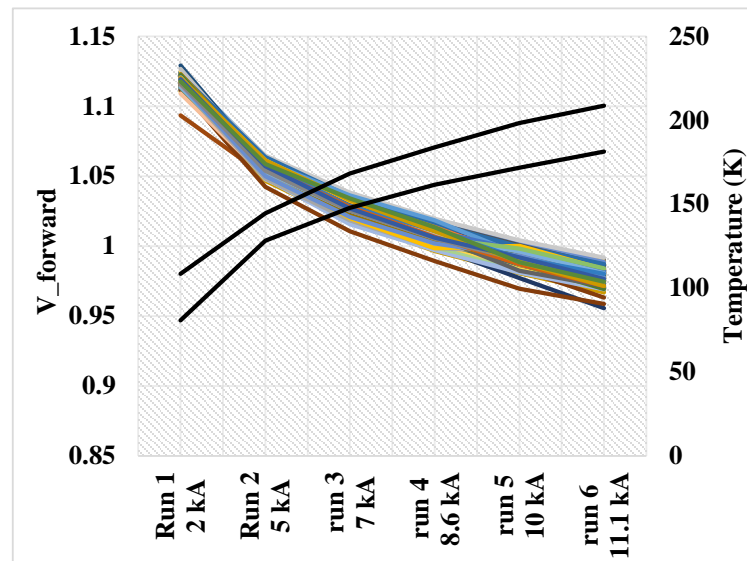
Figure 4. Forward voltage at a current of 1 kA during the decay in the six runs of the CSCM test for 308 out of 1232 dipole diodes. In Figure 2 the current profiles for the 6 runs are shown. The temperature of the wafer is calculated with the $V_f(T)$ dependence.

5. Contact diode to heat sink

The contact of the diode to heat sink, measuring 8 cm in diameter, is assured by Cu-Be washers that keep the Ni-coated diode clamped in between the Ni-coated heatsink with a constant force of 40 kN for both MB and MQ stacks. During the acceptance tests the resistance was measured directly during the high current runs and showed resistances up to 8 μΩ. The discovery of sudden resistance increases in diode leads during quench tests in the LHC in 2011 led to a rigorous investigation of the resistances in the diode by pass. Specifically during special tests at CERN, large variations in resistance were revealed. In many cases, sudden increases were observed when powering the diode for the first time with a short pulse at intermediate currents of 5 to 10 kA [6] [7]. In general, increasing current and/or high energy depositions in the diode would decrease the contact resistance [3]. In the worst case the contact resistance increased to 200 μΩ during the 10 kA CSCM discharge and reduces after increasing the power deposition in the following run [5]. Even in this case, the CSCM qualification test at 11.1 kA was completed successfully. Not a single case of malfunctioning or overheating was observed.

As the resistance during the high current runs is influenced by the current and temperature, a low-current measurement at 100 A to 400 A is used to compare the condition of the diode surface before and after the high-current runs. The most relevant data set is taken on 154 dipole diodes in LHC sector 23, where before and after LS1 the CSCM test was conducted. Figure 5 shows the resistance variation over time before and after the CSCM tests at 100 A to 200 A at 1.9 K and during LS1 with 10 A at 300 K. Although the measurement covers two diode leads the resistance variations are likely in $R_{C,HS-D}$. A cyclic trend is visible, wherein the high current powering leaves an increased resistance, while during the 18 months period at room temperature partially exposed to air, the resistance decreases. After the second CSCM test in 2014, the average resistance reached a higher value than in 2013 which may be caused by the different current levels reached during the tests.
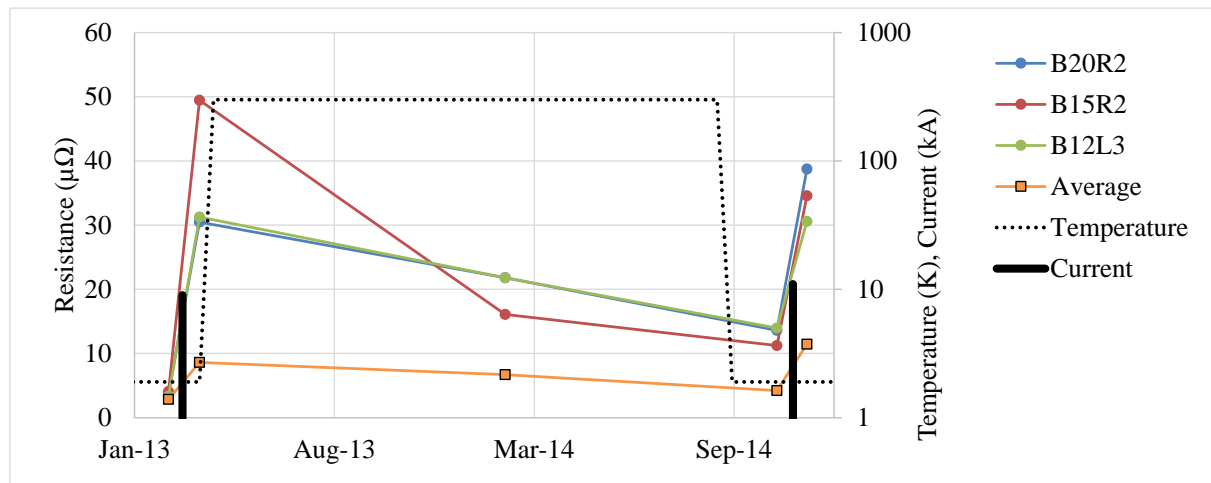
Figure 5. Resistance variation over time for the 3 diode leads in locations B20R2, B15R2, B12L3 showing the highest resistances and the average over 154 leads. The temperature of the circuit and the current during CSCM tests are indicated.

During the CSCM test in 2014-2015 on all dipole circuits, the resistance tends to increase on average during the first 5 runs and decreases after the last run [5], see Figure 6. No negative effect on diode functioning of the rather high resistances has been identified during the tests.

The large variations in the heat sink to diode contacts are believed to be due to partial oxidation of the Ni surfaces in combination with the movement of the micro-contacts during the initial powering. A resistance decrease is observed over time after 1.5 years at room temperature and also after short high-current powering in the order of several minutes where the temperature may reach close to melting temperature at the local contacts. The hypothesis that oxygen diffuses away from the local Ni-O contact points needs further investigation.
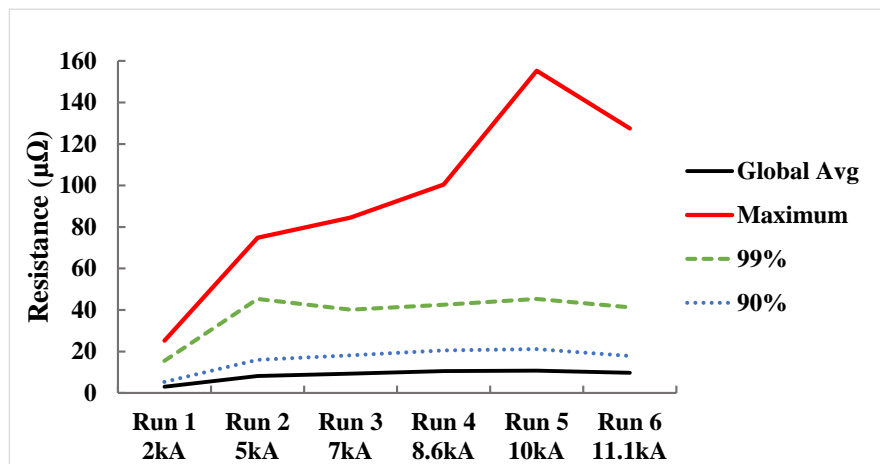
Figure 6. Low current resistance measurement of the diode leads during the CSCM test on 1232 dipole diode stacks. The resistance includes two diode leads. The average and maximum resistance are given in solid lines, 99% of the resistances is below the dashed line and 90% below the dotted line.
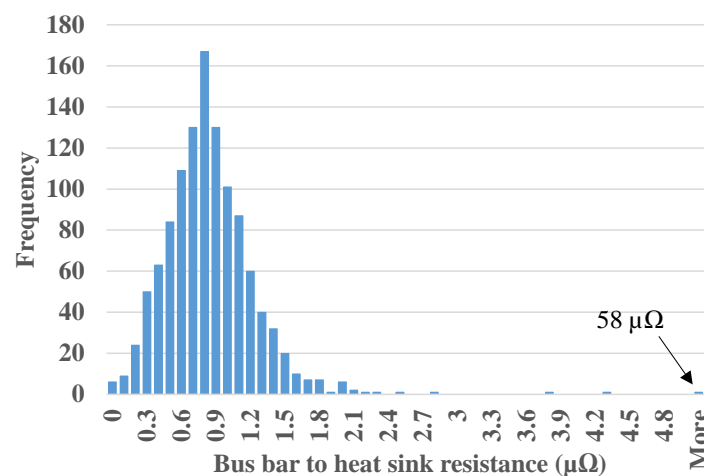
6. Heat sink to bus bar connection

6.1. Dipole heat sink to bus bar connection

During the warm measurements in 2014 the bus bar to heat sink resistance was only measured in series with the heat sink to diode contact and half-moon contact. Direct local measurements of $R_{C,HM}$ were only

measured if the full lead resistance exceeded 15 μΩ. No excess resistance has been reported during LS1 measurements on $R_{HS\text{-}BB}$ and also during special tests at CERN where this resistance was directly measured and a stable resistance below 2 μΩ was recorded [3] [7].

6.2. Quadrupole heat sink to bus bar connection
During special tests at CERN, all 56 diode stacks equipped for measuring this resistance during CERN acceptance tests showed stable and low resistance contacts [6]. During the warm measurements in 2014, a measurement method was developed to measure the bus bar to heat sink resistance in situ. The method was applied on 73% of all diode stacks and revealed 7 contact resistances above the threshold of 2 μΩ that were consolidated, see Figure 7. In the remaining stacks only the full lead including $R_{C,HS\text{-}BB}$ was measured and remained within acceptance limits.

Figure 7. Distribution of bus bar to heat sink resistance for 288 out of 392 diode stacks with 4 connections each. One outlier of 58 μΩ was found and all contacts with higher than 2 μΩ have been remade.

7. Bus bar to bus bar connection
The bus bar to bus bar connection is the only connection made after the acceptance tests, hence these connection were only tested at high current during CSCM tests. In both the dipole and quadrupole bypass circuits these connections are the most critical in terms of thermo-electrical characteristics, since this connection lacks the heat-sink that is present in the other contacts [6].

*7.1. Dipole bus bar to bus bar connection,*
During the production stage significant anomalies were found in the bus bar to bus bar connections, also called half-moon connections, which is a four-screw bolted contact between Ni coated Cu parts. In many cases, a resistance of up to 600 μΩ was measured in this connection made at the factory for the first 210 magnets [7]. These connections were redone afterwards with slightly modified connections and improved installation procedures. Quality control was conducted during the following stages of magnet production and this problem was mitigated.

During the warm measurements in 2014, the bus bar to bus bar resistance was only measured in series with the heat sink to diode contact and the heat sink to bus bar contact. A detailed investigation only took place if the resistance of the lead exceeded 15 μΩ. In the diode stack of dipole magnet MB3058, a high resistance of 210 μΩ and 90 μΩ on both half-moon connections was revealed. This very high resistance, far above the acceptance limit of 2 μΩ [8] could potentially cause an serious thermal runaway during nominal operating condition. Opening of the diode box revealed non-standard washers and the connection was remade according to the correct procedures and quality assurance was conducted. With the CSCM qualification test all half-moon connections have been qualified to 11.1 kA operating current.

7.2. Quadrupole bus bar to bus bar connection
The bus bar to bus bar connections of the quadrupole diode leads were initially made with an intermediate Ni-coated copper plate that is bolted with 2 screws each to the Ni-coated Cu bus bars. During a review of all the main circuits by pass systems, this clamped connection was identified as mechanically under-dimensioned and a reinforcement was designed with additional stainless steel plates and Inconel studs, nuts and washers [3, 8]. During LS1, this reinforced design was applied to all 392 quadrupole diode stacks in the LHC. This major work involved opening of all the magnet interconnections and diode containers and it allowed measurement of all the contact resistances in the diode stack [4]. A maximum resistance of 26 μΩ was found before the consolidation, while after the consolidation all resistances were below 1.5 μΩ, hence below the acceptance limit of 2 μΩ [8].
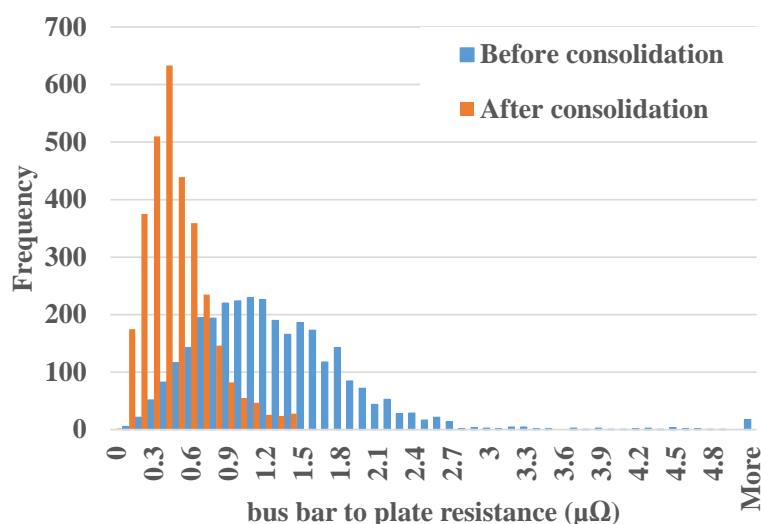
Figure 8. Distribution of bus bar to connection plate resistance for all 392 quadrupole diode stacks installed in the LHC before and after they were remade. Each stack has 8 bus bar to plate connections [4].

8. Conclusion
The protection diodes for the LHC were produced up to 15 years ago and have undergone multiple performance tests, powering cycles and thermal cycles. The diode wafer performance throughout these tests and powering cycles have shown reliable behaviour. A thorough investigation was conducted on the qualification of the diode lead connections after finding sudden resistance changes in the leads during LHC quench tests in 2011. Many experiments and calculations have been performed to establish the stability and limits of all the contact resistances.

The quality of the contact resistances in the quadrupole diode stacks installed in the LHC have been measured directly at room temperature during the long shutdown in 2013-14 and are within the acceptance limits after the consolidation work.

The quality of the contact resistances in the dipole diode stacks was measured for all contacts in series at room temperature during the long shutdown in 2013-14. In one case this revealed an excessive resistance at the level of the half-moon connections which was consolidated. In the following in-situ full current qualification test the full dipole by-pass circuit was qualified for LHC operation conditions at an energy of 6.5 TeV.

The performance of the diodes and leads in the LHC over the last 15 years, combined with the meticulous quality control and consolidation performed during the first long shut down in 2013-2014, and the correct protection of the magnets during hundreds of quenches in 2014-2015 so far gives a very strong confidence that the diodes will safely protect the magnets in the LHC during future operation.

Acknowledgements

References

[1]   Hagedorn D and Nägele W 1991 *CEC conference* Huntsville, USA

[2]   Brown D, Della Corte A, Fiamozzi Zignani A, Gharib A, Hagedorn D, Turtu S and Rout C 2003 *CEC/ICMC, Anchorage, Alaska* CERN-LHC-project-report-686

[3]   Roger V, Bajko M, Dahlerup-Petersen K, D'Angelo G, Dib G, Giloux C, Grand-Clement L, Izquierdo-Bermudez S, Prin H, Savary F, Verweij A and Willering G 2014 *IEEE Trans. Appl. Supercond.* vol 24, no. 3

[4]   Lackner F, Duret M, Grand-Clement L, Prin H, Principe R, Savary F, Scheuerlein C, Tock J-P, Triquet S and Verweij A 2015 *IEEE Trans. Appl. Supercond.,* vol. 25, no. 3

[5]   Rowan S, Auchmann B, Brodzinski K, Charifoulline Z, Panev B, Rodriguez Mateos F, Romera I, Schmidt R, Siemko A, Steckert J, Thiesen H, Verweij A and Willering G 2015 *IPAC15*, Richmond, VA, USA

[6]   Roger V 2012 *CERN internal note,* EDMS 1216375

[7]   Roger V 2013 *CERN internal note*, EDMS 1216363, 2013.

[8]   Verweij A and Charifoulline Z 2015 *CERN internal note*, to be published.

[9]   Verweij A 2011 *CERN* CSCM workshop

[10] Savary F, Bajko M, Bednarek M, Dahlerup-Petersen K, D'Angelo G, Dib G, Giloux C, Grand-Clement L, Izquierdo Bermudez S, Moron-Ballester R, Prin H, Roger V, Verweij A and Willering G 2014 *IEEE Trans. Appl. Supercond.,* vol. 24, no. 3