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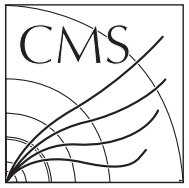

The Compact Muon Solenoid Experiment

Conference Report

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Experience from design, prototyping and production of a DC-DC conversion powering scheme for the CMS Phase-1 Pixel Upgrade

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Abstract

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Abstract

The CMS pixel detector will be replaced during the technical stop 2016/2017. To allow the new pixel detector to be powered with the legacy cable plant and power supplies, a novel powering scheme based on DC-DC conversion will be employed. After the successful conclusion of an extensive development and prototyping phase, mass production of 1800 DC-DC converters as well as motherboards and other power PCBs has now been completed. This contribution reviews the lessons learned from the development of the power system for the Phase-1 pixel detector, and summarizes the experience gained from the production phase.

Keywords: CMS, LHC Upgrades, Tracking Systems, Pixel Detector, Power Distribution, DC-DC Conversion

1. CMS Phase-I Pixel Upgrade

The present CMS pixel detector was designed for the LHC design luminosity of $1 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$. Under these running conditions it has shown excellent performance in LHC Run 1. It is expected that the LHC will surpass its design luminosity during the ongoing Run 2. For the present pixel system this would lead to an increase in hit detection inefficiency, reaching up to 16 % at $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ (or even 50 % if the LHC were to run at 50 ns bunch spacing) in the first layer. In order to maintain high efficiency in the measurement of charged particle tracks close to the interaction point, CMS will install a new pixel detector in the extended year end technical stop of the LHC in early 2017 [1], [2].

The new pixel detector will feature a read-out ASIC with improved rate capability, and an additional fourth detection layer to maintain robust pattern recognition under increased track densities. While the current consumption per channel has been kept similar to the present value, even with increased hit rates, the additional layer leads to a factor of 1.9 higher channel count. On the existing cable plant, which has to be re-used for the upgraded detector, this would lead to a factor 3.6 larger losses, which in turn would result in a rather inefficient power supply system. Operation of the pixel detector under such conditions would require a complete replacement of the power supply system and would lead to elevated and very likely unacceptable temperatures in the cable channels.

2. The Powering Scheme and its Implementation

A DC-DC conversion powering scheme was chosen to improve the efficiency of the power supply system [5], [6], [7].

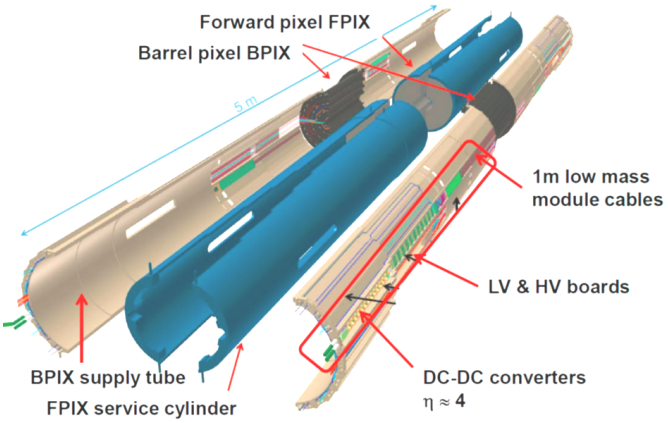

Figure 1: Overview of the CMS Phase-1 Pixel Detector. The dark and light grey volumes in the centre are the barrel and forward pixel detectors where the pixel detector modules measure the tracks of charged particles. The outer and inner cylindrical structures to both sides are the barrel pixel supply tubes and the forward pixel service cylinders, respectively, which hold the services for the detector modules: low voltage distribution through DC-DC converters, bias voltage distribution, and hybrids for the optical communication to and from the modules.

Power is transmitted at a voltage of 10 V over the approximately 50 m long supply cables and converted to 2.4 V and 3.3 V (or 3.5 V) at a distance of 1-2 m from the pixel modules by means of DC-DC converters. These voltages correspond to the required analogue and digital supply voltages of the 250 nm read-out ASICs when taking into account the voltage drops along the 1-2 m of low mass cabling to the pixel modules. Since the currents to be supplied over the approximately 50 m long cables are reduced by a factor of 3 to 4, the losses on these cables are reduced by an order of magnitude. This allows the new pixel detector to be powered through the existing cable plant and using the existing power supplies.

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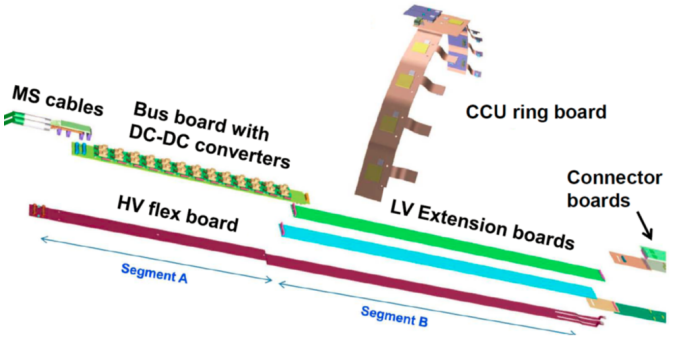

Figure 2: Overview of the PCBs employed in the barrel pixel power supply system.

The DC-DC converters are placed on the barrel pixel supply tube and the forward pixel service cylinder, at a pseudo-rapidity of around 4 and therefore outside the tracking volume (Fig. 1). A total of 1200 converters are needed. Each pair of 'analogue' and 'digital' converter (named after the voltage they supply to the read-out ASICs) powers one to four pixel modules. The required output currents are in the range of 1 to 2.5 A. In order to promote system stability both the external power supplies and the converters regulate the voltage locally at their output (no remote sensing). However, the external power supplies feature a slow regulation that compensates voltage drops on the long supply cables.

A chain of PCBs is needed to implement DC-DC converters into the pixel system. For the barrel part it consists of DC-DC Bus Boards that receive the 50 m long cables and carry 13 pairs of converters, Low Voltage Extension Boards that carry the supply voltages up to the point where the low mass module cables are plugged in, and a 1.3 m long High Voltage Flex Board that routes the sensor bias voltage from the long cables to the module cables (Fig. 2). Such a chain of boards sits in each of the 32 channels of the barrel pixel supply tube. A functionally similar arrangement is used for the forward pixel detector. The status of the converters can be read out and pairs of converters can be disabled through CCU Ring Boards that span eight channels each in the barrel pixel part (similarly in the forward pixel part).

Since the converters provide fixed output voltages, their values have to be carefully chosen such that, taking into account the load dependent voltage drops over the 1-2 m of low mass boards and cabling between the converters and the pixel modules, the input voltages to the read-out ASICs remain within the allowed ranges under all running conditions. Too low a voltage will impair the proper operation of the ASIC, in particular after irradiation, while too high a voltage may be harmful to the ASIC, causing permanent damage. For example, for a converter supplying the digital voltage to 4 modules of layer 3 with a total load current of 2.44 A, the voltage drop from the converters to the modules amounts to 580 mV at full load, i.e. full hit rate. Adding to this a converter output voltage spread of 50 mV, a load variation of up to -10 mV/A, a temperature variation of around 0.7 mV/K leading to a shift of about 30 mV between room and operating temperature, and finally a change of output voltage with radiation of about 30 mV leaves very little room to choose the converter output voltage. The final choice of the voltage values has been made based on detailed simulations and careful measurements of final versions of all boards and cables.

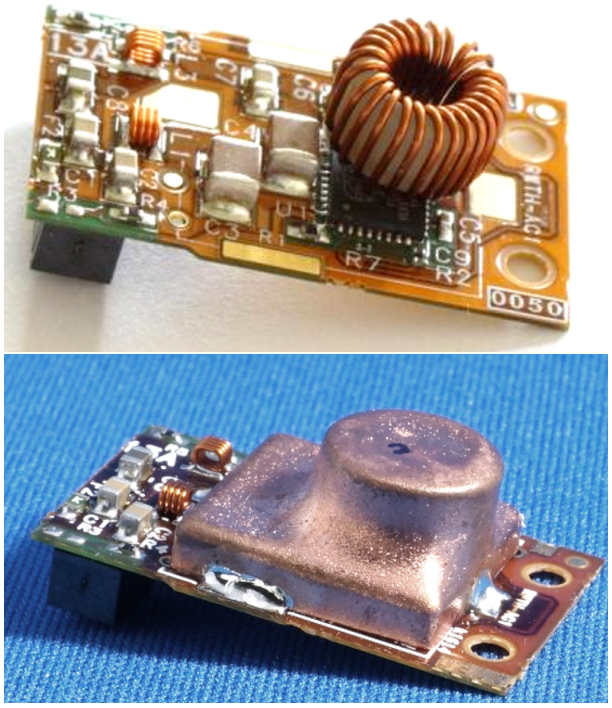

Figure 3: DC-DC converters without (top) and with (bottom) electromagnetic shielding.

3. DC-DC Buck Converters

The DC-DC converters to be used in the Pixel System have to operate in the 3.8 T magnetic field of CMS and a radiation field of up to 100 kGy and $2 \cdot 10^{14}$ n_{eq}/cm^2 (for an integrated luminosity of 500 fb^{-1}). Since no commercially available converters are designed to meet these requirements, an R&D program was launched at CERN and by CMS to develop and qualify appropriate DC-DC converters. Buck-type converters have been chosen as they require relatively few components and can provide large currents. CERN has developed the FEAST 2 ASIC that implements the high current switches required for the DC-DC conversion as well as including the control logic and protection features [3]. It is manufactured in a commercial 350 nm CMOS technology, with a high voltage module developed mainly for automotive applications. These ASICs have been shown to reach the required radiation tolerance and to be sufficiently immune to single event effects [4].

Based on this ASIC CMS has developed a DC-DC converter module that is tuned to the needs of the pixel system. It consists of a 2.8×1.7 cm^2 two-layer PCB that carries a FEAST 2 ASIC, a 430 nH toroidal air-core inductor, input and output filters and a 32 pin connector (Fig. 3). The ASIC is set to a switching frequency of 1.5 MHz and the output voltages mentioned above. Switching large currents at frequencies near the bandpass of

the pixel detector front-end electronics has been a major concern in the development of the powering system. An extensive R&D program including measurements of conducted and radiated noise and various system tests has lead to a DC-DC converter design that was shown not to have any negative influence on the performance of the pixel detector. An important part of this design is an electromagnetic shield that covers the ASIC, the toroid and the noisy parts of the PCB. It consists of a plastic core plated with 60 μm of copper on the outside and acts at the same time as a heat sink for the toroid. The thermal contact of the toroid to the shield is improved by thermally conductive grease. The shape of the shield had to be specially designed to the boundary conditions in the pixel system. The shield is soldered to the PCB. A large copper area on the bottom of the PCB acts as the cooling contact. The total weight of one converter is 3 g.

When the input voltage to the converters exceeds 5 V they commence operation through a soft start cycle that ramps up the output voltage within 440 μs and then regulates it based on a bandgap reference. The converters switch off if the temperature of the ASIC exceeds 103 °C or if the input voltage falls below 4.5 V, and restart again once conditions are again in the allowed range (with some margin). The converter output current is limited to 4.8 A. A solid state fuse will disable converters with excessive current values permanently such that the other converters (and modules) supplied by the same external power supply can still be operated. Individual converter pairs can be enabled or disabled and their status read back via slow control communications.

4. DC-DC Converter Production

While 1200 DC-DC converters are needed for the CMS Pixel upgrade a target of 1800 converters was set for the production. This surplus in production was deemed necessary to cover defects due to the untested FEAST 2 ASICs and due to other imperfections during production, to be able to reject converters in the tails of the output voltage distributions, and to have about 20 % fully functional spares available at the end of production.

The production proceeded in several steps. In the first step the PCBs, the toroidal inductor and the electromagnetic shields were manufactured in industry. After optical inspection and selection of inductors based on the measured inductance, these components were given to an assembly company that performed the placement and soldering of all components, along with several quality control tests: automated optical inspection, high-resolution X-ray imaging of all samples, micrographs of samples, and ten passive thermal cycles between −30 °C and +60 °C of all converters . This production followed the specifications of IPC-A-610D (class 3).

After reception the converters were subjected to a quick electrical test that measured the output voltage and tested the status bit and the enable feature. Slightly more than 10 % of the converters were rejected at this point due to a known feature of the (untested) FEAST 2 ASIC that results in a non-functioning status bit. This quick test was in fact performed twice: firstly at an intermediate step in assembly before the electromagnetic shield was mounted and secondly after reception of the finished converters.

A much more involved test followed, which consisted of 10 thermal cycles between −28 °C and +20 °C during which it was ensured that the converters were fully operational and delivered an output current of 3 A each (Fig. 4). Input and output voltages, input currents, status bits and temperatures were monitored. Furthermore it was checked that the converters could be switched on and off, both via the supply voltage and the enable feature, at the high and low temperatures of the cycles. The load current drawn from the converters was switched off at both temperatures for a short time. A special test stand was built for these tests in which 16 converters could be tested at a time. A throughput of about 80 converters per week was reached.

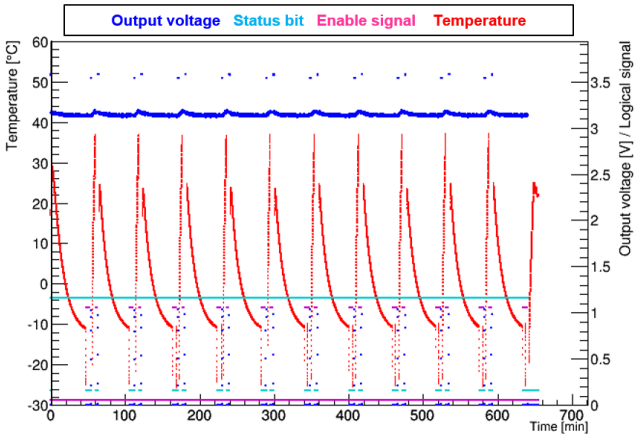

Figure 4: Example of one thermal cycling run. Shown are the temperature of the shield of one of the converters, the output voltage, the status bit, and the enable signal versus time. The load currents of the converters are switched off for a short time at both high and low temperatures, leading to increased output voltages during these short intervals.

This thermal cycling under load has proved to be a very valuable test. During pre-production converters were identified that would switch off after several thermal cycles. This was traced to non-uniform solder deposition under the FEAST 2 ASIC BGA package. This had not been spotted by optical inspection and (low resolution) X-ray tests at the originally chosen assembly company and ultimately led to a move to a different assembly company and to the requirement of production according to IPC-A-610D (class 3). The much improved quality control at the new assembly company spotted another issue (voids in the soldering of a certain SMD resistor, which was fixed by a change of supplier), demonstrating once more the importance of quality control and assurance.

At the end of production and testing of all 1800 DC-DC converters 14 % of them showed the faulty status bit feature of the FEAST 2 ASIC. The remaining yield was 99 %: only 14 converters showed various other defects without an obvious pattern. 21 % of all faults were identified during the active thermal cycling, most of them during the first two cycles, but at the latest during cycle number 4 of 10. The efficiency, defined as the ratio of output to input power, is high (around 80 %) and uniform. The spread of the output voltages has a standard devi-

ation of 35 – 50 mV, as expected from the accuracy of the SMD resistors used to set the output voltage (Fig. 5 top). The lower diagram in Fig. 5 shows the measured load regulation, defined as the change in output voltage with output current. It is small and negative as it should be in order to avoid a possible positive feed-back between the converter and the linear regulators in the front-end ASICs.

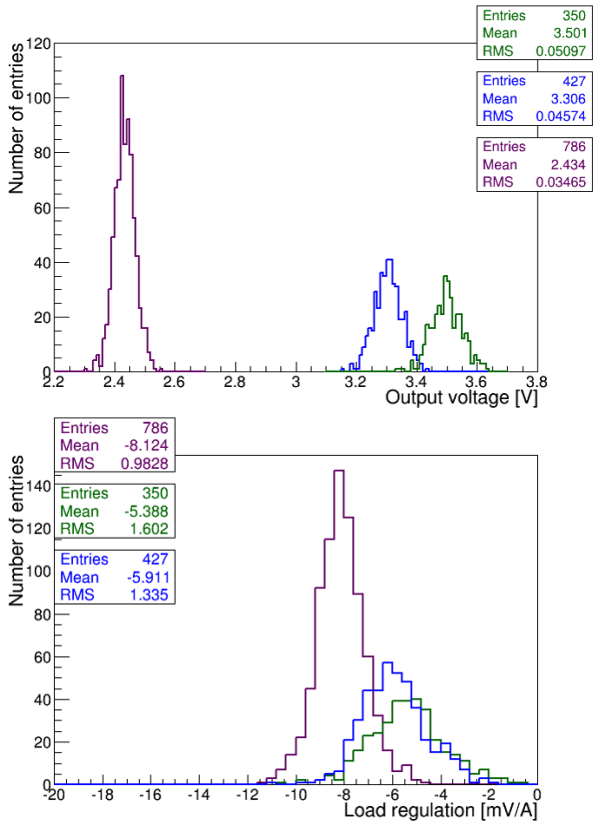

Figure 5: Distribution of the measured output voltages (top) and the load regulation (bottom) of all produced and qualified converters of the three output voltage types: 2.4, 3.3, and 3.5 V. The load regulation measures the change of converter output voltage with output current.

5. Electrical and Thermal Integration of the Converters

Figure 6 shows a section of the Bus Board with 4 DC-DC converters mounted. There are empty positions on both sides in which aluminium cooling bridges are visible, to which the converters are screwed such that the cooling contact at the bottom of the converter PCB makes good thermal contact with the bridge. The bridges themselves consist of an upper and a lower part, which are clamped around the CO_2 cooling pipes running along the upper and lower end of the bridges. With the CO_2 running at $-20°C$, the top of the converter shield has a temperature of around $-5°C$. Fig. 7 shows a fully loaded channel with 13 pairs of DC-DC converters.

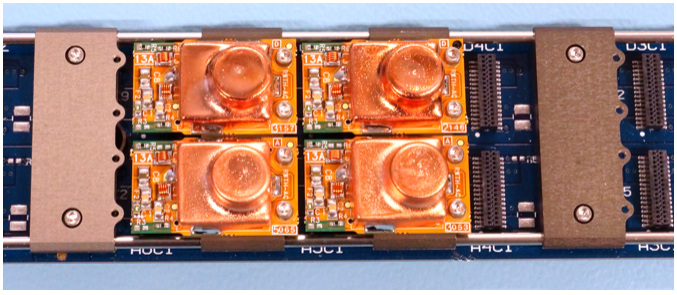

Figure 6: Close-up view of a section of a Bus Board with four DC-DC converters mounted on the cooling bridges. These bridges are glued to the Bus Board and clamped around the CO_2 cooling pipes running along the upper and lower edges of the picture.

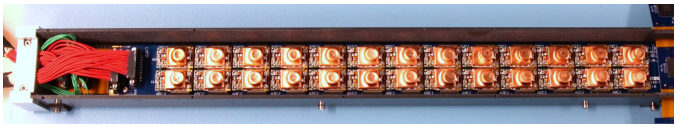

Figure 7: A prototype channel of the supply tube equipped with a Bus Board fully loaded with 26 DC-DC converters.

6. Summary and Outlook

The new CMS pixel detector will be powered through a DC-DC conversion powering scheme. This allows the operation of a detector system with much improved rate capability and an additional detection layer for robust pattern recognition through the legacy cable plant and power supplies. The production of the DC-DC converters and all required power PCBs was completed in November 2015. Installation of these components in the pixel support structures starts in February 2016. Installation of the new pixel detector in CMS is planned for the extended year end technical stop 2016/17.

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