SALT, a dedicated readout chip for strip detectors in the LHCb Upgrade experiment

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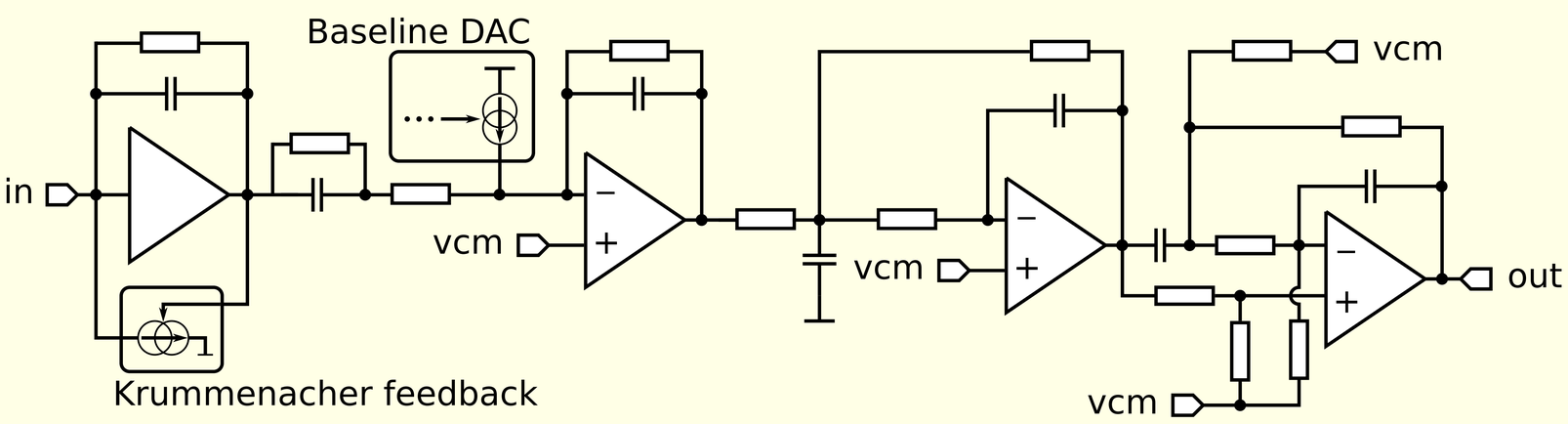
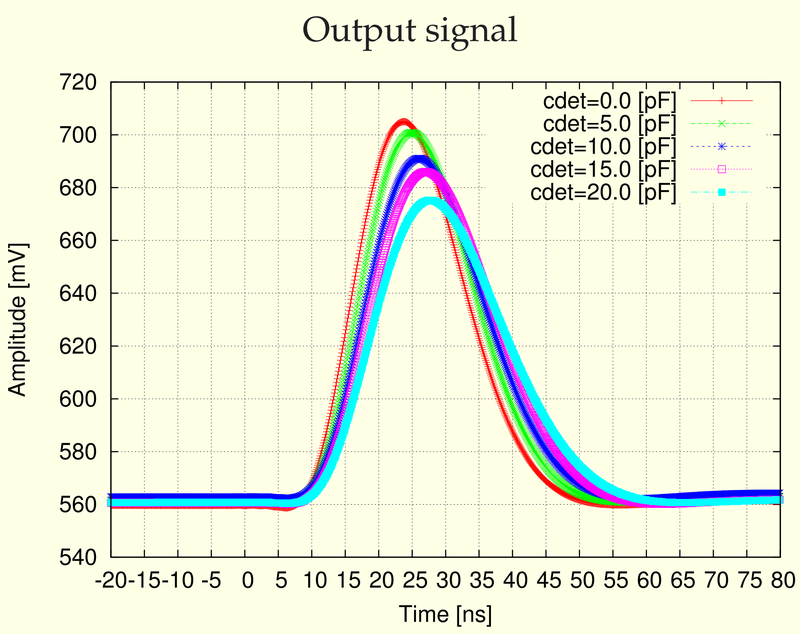
Introduction

Silicon strip detectors in the upgraded Tracker of LHCb experiment require a new readout ASIC. A project of a 128-channel ASIC called SALT (**S**ilicon **A**SIC for **L**HCb **T**racking), is ongoing. The SALT extracts and digitises analogue signals from the sensor, performs digital processing and transmits serial output data. It is designed in CMOS 130 nm technology and uses a novel architecture comprising an analog front-end and 6-bit ADC in each channel. A dedicated DLL is used to control precisely the ADC sampling phase.
The digitised data from each ADC channel are processed in a DSP block which first subtracts pedestals and calculates mean common mode (MCM), as an average over channels without signal. Then the MCM is subtracted in each channel. The last DSP step is zero suppression (ZS). After the ZS the data are buffered in SRAM, a data packet is formed and sent to DAQ (Tell40) via a number of serial DDR e-links. The serialization and fast data transmission utilize a dedicated ultra low power PLL circuit.
The prototypes of key components: 6-bit ADC, preamplifier with shaper and single-ended to differential converter, PLL and DLL were designed and fabricated in two 130 nm CMOS technologies: A and B. The tests of key components in process A were completed while for process B are in progress.

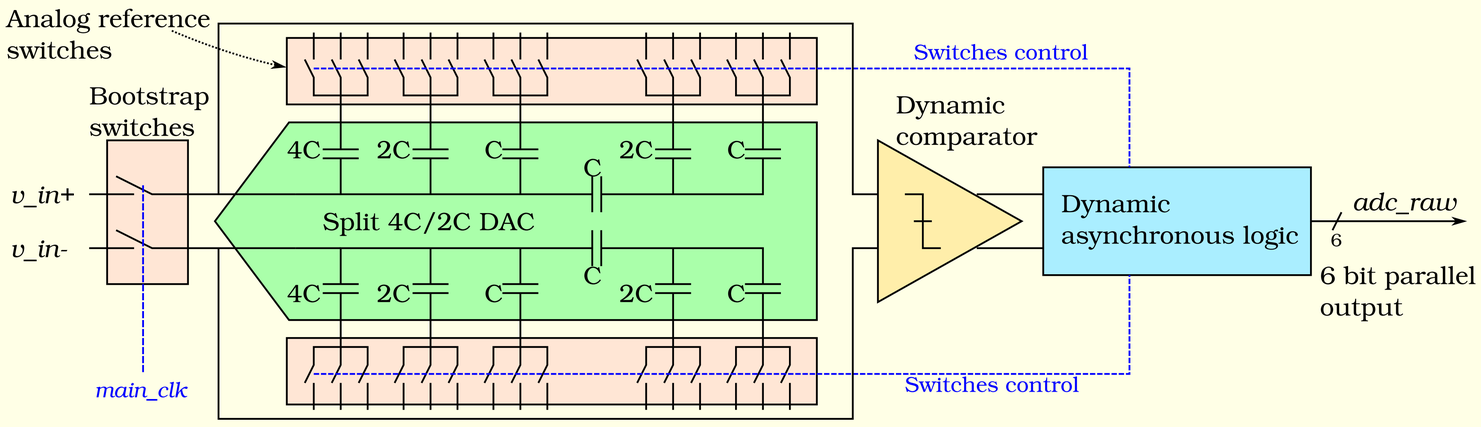
Analogue front-end

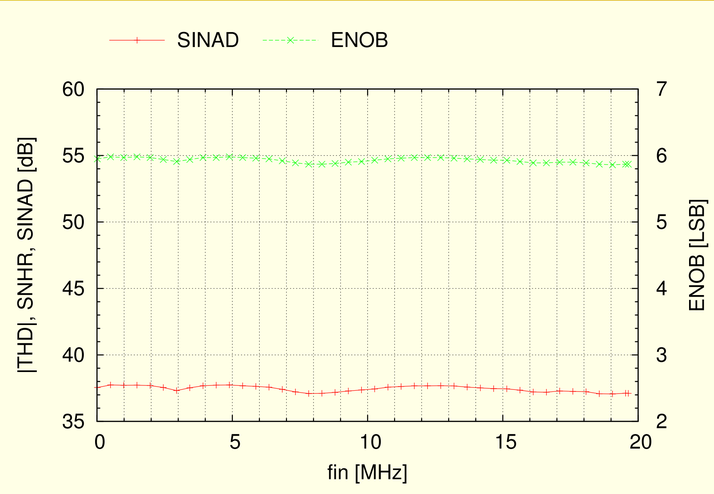




The front-end comprises a charge preamplifier and a fast shaper (T_{peak}=25ns and fast recovery) required to distinguish pulses from subsequent LHC bunch crossings at 40 MHz. To achieve this, a specific non-standard shaper is required. The prototype front-end (process A) works with sensor capacitances between 5–30 pF.

6-bit ADC



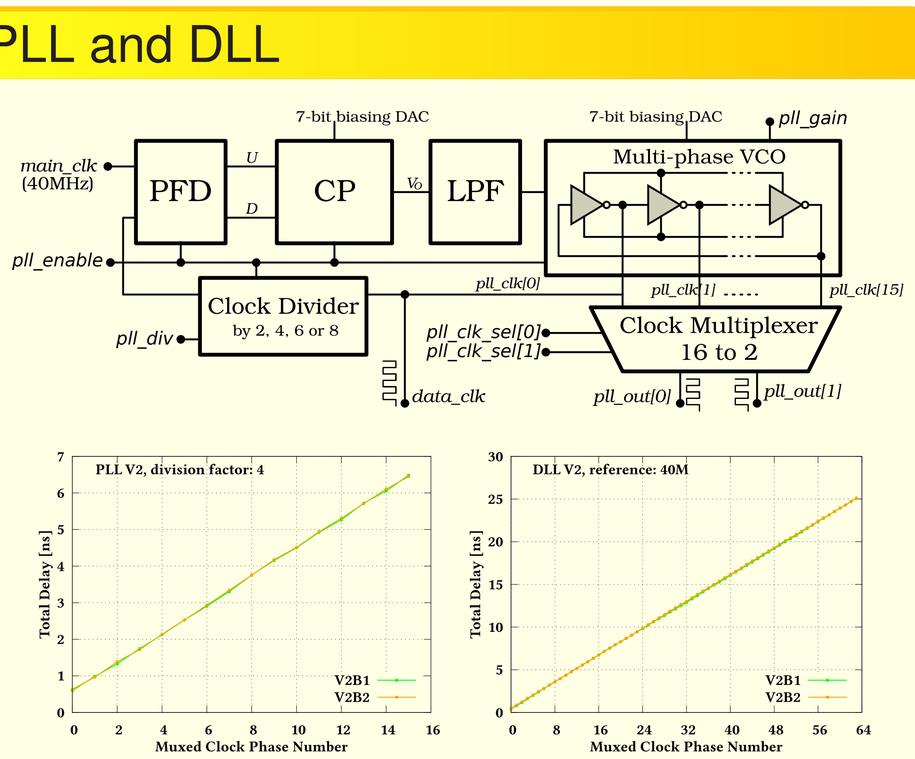


Specification:
- resolution 6 bit
- sampling frequency 40 MHz
- power consumption @ 40MSps < 0.5 mW

Architecture:
- merge capacitor switching (MCS) with split capacitor DAC
- dynamic comparator
- dynamic asynchronous logic

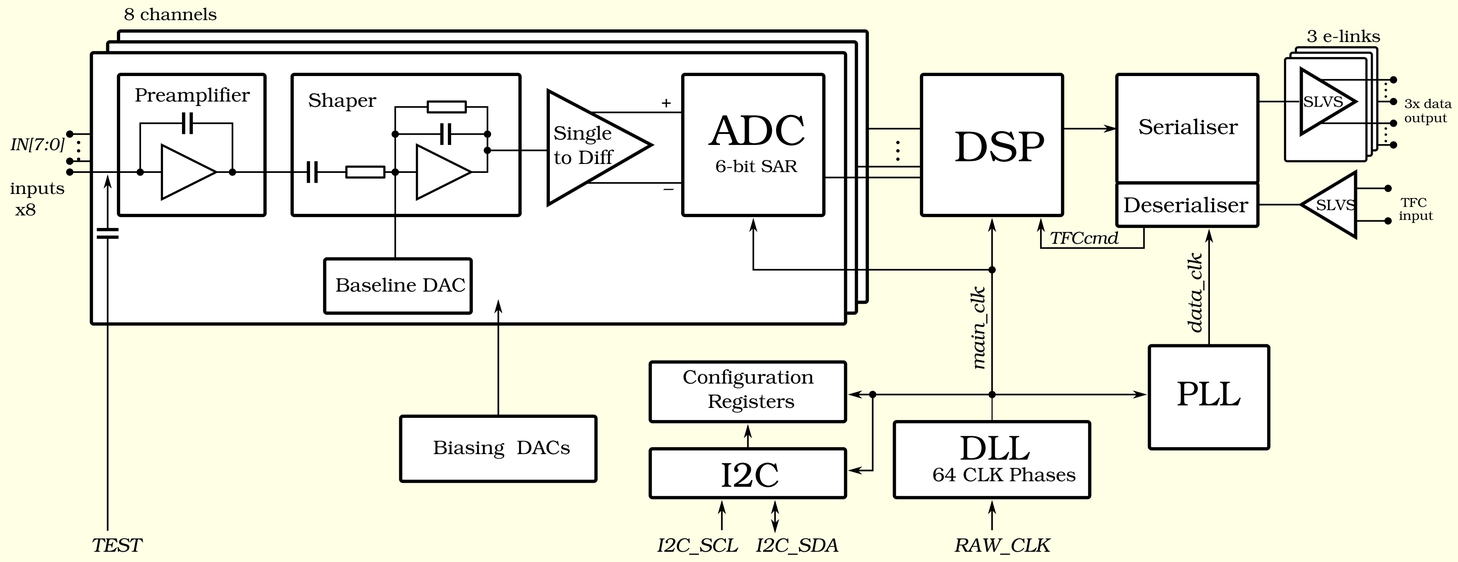
Scan of dynamic parameters vs input signal frequency, performed at 40 MHz sampling frequency, gives effective resolution ENOB>5.85.

PLL and DLL



The PLL and DLL were manufactured and successfully measured in both technologies A & B. See talk by Mirosław Firlej: *Development of a low power Phase-Locked Loop (PLL) and Delay-Locked Loop (DLL) in 130nm CMOS technology*.

SALT 8-channel prototype



The 8-channel SALT prototype was designed and fabricated in technology B. Basic tests show fully functionality of slow control (I^2C), input (TFC) and output (data) interface. The PLL based (de)serialisation also works correctly. Other tests are in progress.

A full 128-channel prototype (including: calibration circuit, TFC debug registers, SEU mitigation, 5 elinks, etc.) in technology B is planned to be submitted in February 2016.